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Effects of Aging and Moisture on 1/f Noise in MOS Devices

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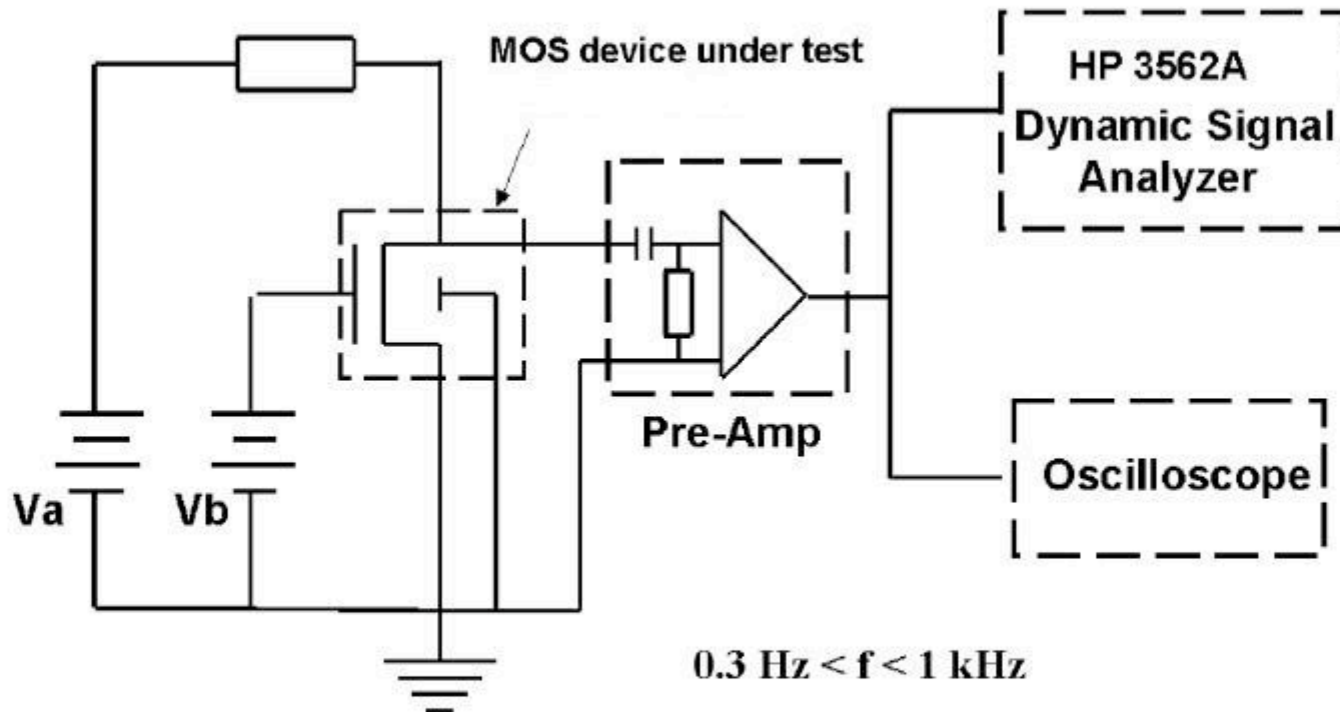
Outline

- Motivation
- Experimental details
  - Devices under test
  - Noise system set-up
- Results and discussion
  - Aging effects
  - Moisture exposure before irradiation
- Mechanisms
- Conclusion

Experimental Details

- **Devices: 3 µm x 16 µm (*L* x *W*) *n*- and *p*MOS devices, poly gate (mid 1980's Sandia parts)**
  - **Exposed (to humidity) vs. control (hermetically sealed)**
    Some devices exposed to 85% relative humidity at 130 °C for 1 week; all pins shorted; non-hermetic
  - **Pre- and post-rad**
  - **t_{ox} = 32 nm, 48 nm, 60 nm**
  - **w and w/o high temperature N_2 post-oxidation anneals**
- **Noise test: noise power spectral density S_V (corrected for background noise)**
- **V_{th} measurements**

Noise System Set-up



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Aging effects

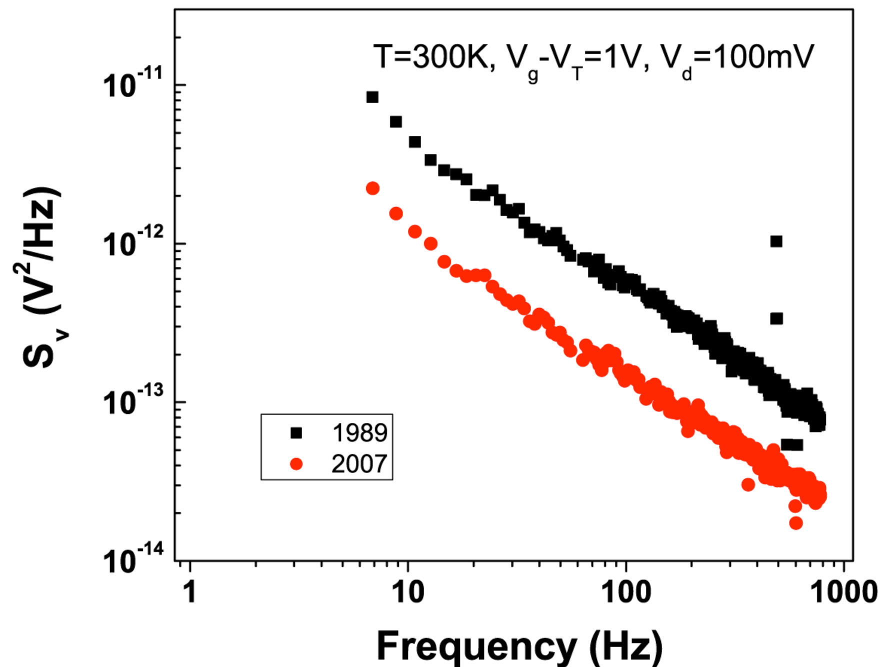
Effects of 18 Years Storage (non-hermetic) on Noise

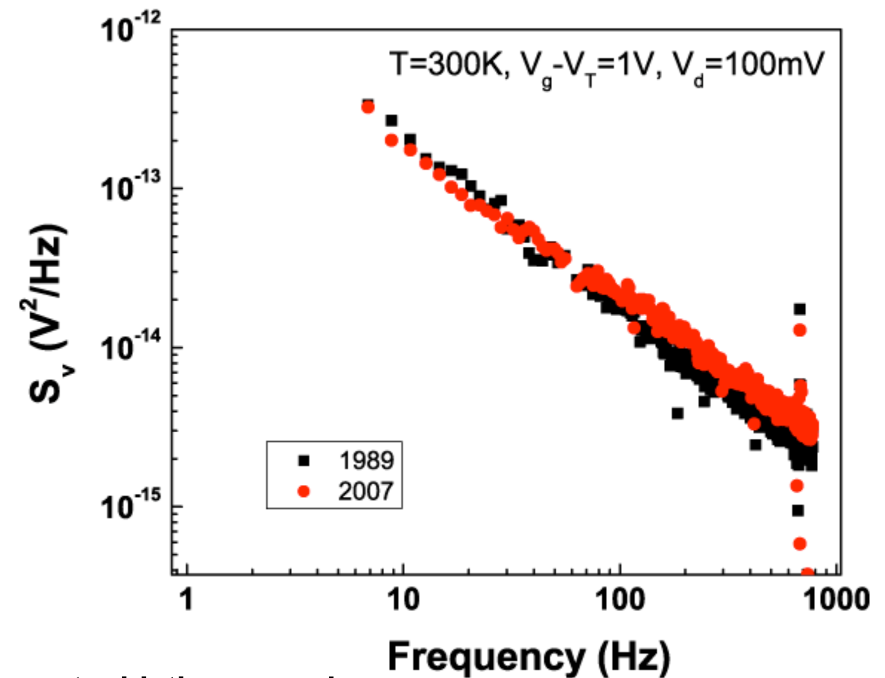
N_2 postoxidation anneal

t_{ox} = 48 nm, sample C

No N_2 postoxidation anneal,

t_{ox} = 60 nm, sample D

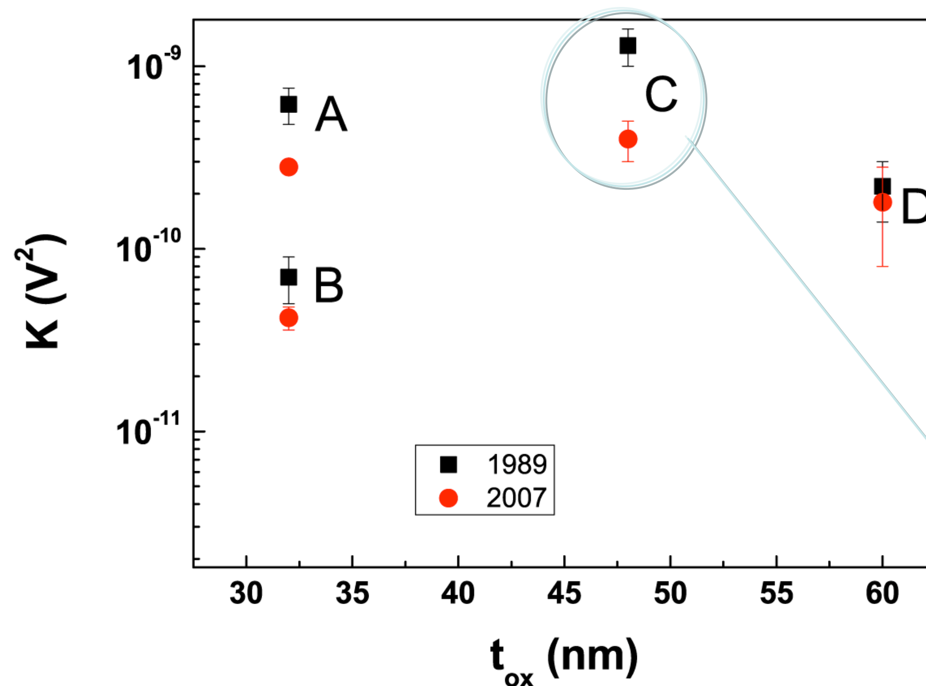




A: 15 min, 1000 ºC dry oxide; 30-min, 1100 ºC N_2 postoxidation anneal
B: 25 min, 850 ºC steam oxide; no postoxidation anneal
C: 30 min, 1000 ºC dry oxide; 30-min, 1100 ºC N_2 postoxidation anneal
D: 50 min, 850 ºC steam oxide; no postoxidation anneal

X. J. Zhou et al., Appl. Phys. Lett., 91, p. 173501 (2007)

Changes in noise vs. processing



$$K = S_v \frac{f^{\gamma}(V_g - V_t)^2}{V_d^{\ 2}}$$

- For devices receiving N_2 anneals: significant decrease in K
- For devices w/o N_2 anneals: negligible change in K

$$N_{bt} \cong E_g LW \frac{(\varepsilon_{ox}/t_{ox})^2 \ln(\tau_1/\tau_0)}{qkT} K$$

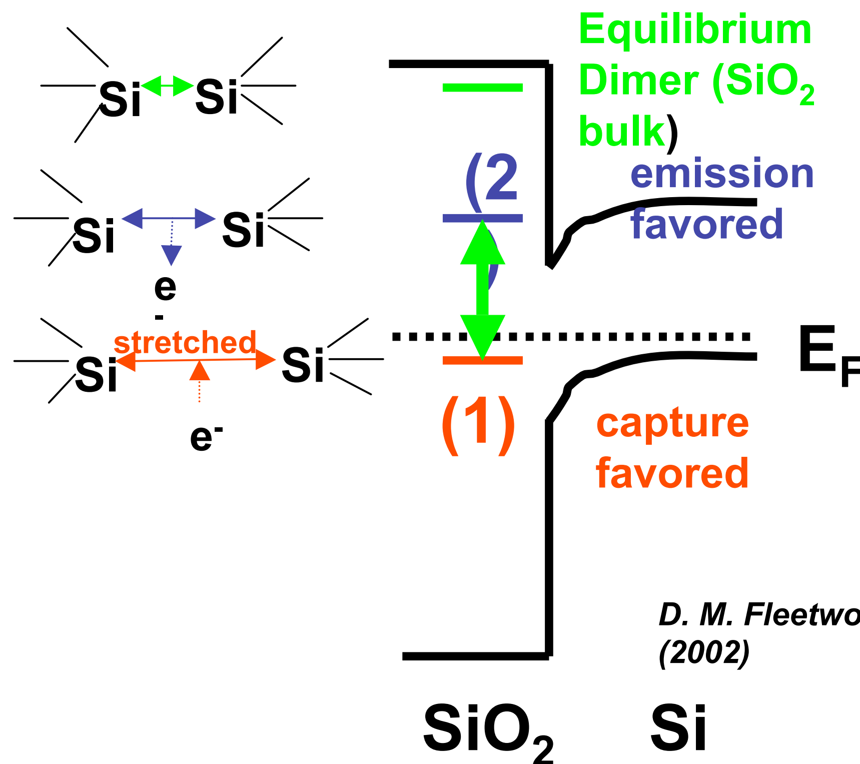
D. M. Fleetwood et al., J. Appl. Phys. 58, p. 5058 (1993)

N_{bt} = 1.5 × 10^{11} cm^{-2} (1989) → 4.5 × 10^{10} cm^{-2} (2007) ↓ with aging;

ΔN_{bt} = 1 × 10^{11} cm^{-2} after 18 years of aging

A: 15 min, 1000 ºC dry oxide; 30-min, 1100 ºC N_2 postoxidation anneal
B: 25 min, 850 ºC steam oxide; no postoxidation anneal
C: 30 min, 1000 ºC dry oxide; 30-min, 1100 ºC N_2 postoxidation anneal
D: 50 min, 850 ºC steam oxide; no postoxidation anneal

Effects of strained bonds associated with O vacancies



D. M. Fleetwood et al., IEEE Trans. Nucl. Sci. 49, 2674 (2002)

- Stretched Si-Si bond near interface --- capture strongly favored (1)
- After capture, the negative charge causes the Si-Si bond length to be reduced, increasing the energy of the trap level, and causing the electron to be emitted (2)
- Reconfiguration leads to decrease in the number of strained bonds (and/or for O vacancies) devices exposed to N_2 anneals

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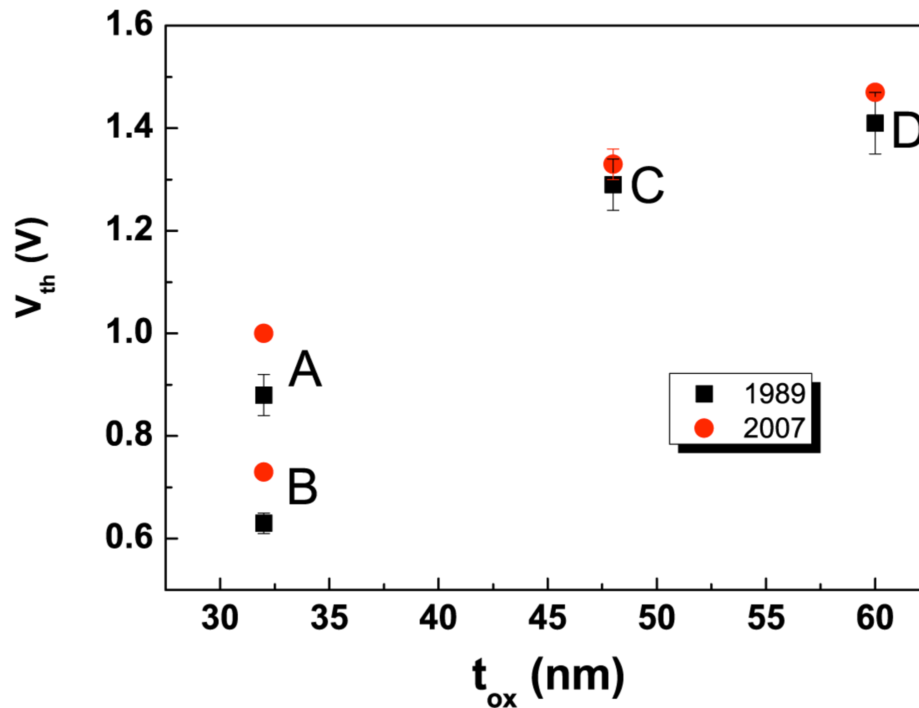
ΔV_{th} as a function of t_{ox} and processing



- Positive ΔV_{th} observed for devices w & w/o N_2 anneals
- Due to electron traps or interface traps – due to moisture/hydrogen (?)
  - Does not affect noise significantly in this case

A: 15 min, 1000 ºC dry oxide; 30-min, 1100 ºC N_2 postoxidation anneal
B: 25 min, 850 ºC steam oxide; no postoxidation anneal
C: 30 min, 1000 ºC dry oxide; 30-min, 1100 ºC N_2 postoxidation anneal
D: 50 min, 850 ºC steam oxide; no postoxidation anneal

Consequences of aging effects

- **Relaxation in MOS devices with relatively high densities of O vacancies and strained Si-Si bonds.**
  - **Can lead to changes in modern MOS performance, reliability and radiation response in systems operating for long times (e.g., in space)**
  - **may cause mobility decrease, if deliberately introduced strains relax similarly over long times**
- **Important to high-K dielectrics or devices using strain engineering.**

Moisture exposure

t_{ox}= 32 nm, L × W = 3 μm × 16 μm, *n*- and *p*- MOSFETs

exposed: 85% RH @ 130 °C for 1 week;

control: hermetically sealed

10 keV X-ray, Dose rate: 31 krad (SiO_2)/min, gates were biased at +6 V and all other pins were grounded

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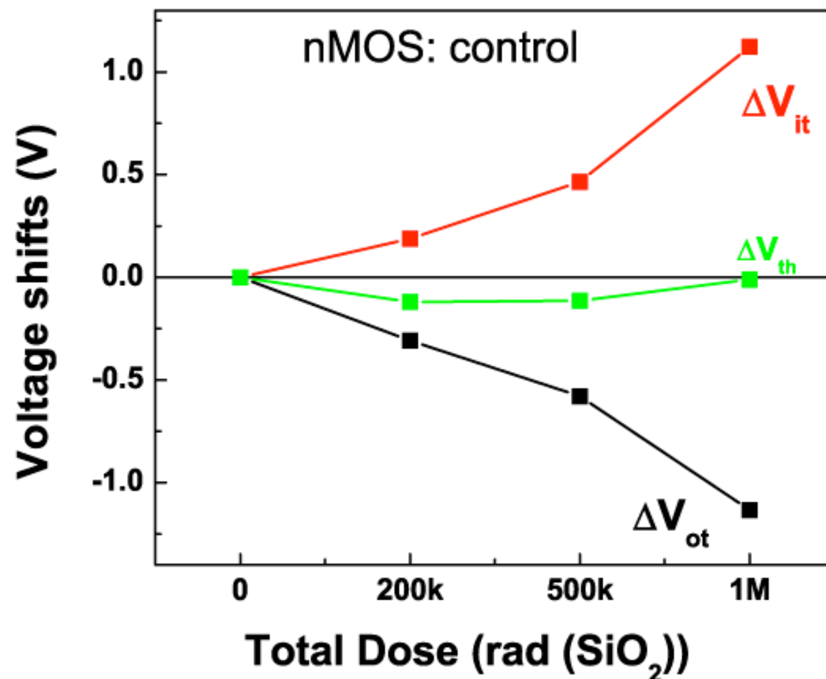
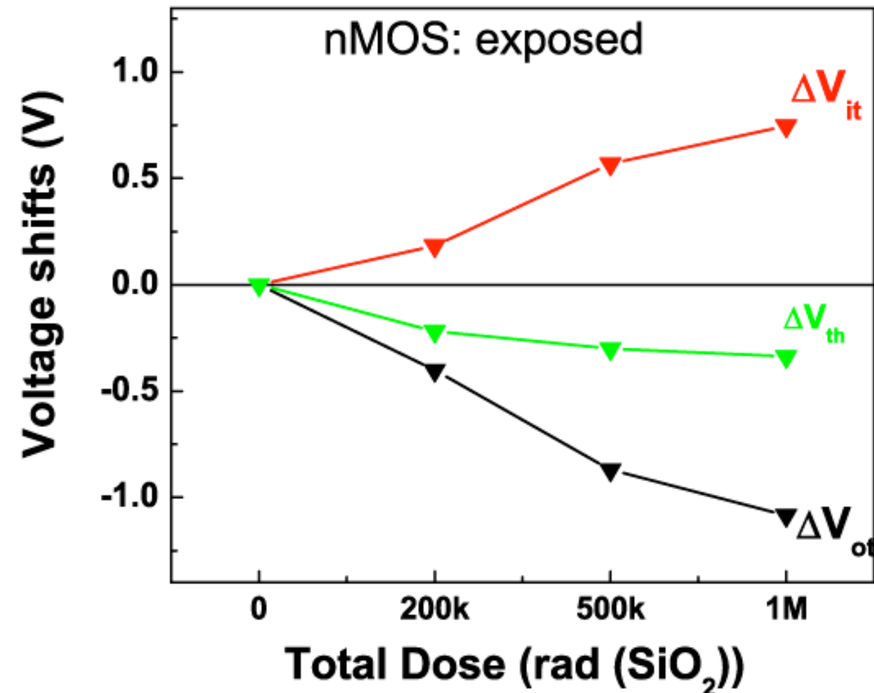
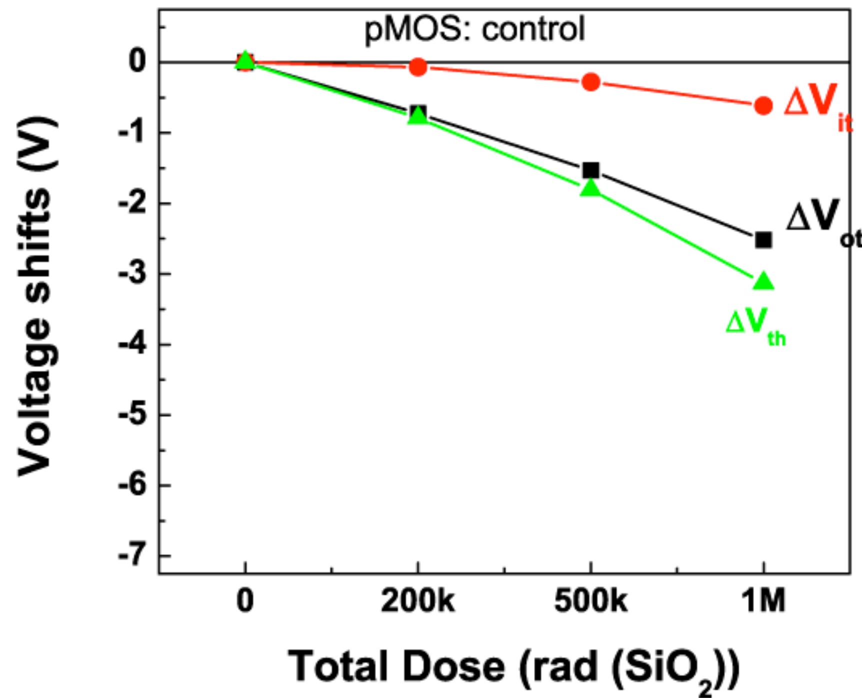
Voltage Shifts for Control vs Exposed Devices: nMOS

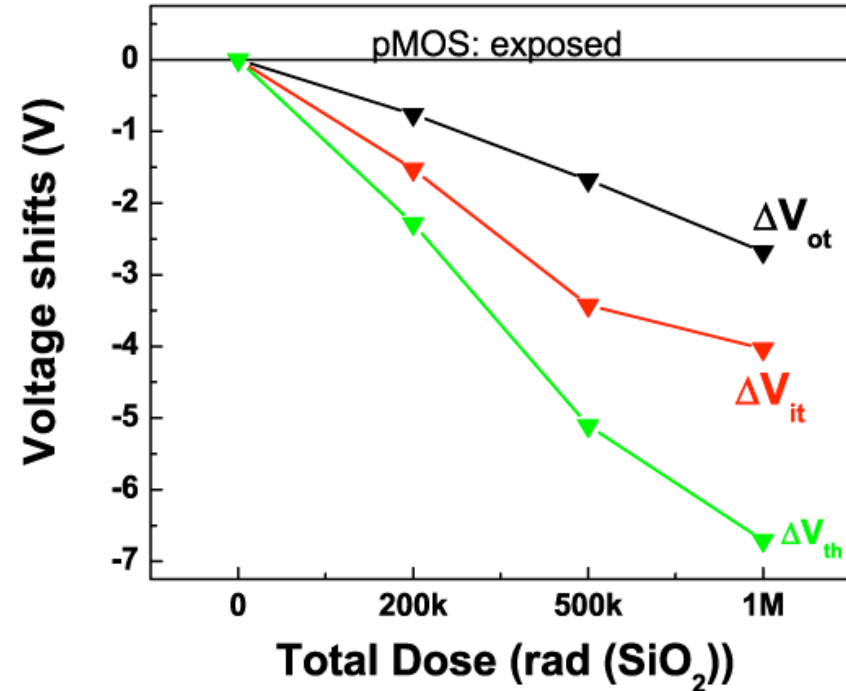




- **Voltage shifts due to radiation induced oxide trapped charges and interface traps are comparable for *n*MOS with moisture exposure.**

Voltage Shifts for Control vs Exposed Devices: pMOS

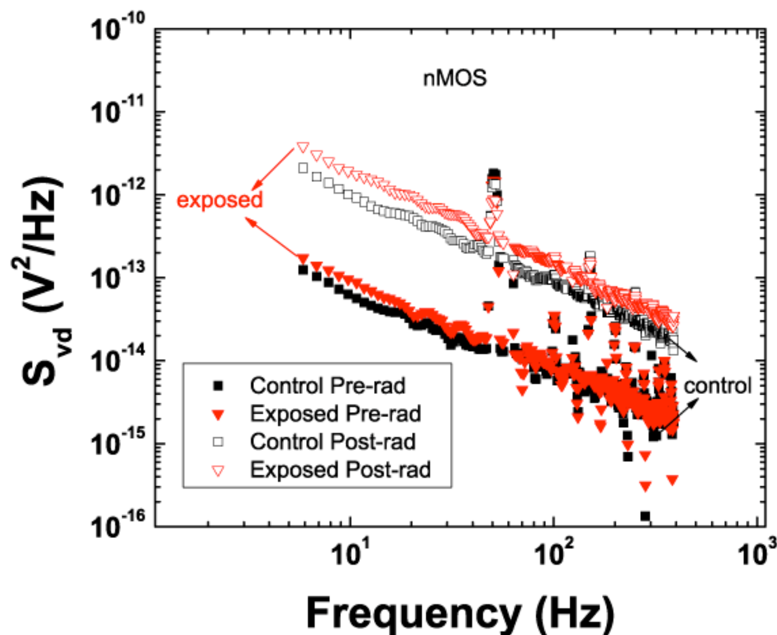


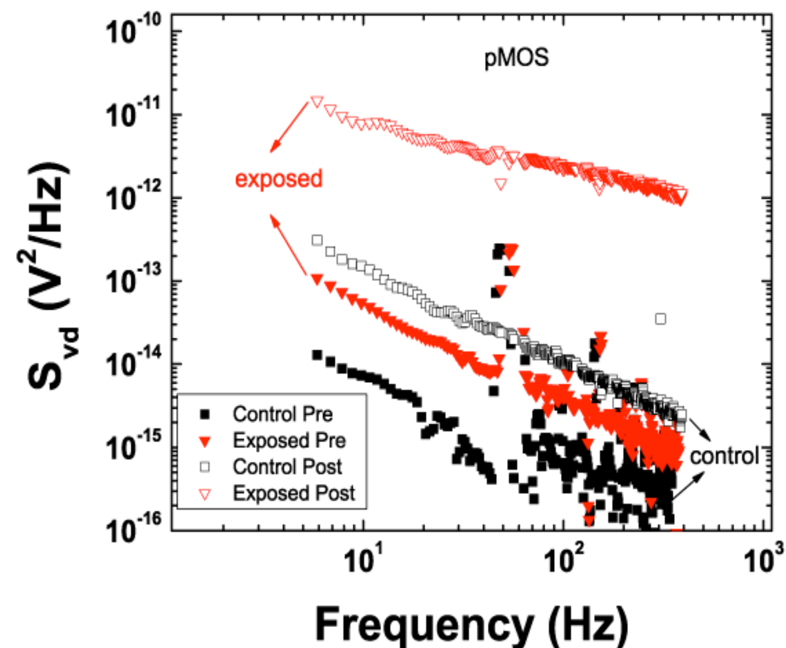


- There are large differences in defect density for *p*MOS with moisture exposure.

Radiation Response for Control vs. Exposed Devices

Total dose: 1 Mrad(SiO_2) Noise measurements: ($V_g - V_{th}$ = 1 V; V_d = 100 mV)

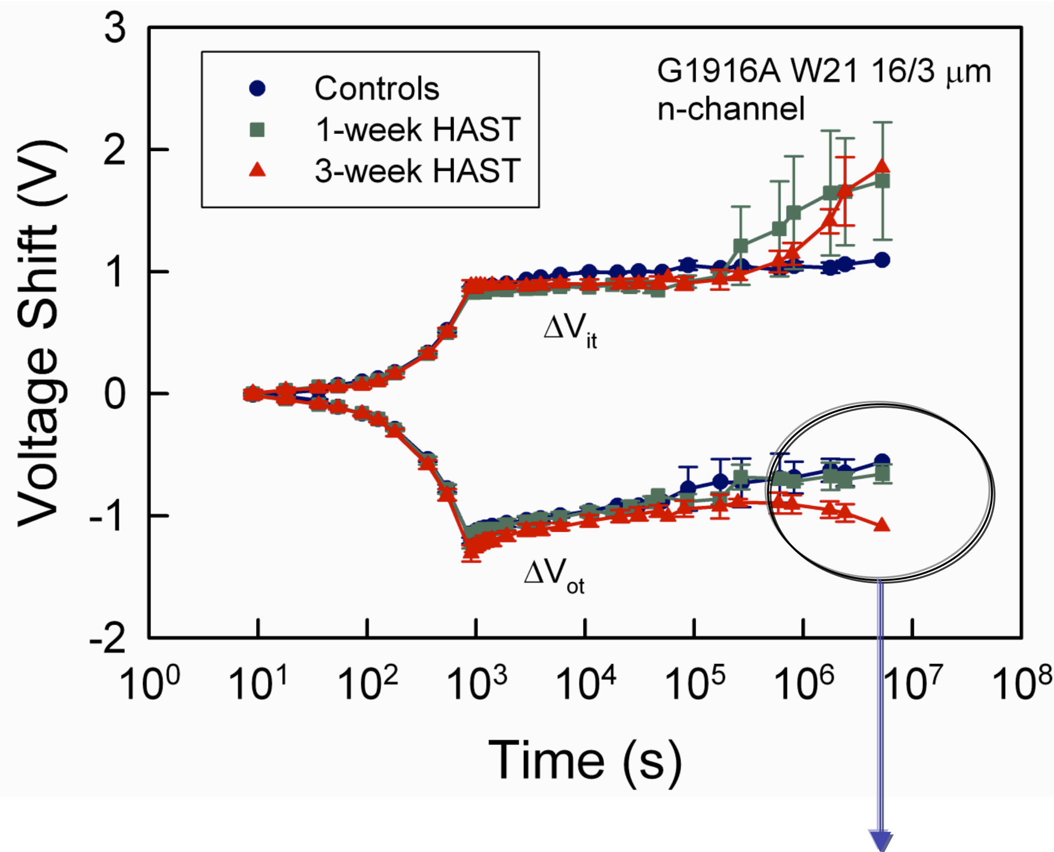




- **pMOS devices have more pronounced changes after irradiation due to the moisture exposure**

  -- Increased oxygen vacancy densities during the exposure

Longer HAST (highly accelerated stress test) induces an increase in trapped charge after ~10^5 s post-rad anneal for nMOS



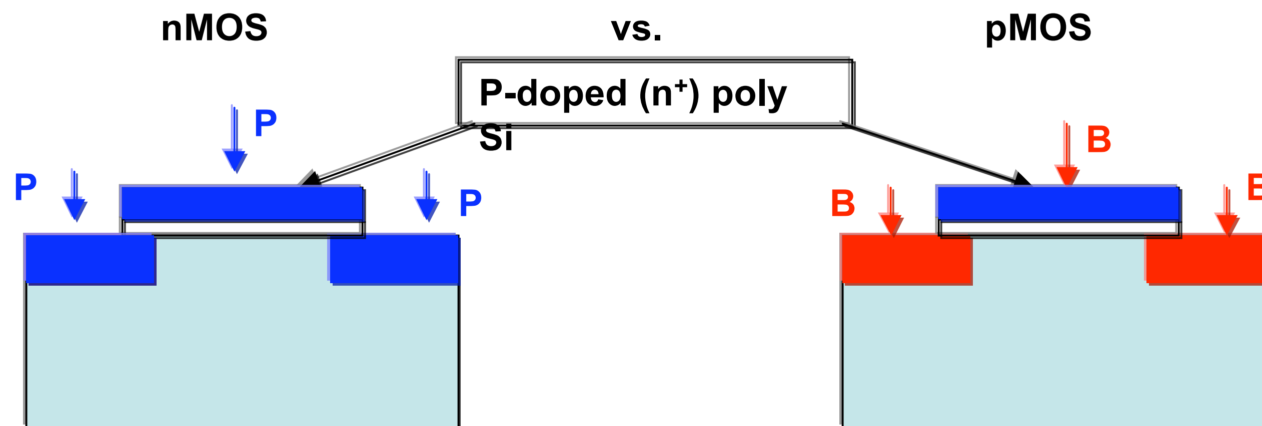
- **During the HAST stress all devices were biased with all pins shorted**
- **Rad bias: V_{GS} = 4 V**
- **Dose: 500 krad(SiO_2)**
- **Schwank et al., IEEE NSREC 2008**

nMOS are also sensitive to moisture exposure after longer times (e.g., 3 weeks)

pMOS vs. nMOS charge trapping/noise

- *Phosphorus prevents moisture diffusion*
  - *PSG is used as moisture barrier for the whole chip.*
  - *More P in the materials surrounding the gate oxide for nMOS than pMOS.*
    - *Further inhibits final stage of moisture diffusion for nMOS.*
    - *B compensates P in the poly Si, facilitating diffusion of hydrogenous species through poly-Si grain boundaries for pMOS.*

- *Enhanced O vacancies for BSG than PSG (Warren et al., IEEE TNS, 42, p.1731, 1995)*



Conclusions

- **Decrease in low-frequency noise observed with 18 years of room-T storage (non hermetic)**
  - **Most pronounced for devices with high O vacancy densities.**
  - **Up to 3× decrease in border trap density.**
  - **Accompanied by ~ 10% increase in V_{th} for transistors.**
    - Due to interface trap buildup during aging.
    - Perhaps related with hydrogen.

- **Moisture exposure increases pMOS ΔV_{ot} and noise**
  - **No significant changes in *n*MOS for short times.**
  - **Phosphorus inhibits moisture diffusion for nMOS.**
  - **More charge trapping in BSG than PSG.**