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Radiation Effects on ZRAMs

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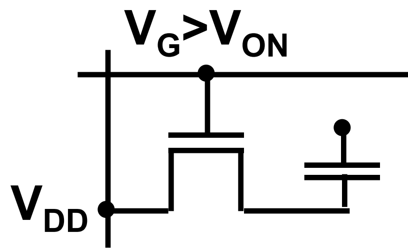
Outline

- Introduction
- Experimental Details
  - Test Conditions
  - Mechanism
  - Irradiation Conditions
- Results and Discussion
  - Program windows for FinFETs with different fin widths
  - Total dose radiation effects
- Conclusion

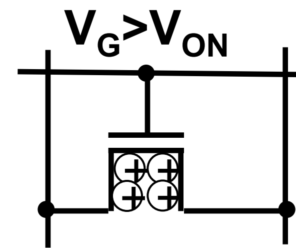
Introduction

What is a ZRAM?

-- Zero capacitor DRAM, a real 1T DRAM cell



Traditional DRAM cell



1T-DRAM cell, Z-RAM cell

Why use ZRAM?

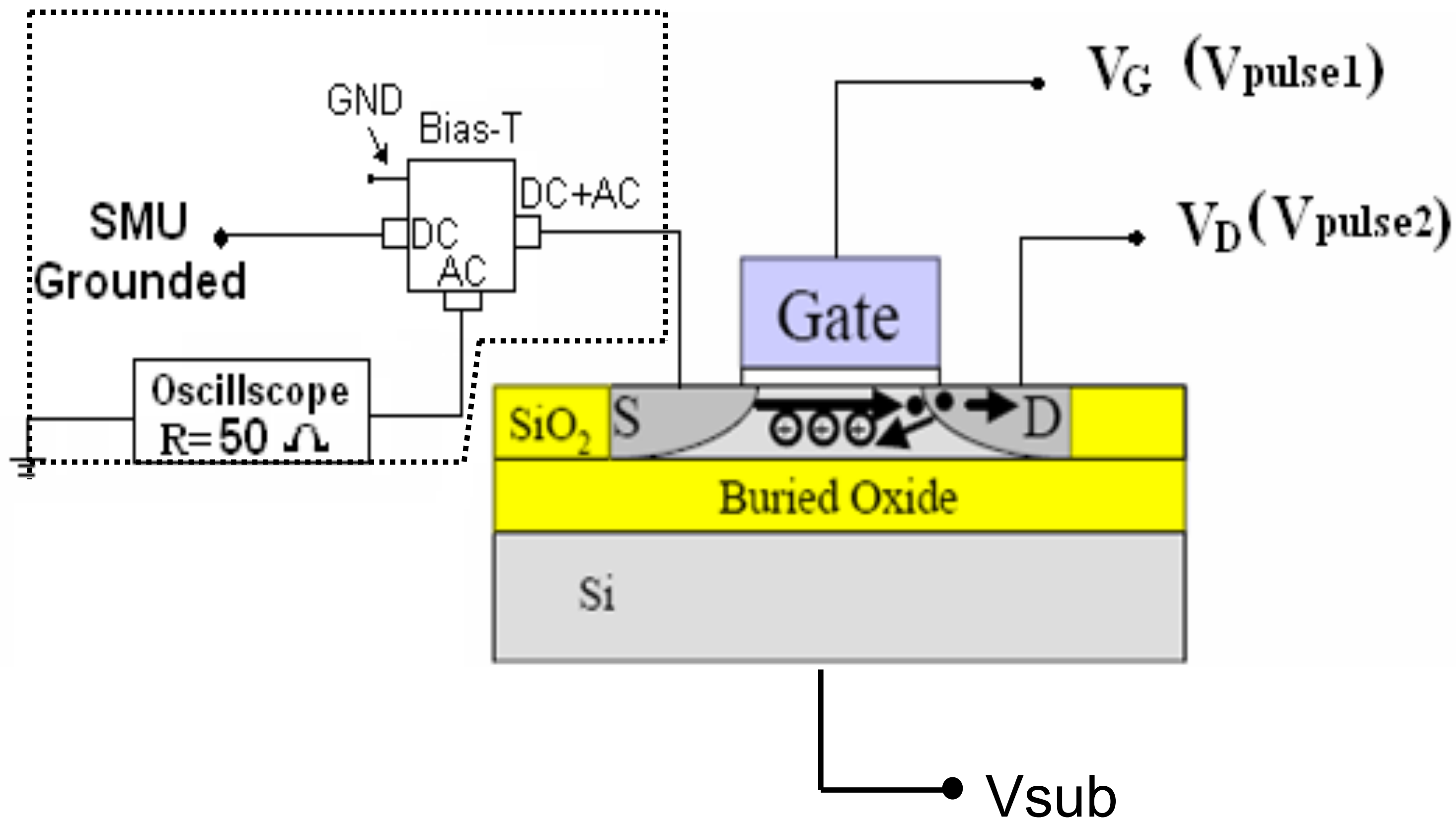
-- Scalability, high performance, low power, low cost……

How to characterize ZRAM?

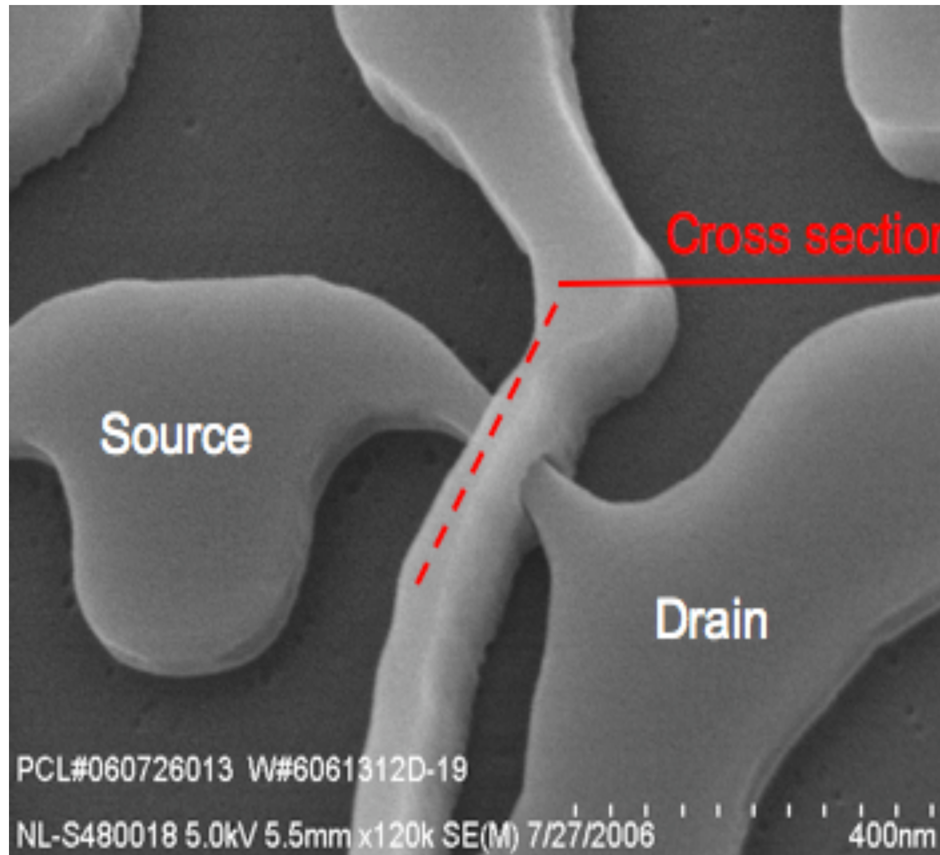
-- Gate Induced Floating Body Effect

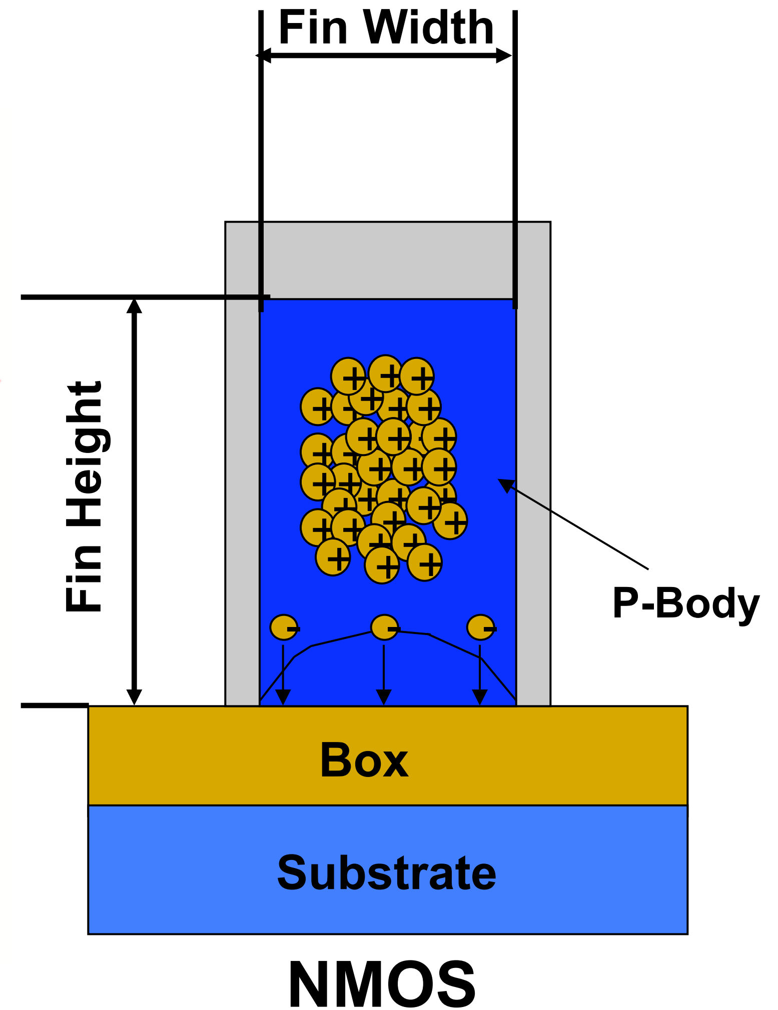
M. Bawedin, S. Cristoloveanu a, D. Flandre, Solid-State Electronics 51 (2007) p.1252

ZRAM cell Programming and Readout



Mechanisms





Devices and Irradiations

Characterization of ZRAM:

Device: n- and p-FinFETs with different fin widths, 58 nm fin height and 2 nm gate oxide (SiO_2)

ZRAM Test: I_D vs. V_G under different back-gate bias; I_D/I_S current vs. time under V_G/V_{BG} and V_D pulse

Irradiation Test Conditions:

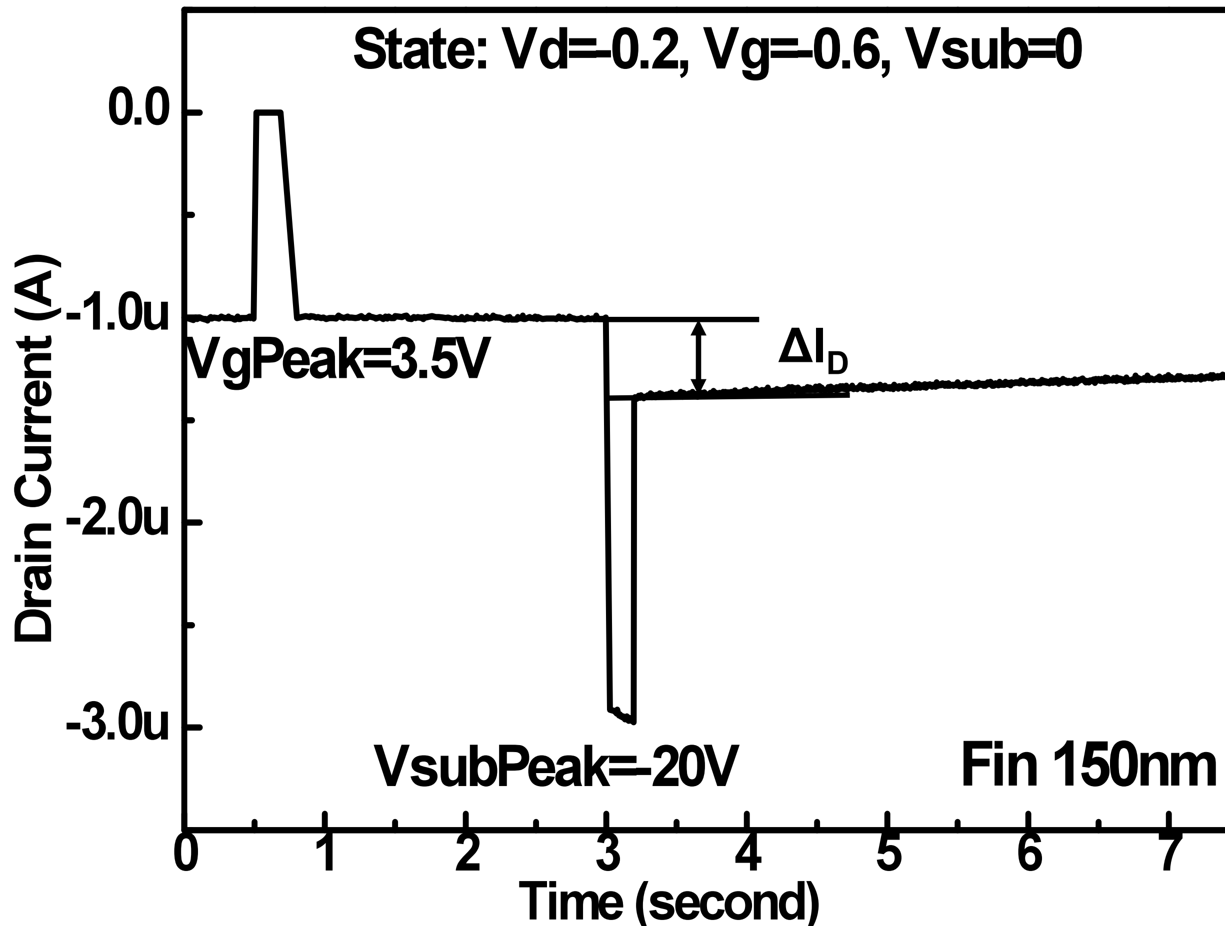
ON-state: V_G= 0.5 V, V_D = V_S = Vsub = 0 V (NMOS);

OFF-state: V_G = V_S = V_{sub} = 0 V, V_D = –0.5 V (PMOS);

Total dose: 0 ~ 500 k with 10-keV X-rays

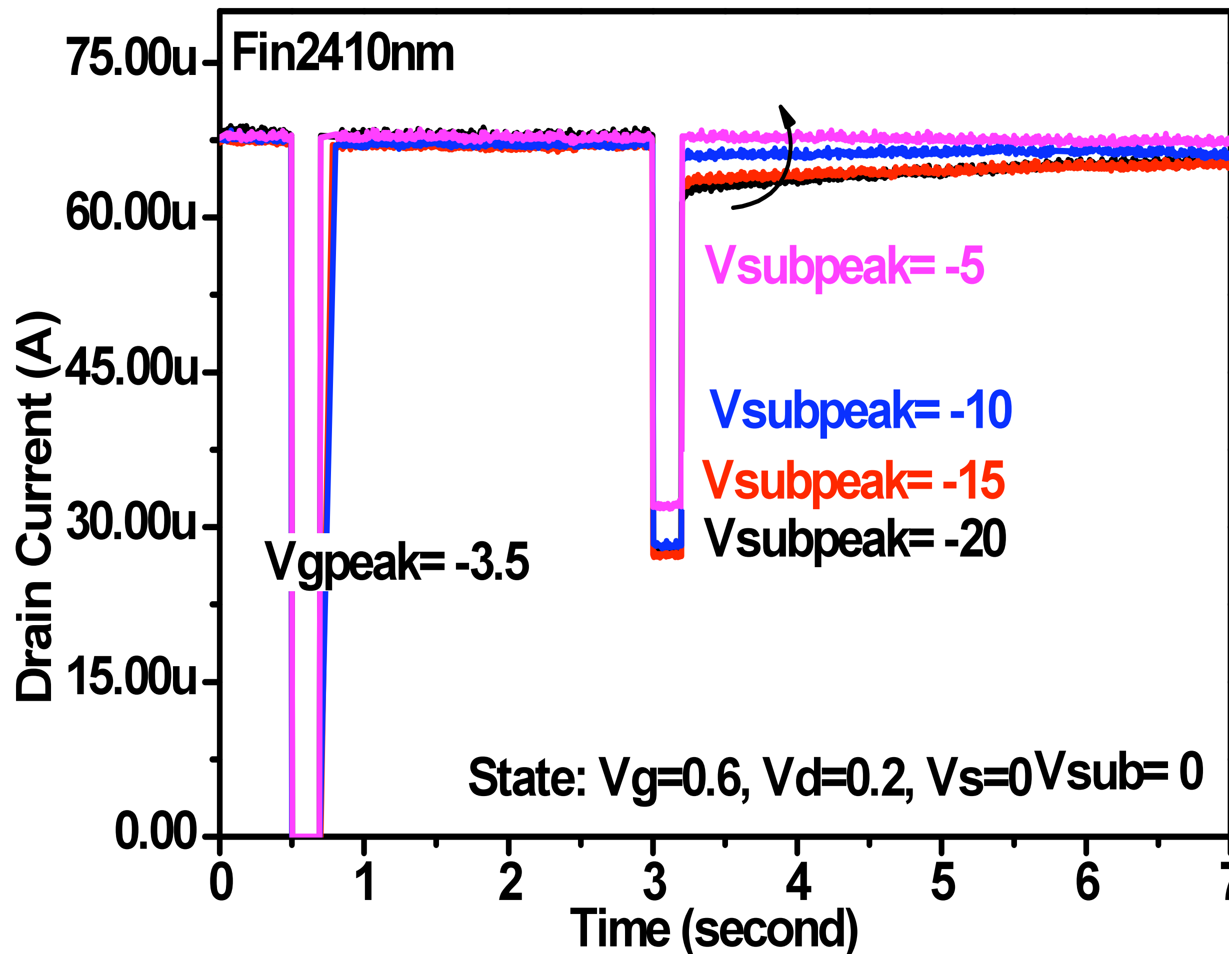
Results & Discussions

Transient effect on ZRAM cell/pMOS



- Large current transient is induced by back-gate pulse.
- Memory sensor margin is 40% ($\Delta I_D/I_0$).
- Sufficient for efficient memory operation.

Transient effect on ZRAM cell/nMOS



- **Maximum memory sensor margin is only ~7.6% ($\Delta I_D/I_0$).**
- **Memory window and retention time increase with back-gate pulse magnitude, but << pMOS.**
- **Stored electrons more stable than holes in these particular devices.**

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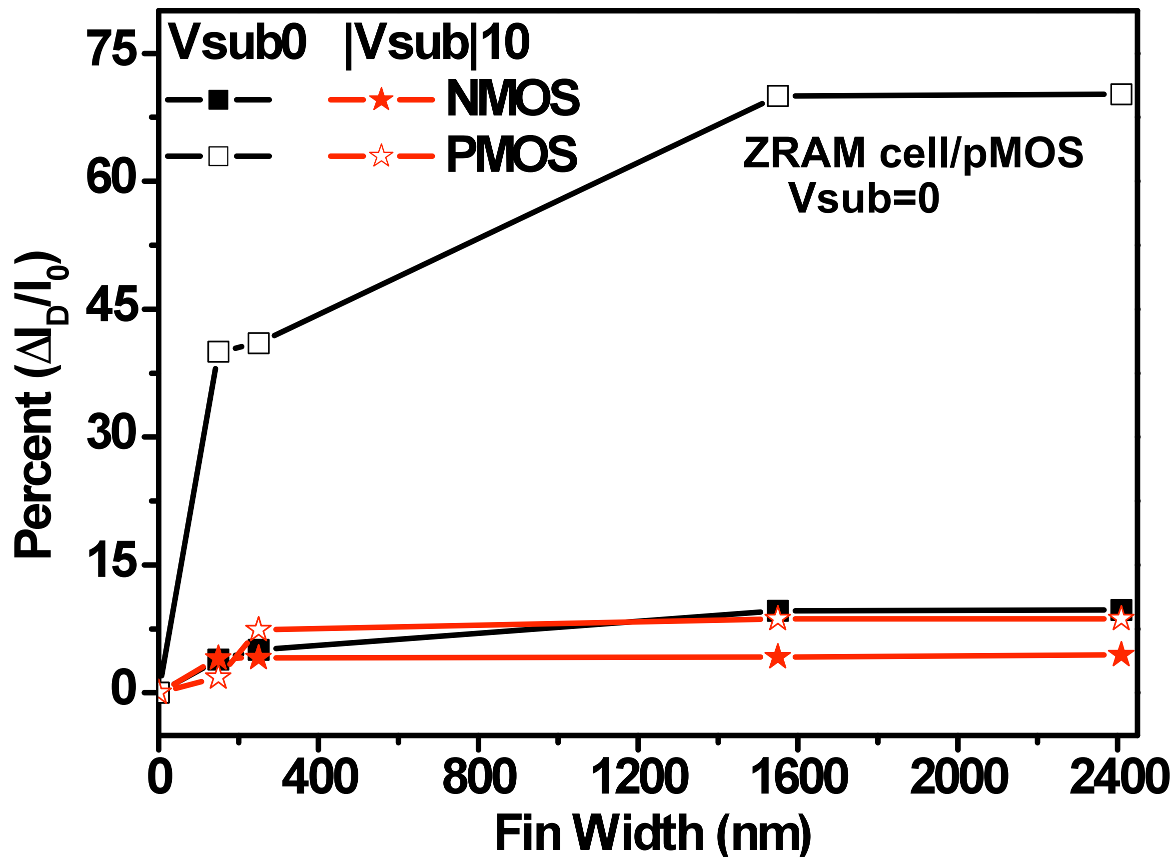
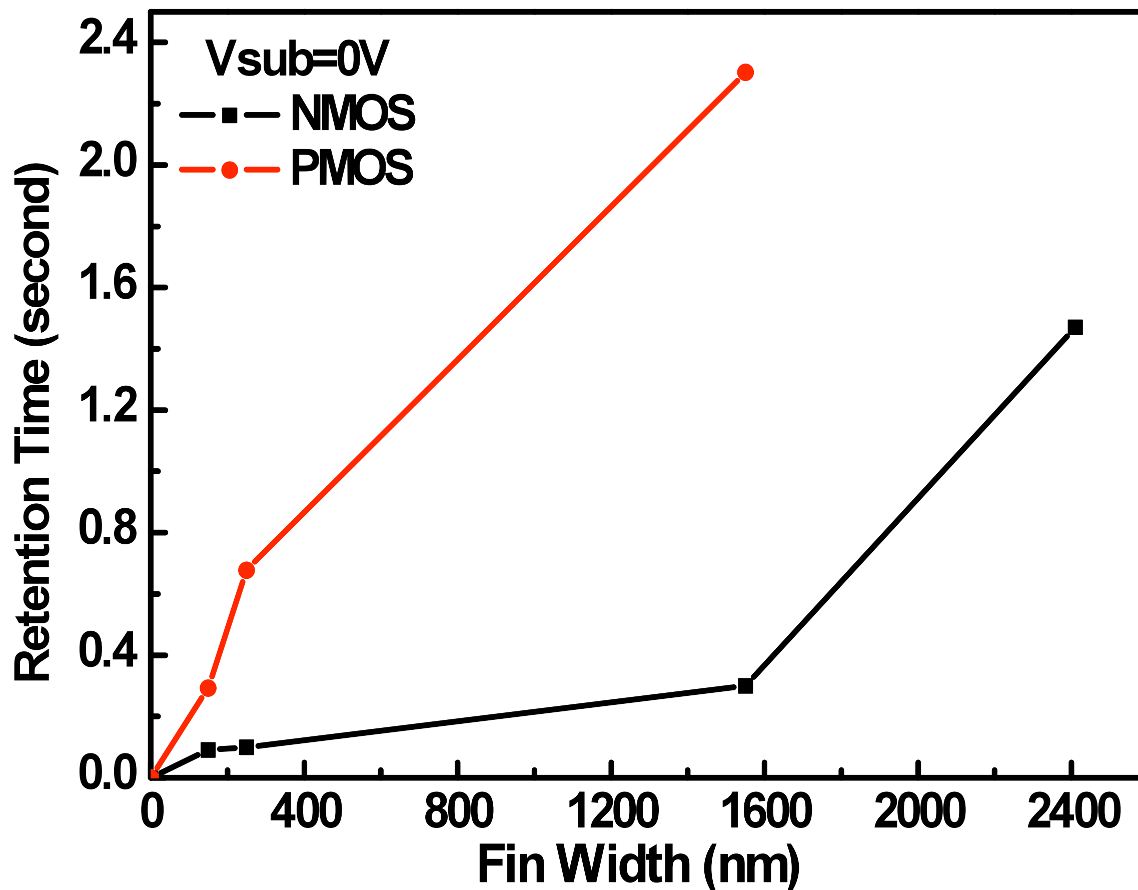
Fin width dependence of ΔI_D



- Program window of the ZRAM cell increases with increasing fin width.
- ZRAM/pMOS has a larger program window than nMOS with same fin width.
- The program window strongly depends on the back-gate bias (V_{sub}).

Fin width dependence of retention time



Retention time is defined as the time it takes to lose 50% of the charge.

- Retention time increases with fin width.
- ZRAM/pMOS has a longer retention time than nMOS with same fin width for these devices and programming conditions.

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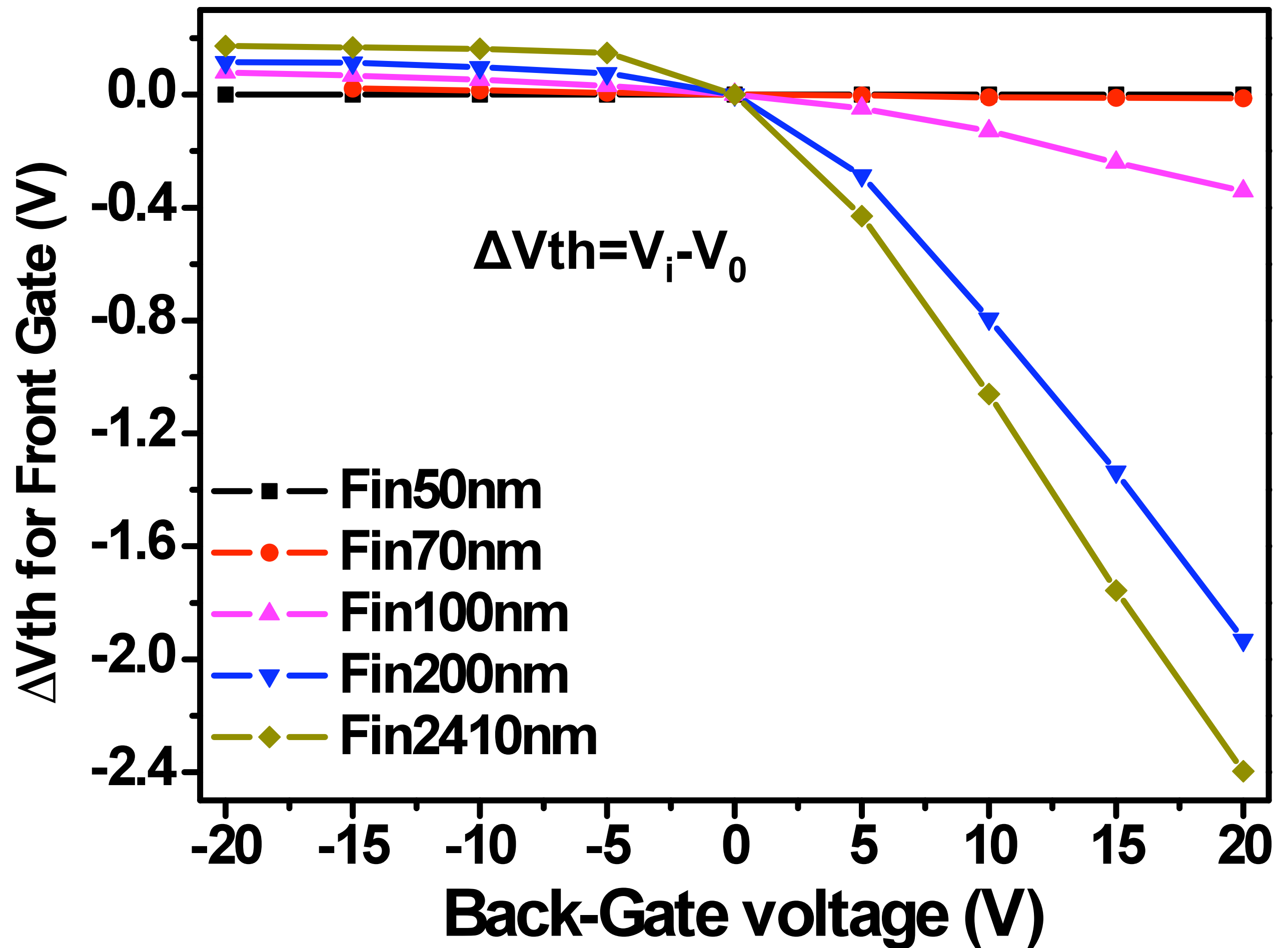
Fin width dependence of the coupling effect between front-gate & back-gate



V_i: Vth under applied back-gate bias

V_0: Vth with grounded back-gate bias

- For smaller fins, the applied side-gate bias reduces the front to back gate coupling, as well as GIFBE.
- Significant to consider for device scaling.

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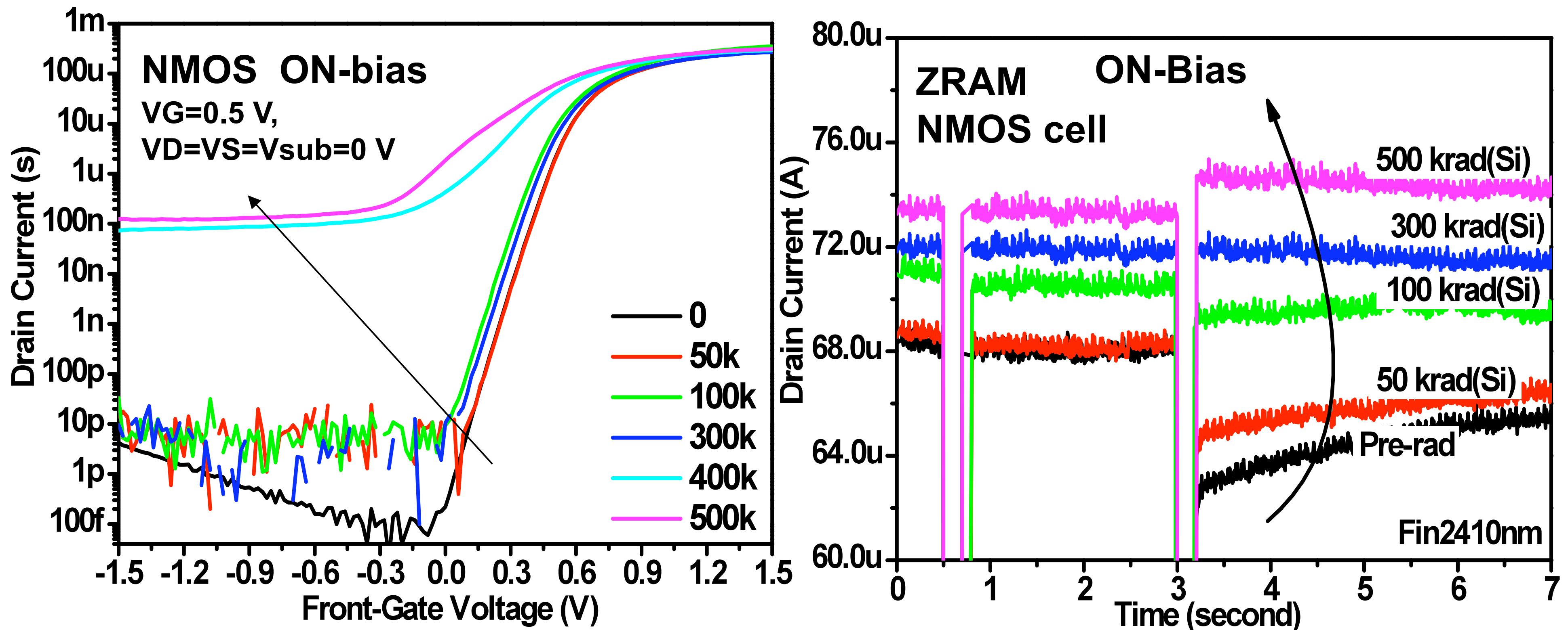
First look: Radiation effects on nMOS ZRAMs



- Current increase with TID is due to back gate leakage
- ZRAM retention disappears with large back gate leakage

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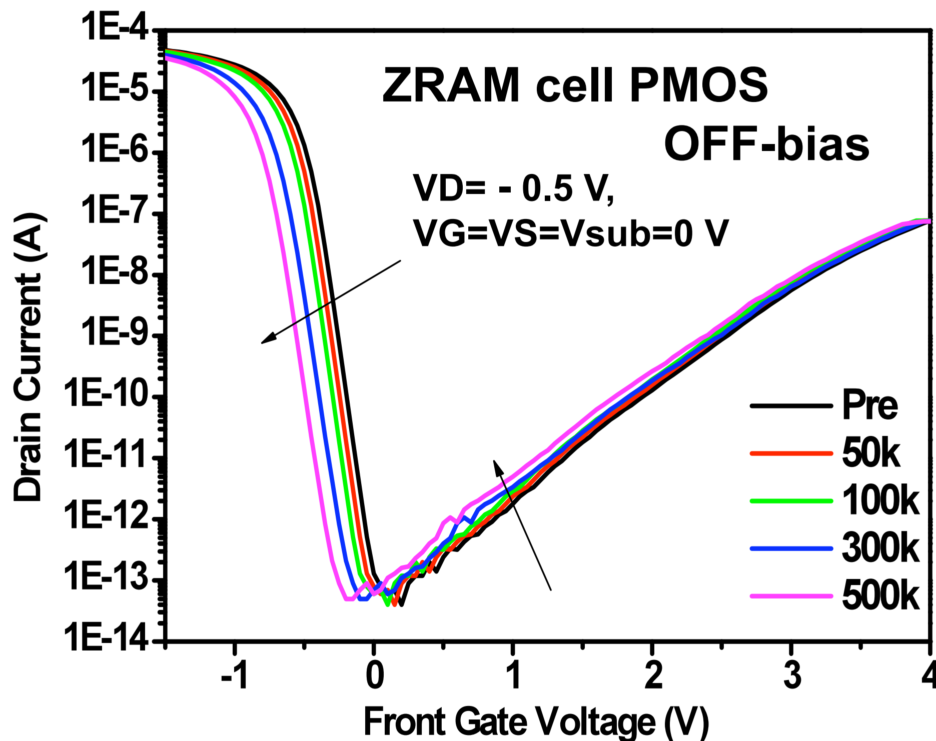
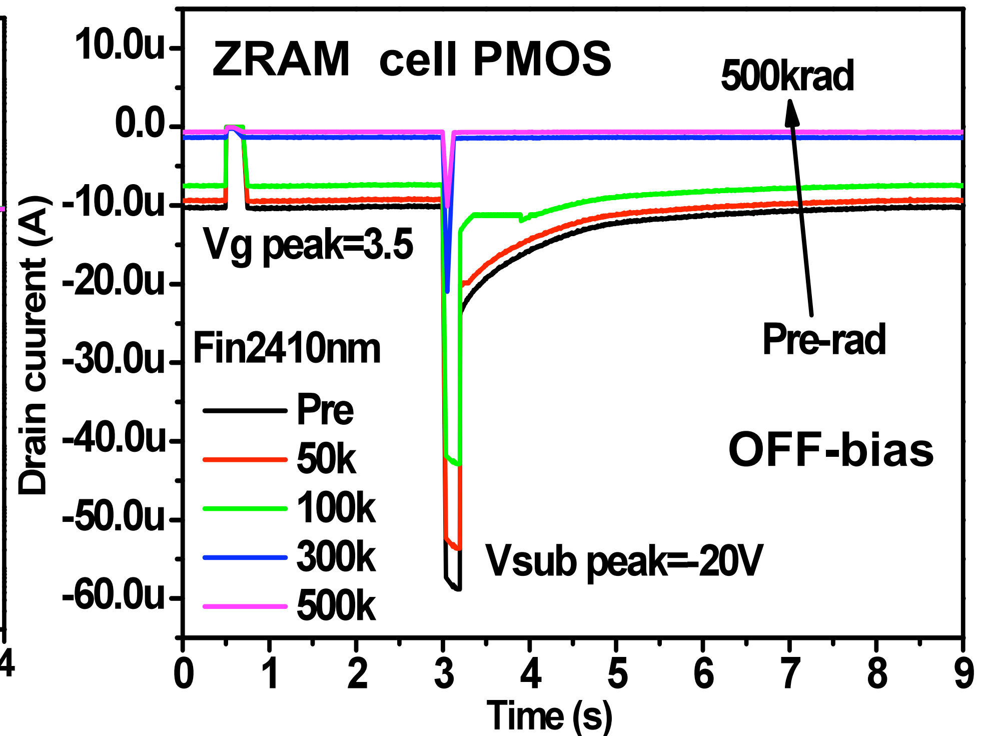
First look: Radiation effects on pMOS ZRAMs





- ZRAM retention decreases with increasing TID for these irradiation and programming/readout conditions
- Loss of retention probably due to BG V_{th} shifts in the BOX. If so, may require adjustment to BG pulse voltage in radiation environment.

Conclusions

- **ZRAM retention increases with fin width due to increased gate-induced floating body effects.**
- **For these devices and programming conditions, memory retention is superior for pMOS than nMOS.**
  - **Stored electrons in body more stable than holes.**
  - **Results may vary for other technologies.**
- **ZRAM retention may be quite sensitive to total-dose irradiation (at least for high doses).**
  - **Characterization of other kinds of devices is planned.**

Thanks