Layout-related stress effects on TID-induced leakage current

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Introduction

• Mechanical stress plays an important role in process modeling

• It controls the structural integrity of the device; the mobility of charged carriers and leakage currents are changed by stresses

• STI-induced mechanical stress increases with the reduction of the device active area. Many processing steps contribute to STI stress:
  – Liner oxidation, (HDP) oxide deposition, thermal oxidation processes after STI formation...

While the implication of stress on device performance is well established before irradiation, the effects of stress on the TID response are not fully understood
Types and sources of stress for NMOS and PMOS

- NMOS and PMOS have different desired stress in different directions
- Stress generated due to thermal or lattice mismatch

- Main sources of stress:
  1. Shallow trench isolation
  2. Embedded SiGe (PMOS)
  3. Dual-stress nitride liner

V. Joshi et al “Stress Aware Layout Optimization” ISPD-08, ACM 978-1-60558-048, April 2008
Dependence of channel stress on layout

- Amount of stress transferred to the channel has a strong dependence on layout:
  - Longer active space (higher SA), STI pushed away from the channel

- Two devices with same W, L can differ significantly in performance

The purpose of this work is to study the STI-stress effect on TID induced leakage current

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Active space distance effect on Device Parameters

Test structures used are:
- 90 nm commercial bulk CMOS using STI
- Symmetric NMOS transistors with different SA (varying from 0.24 µm to 2 µm).

This layout dependence is known as STI stress effect.

The STI stress effect is higher when SA decreases.
Stress Effects on Doping

For smaller SA, compressive stress originating in the STI edge results in:

- Higher doping at the channel edges, (along “Cutline X”) increasing $V_{th}$
- Higher doping at the STI sidewall, (along “Cutline Y”) decreasing $I_{off}$
SA effect on TID induced leakage current

- TID-induced leakage current increases with increasing SA.
- TID-induced leakage current is smaller for smaller SA.
- The sidewall doping concentration is higher in devices with smaller SA due to the impurity diffusion in the channel region and at the STI sidewall.
**Channel width effect on TID induced leakage current**

Strong dependence on channel width: with the narrow devices exhibiting less leakage pre-rad, but more post-rad.
Channel width effect on TID induced leakage current

The on-state current does not change after irradiation, only the off-state current changes.

Pre-rad

![Graph showing Drain current vs. Gate voltage for different channel widths before irradiation.]

Post-rad

![Graph showing Drain current vs. Gate voltage for different channel widths after irradiation.]

- W=0.12 um
- W=0.9 um
- W=10 um

Pre-rad

- L=0.08um
- Vd=1.2V

Post-rad (500 Krad)

- L=0.08um
- Vd=1.2V
Possible Mechanisms of TID Dependence on Channel Width

- **Doping profile at the STI sidewall**
  - The compressive stress dependence on the space between adjacent STI edges \(^1\)
  - Doping profile differences at the device edges (The diffusion can be affected by local strain, which varies with width)

- **The enhanced radiation sensitivity for narrow devices may be related to the influence of stress in the STI oxide on the amount of positive trapped charge**
  - The amount of radiation-induced positive charge trapped in oxides has been shown to depend on the stress in the oxide \(^2,3\)

- **Fringing electric field may be higher at the STI edges for narrower width devices**

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\(^1\) M. Miyamoto et al. TNS, Mar 2004
\(^2\) H. Park et al. IEDM, Dec. 2008
\(^3\) K. Kasama et al. TNS, Dec. 1986
Mechanical stress extraction using measured $I_{d\,(sub)}$

\[
I_{d\,(sub)} \propto n_i^2 \propto \exp\left(-\frac{E_g}{K T}\right) \\
\Delta E_g = \Delta E_c - \Delta E_v = -4.39 \times 10^{-11} \times \sigma
\]

\[
\sigma = \ln\left(\frac{I_d(SA = 2\,\mu m)}{4.39 \times 10^{-11}}\right) \times KT
\]

C. Hsieh et al. TNS, Mar 2008
D. Kim et al. “Influence of Dummy Active Patterns on Mechanical Stress Induced by Spin-On-Glass-Filled STI in n-MOSFETs.”
Mechanical stress extraction using measured $I_{d\text{ (sub)}}$

$$I_{d\text{ (sub)}} \propto n_i^2 \propto \exp\left(-\frac{E_g}{KT}\right)$$

$$\Delta E_g = \Delta E_c - \Delta E_v = -4.39 \times 10^{-11} \times \sigma$$

$$\sigma = \ln\left(\frac{I_d}{I_d(W = 10 \mu m)}\right) \times KT \frac{4.39 \times 10^{-11}}{4.39 \times 10^{-11}}$$

C. Hsieh et al. TNS, Mar 2008
D. Kim et al. “Influence of Dummy Active Patterns an Mechanical Stress Induced by Spin-On-Glass-Filled STI in n-MOSFETs.”
Conclusion

- TID-induced leakage current increase with increasing active-to-isolation spacing

- Mechanical stress reduces impurity diffusion in the channel region, affecting the TID sensitivity

- The enhanced radiation sensitivity for narrow devices may be related to the influence of stress in the STI oxide on the amount of positive trapped charge

**Future work:**

- Estimate the amount of stress at the STI sidewall for different SA spacing and channel width using process simulations