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Layout-related stress effects on TID-induced leakage current

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Outline

- **Introduction**
  - Types and sources of stress for NMOS and PMOS
  - Dependence of channel stress on layout
- **Active space (SA) distance effect on TID induced leakage current**
  - Pre-irradiation V_{th} and I_{off} vs. SA
  - Post-irradiation I_{off} vs. SA
- **Channel width effect on TID induced leakage current**
- **Mechanical stress extraction using measured $I_{d\ (sub)}$**
- **Conclusion**

Introduction

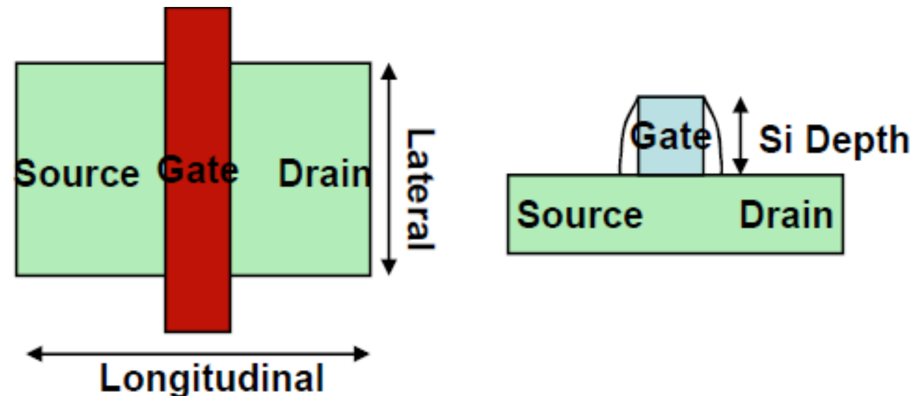
- Mechanical stress plays an important role in process modeling
- It controls the structural integrity of the device; the mobility of charged carriers and leakage currents are changed by stresses
- STI-induced mechanical stress increases with the reduction of the device active area. Many processing steps contribute to STI stress :
  - Liner oxidation, (HDP) oxide deposition, thermal oxidation processes after STI formation...

While the implication of stress on device performance is well established before irradiation, the effects of stress on the TID response are not fully understood

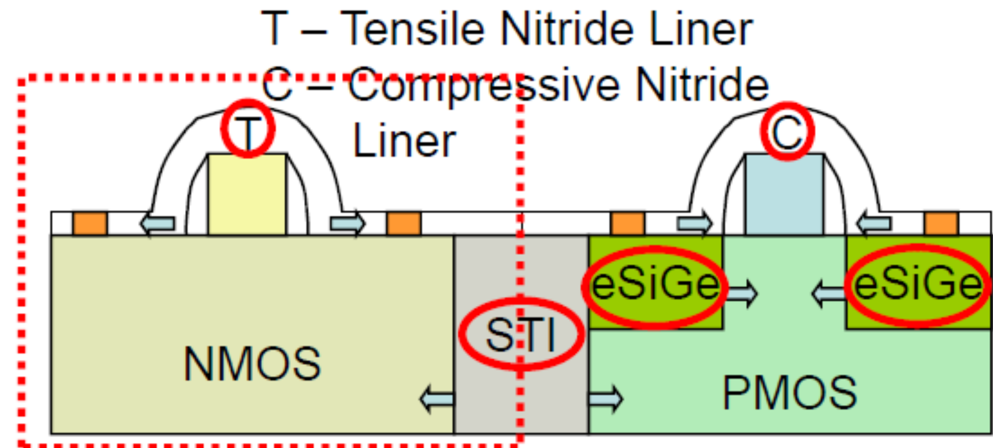
Types and sources of stress for NMOS and PMOS

- NMOS and PMOS have different desired stress in different directions

- Stress generated due to thermal or lattice mismatch



- **Main sources of stress:**
  1. Shallow trench isolation
  2. Embedded SiGe (PMOS)
  3. Dual-stress nitride liner

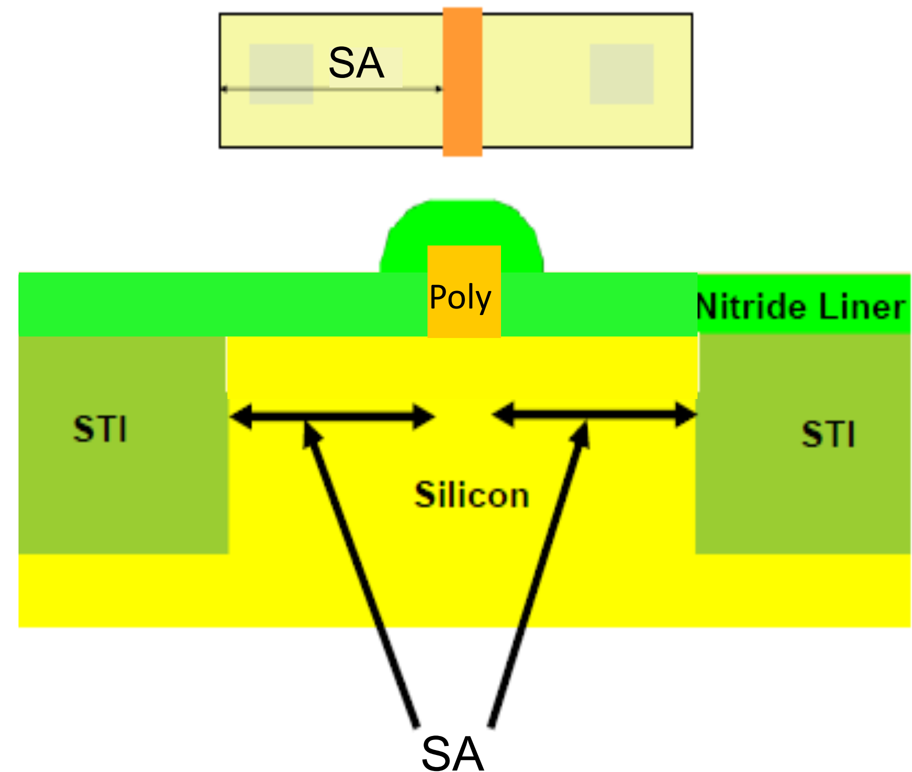


V. Joshi et al "Stress Aware Layout Optimization" ISPD-08, ACM 978-1-60558-048, April 2008

Dependence of channel stress on layout

- **Amount of stress transferred to the channel has a strong dependence on layout:**
  - Longer active space (higher SA), STI pushed away from the channel

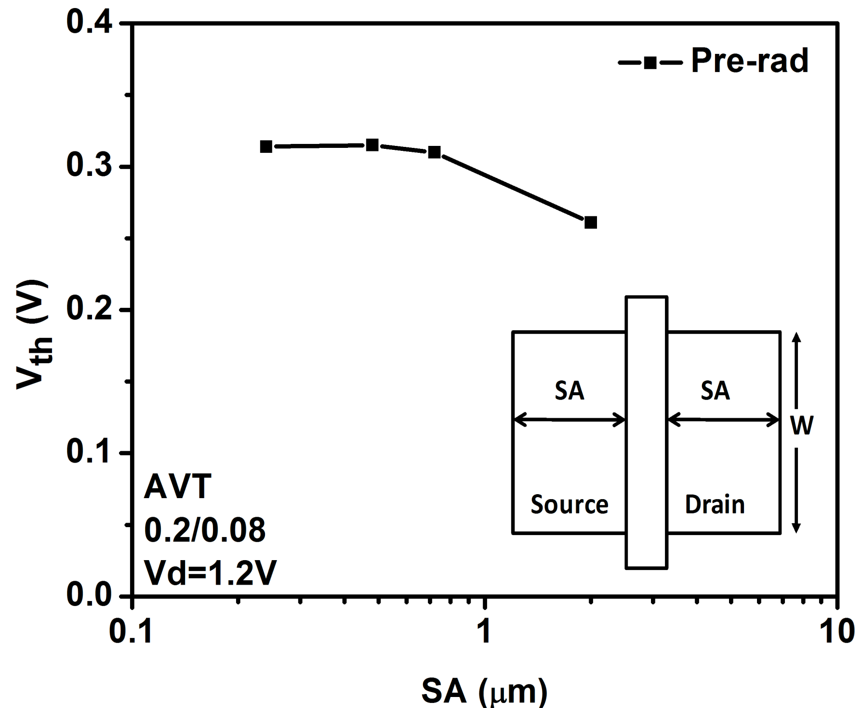
- **Two devices with same W, L can differ significantly in performance**

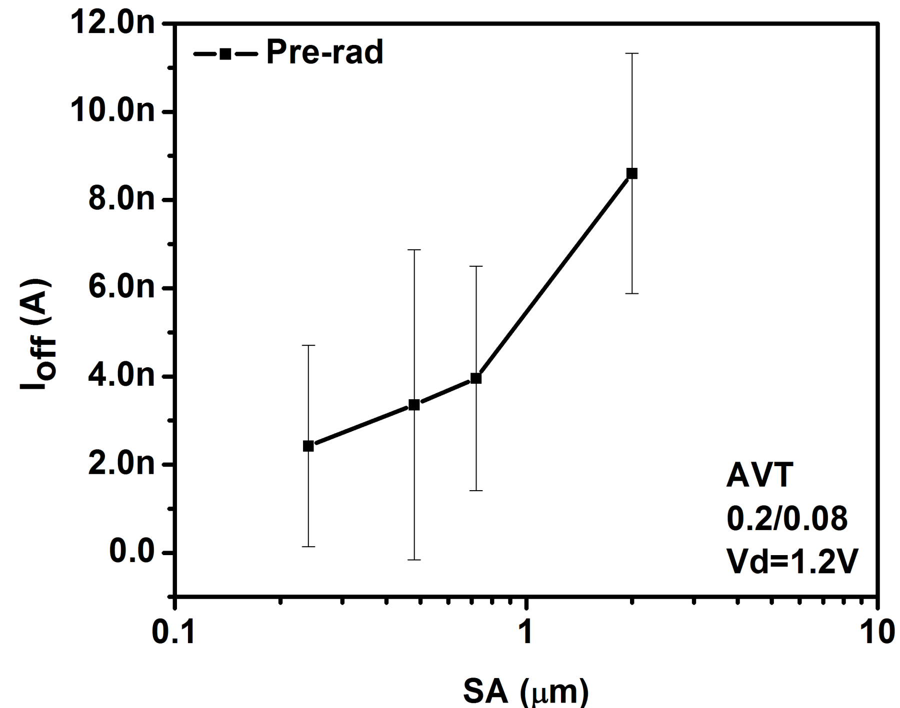


The purpose of this work is to study the STI-stress effect on TID induced leakage current

V. Joshi et al "Stress Aware Layout Optimization" ISPD-08, ACM 978-1-60558-048, April 2008

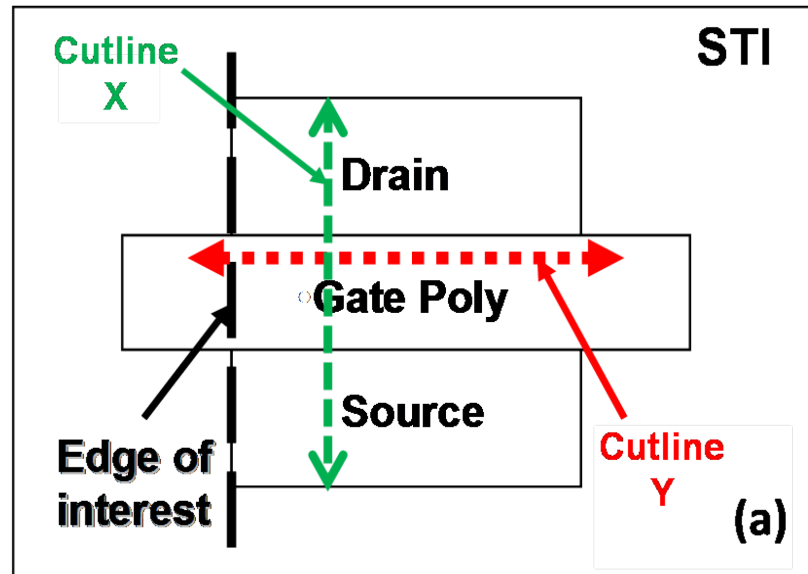
Active space distance effect on Device Parameters



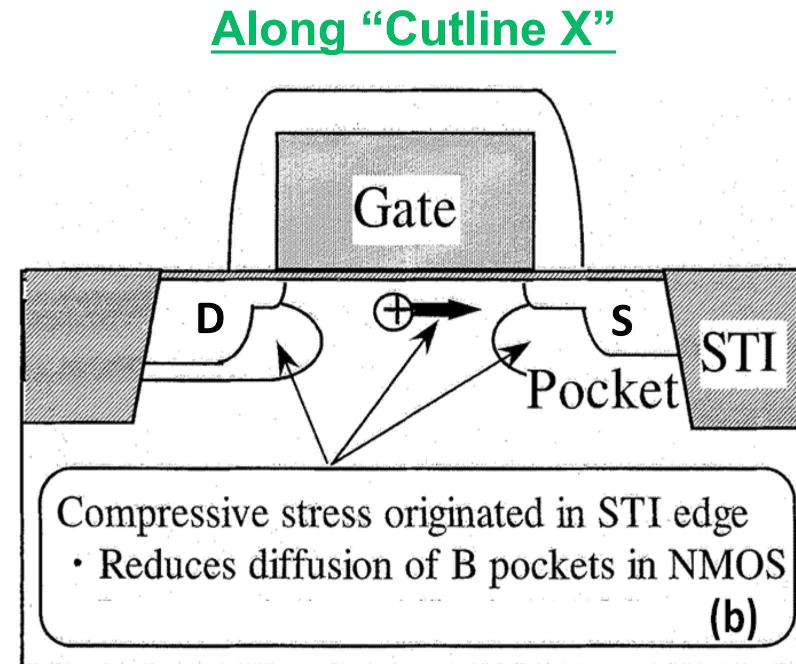


- **Test structures used are :**
  - 90 nm commercial bulk CMOS using STI
  - Symmetric NMOS transistors with different SA (varying from 0.24µm to 2µm).
- This layout dependence is known as STI stress effect
- The STI stress effect is higher when SA decreases

Stress Effects on Doping



Along "Cutline X"



For smaller SA, compressive stress originating in the STI edge results in:

- Higher doping at the channel edges, (along "Cutline X") increasing V_{th}
- Higher doping at the STI sidewall, (along "Cutline Y") decreasing I_{off}

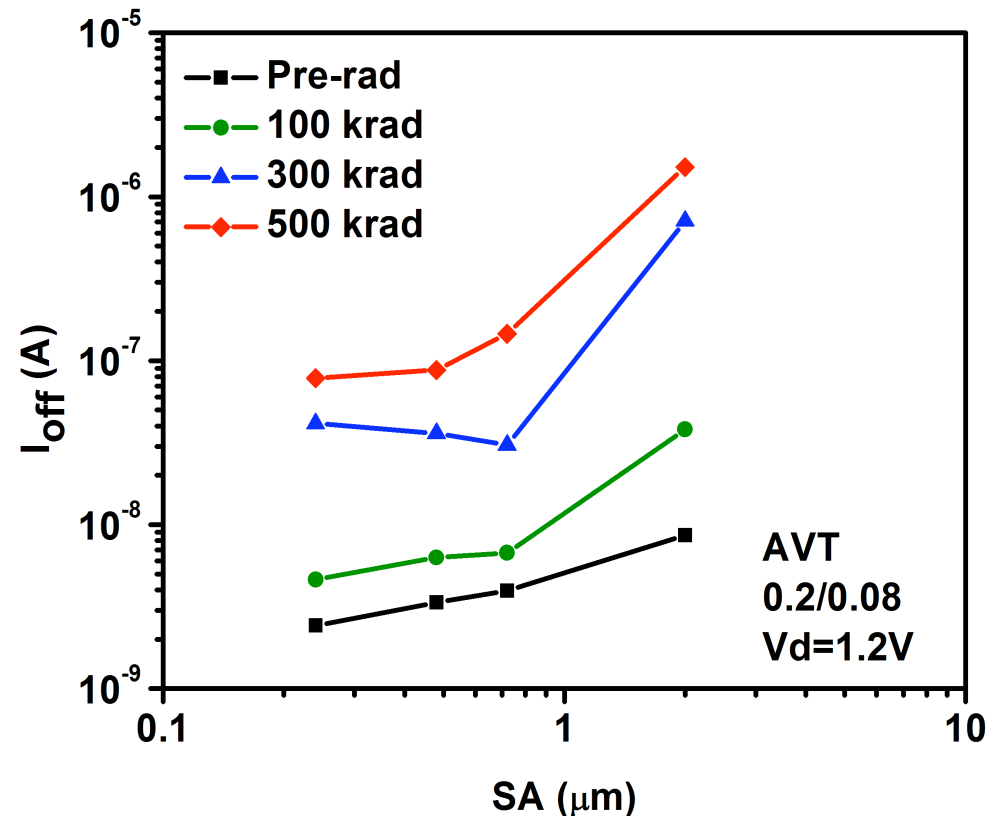
M. Miyamoto et al "Impact of Reducing STI-Induced Stress on Layout Dependence of MOSFET Characteristics" TNS, March 2004

SA effect on TID induced leakage current

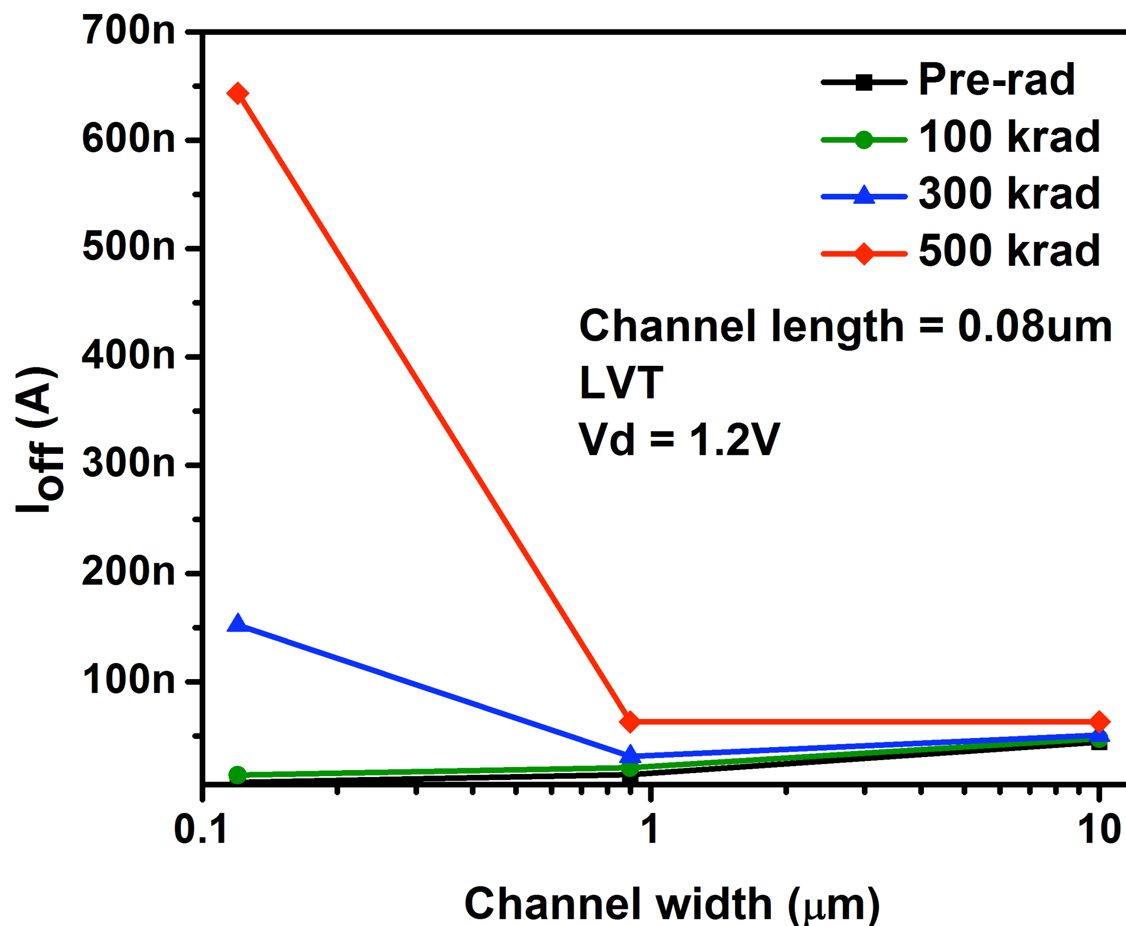
- TID-induced leakage current increases with increasing SA

- TID-induced leakage current is smaller for smaller SA.

- The sidewall doping concentration is higher in devices with smaller SA due to the impurity diffusion in the channel region and at the STI sidewall.

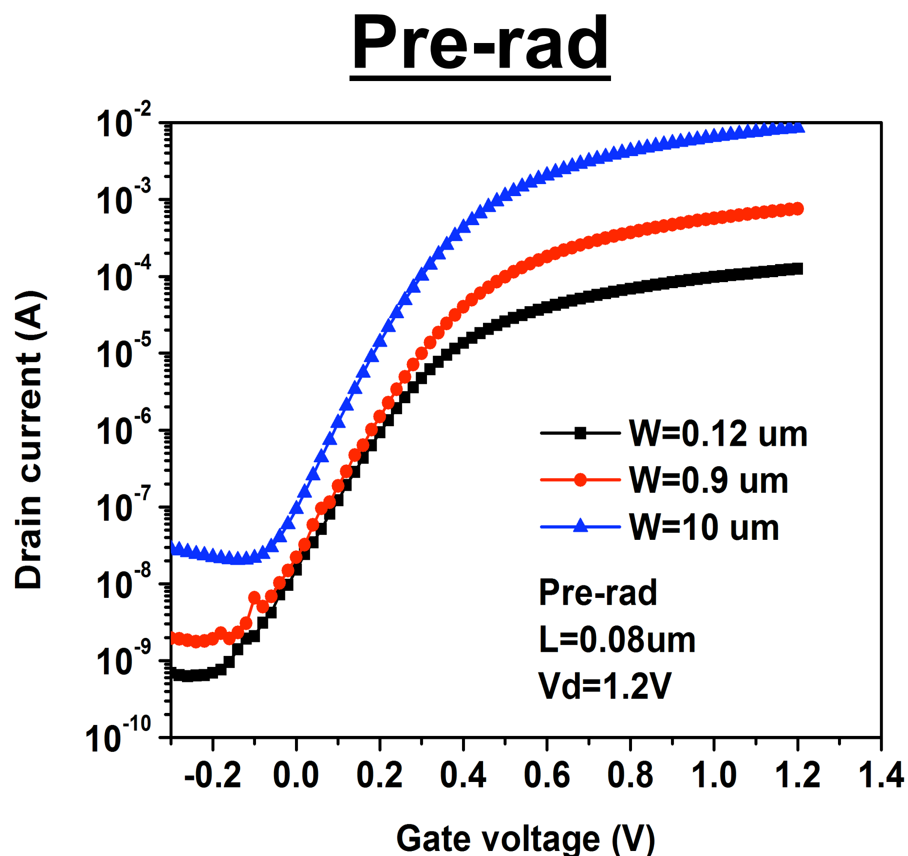


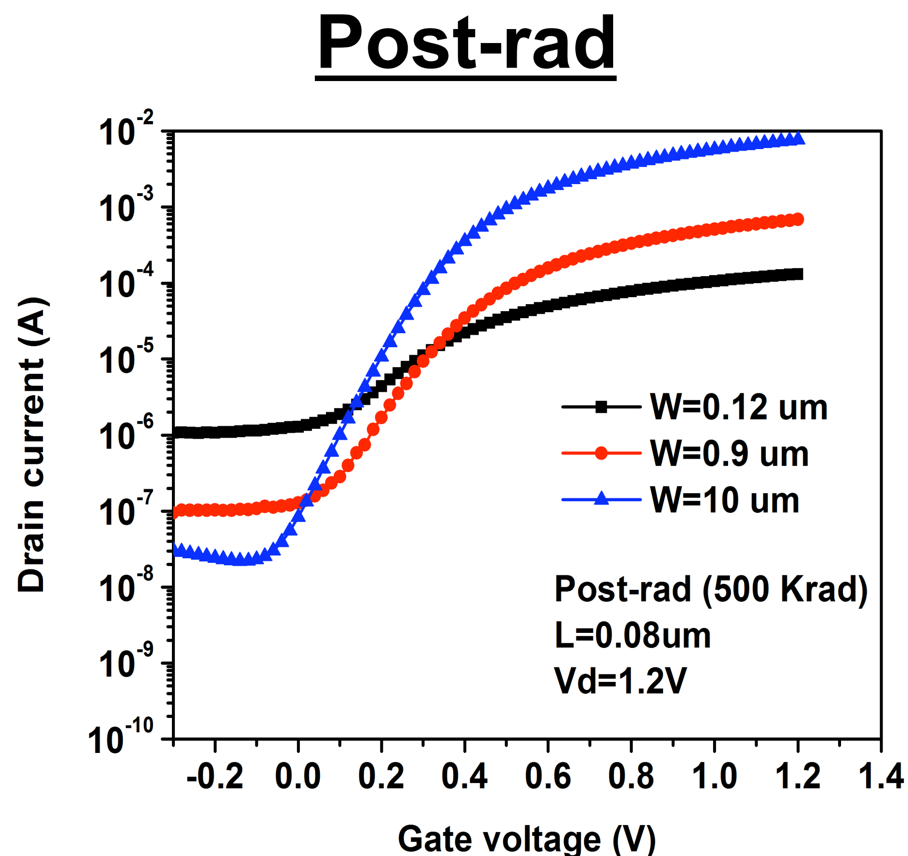
Channel width effect on TID induced leakage current



Strong dependence on channel width: with the narrow devices exhibiting less leakage pre-rad, but more post-rad

Channel width effect on TID induced leakage current

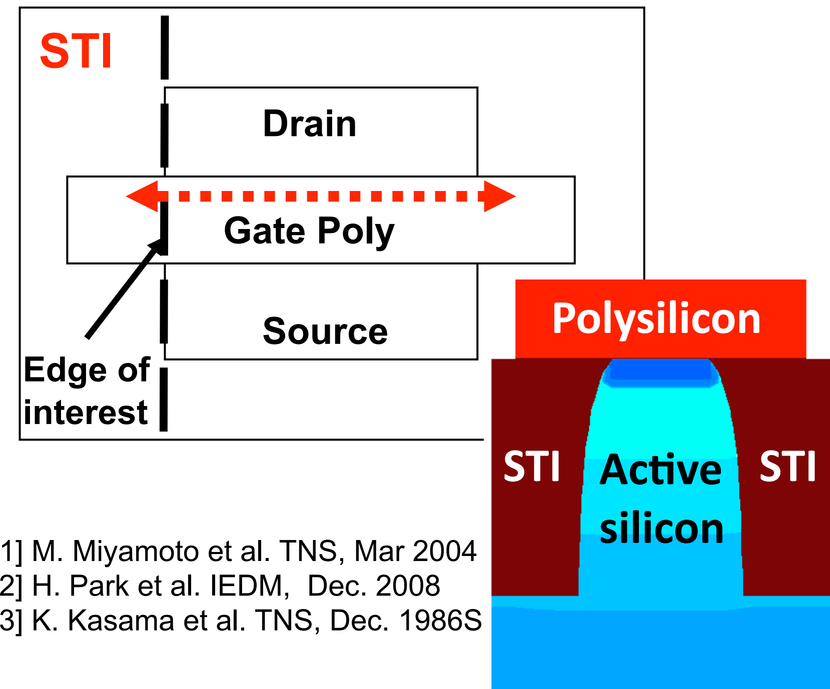




The on-state current does not change after irradiation, only the off-state current changes

Possible Mechanisms of TID Dependence on Channel Width

- **Doping profile at the STI sidewall**
  - The compressive stress dependence on the space between adjacent STI edges [1]
  - Doping profile differences at the device edges (The diffusion can be affected by local strain, which varies with width)



[1] M. Miyamoto et al. TNS, Mar 2004
[2] H. Park et al. IEDM, Dec. 2008
[3] K. Kasama et al. TNS, Dec. 1986S

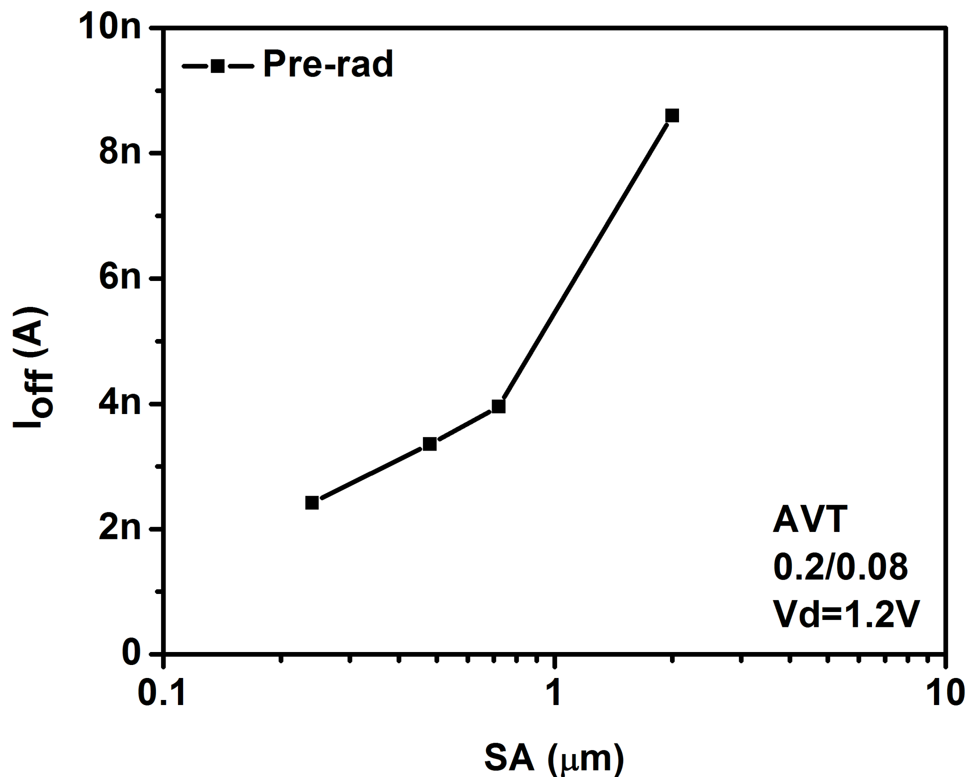
- **The enhanced radiation sensitivity for narrow devices may be related to the influence of stress in the STI oxide on the amount of positive trapped charge**
  - The amount of radiation-induced positive charge trapped in oxides has been shown to depend on the stress in the oxide [2,3]
- **Fringing electric field may be higher at the STI edges for narrower width devices**

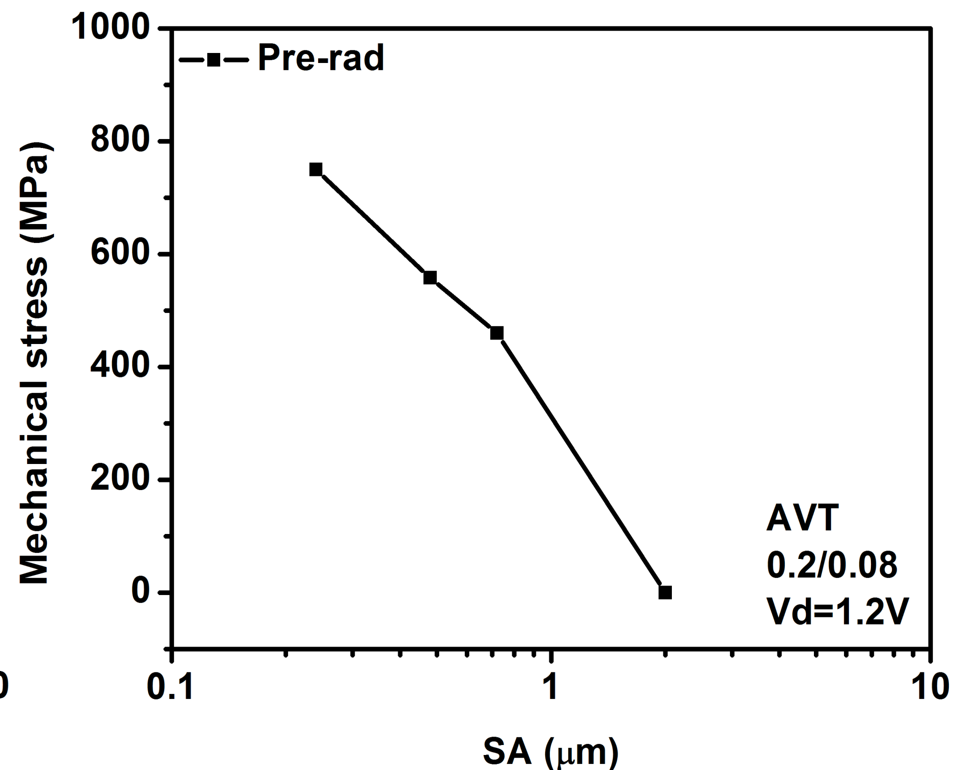
Mechanical stress extraction using measured $I_{d\,(sub)}$

$$I_{d(sub)} \propto n_i^2 \propto \exp(-\frac{E_g}{KT})$$

$$\Delta E_g = \Delta E_c - \Delta E_v = -4.39\times10^{-11}\times\sigma$$

$$\sigma = \frac{\ln(\frac{I_d}{I_d(SA=2\mu m)})\times KT}{4.39\times10^{-11}}$$





C. Hsieh et al. TNS, Mar 2008

D. Kim et al. “Influence of Dummy Active Patterns an Mechanical Stress Induced by Spin-On-Glass-Filled STI in n-MOSFETs.”

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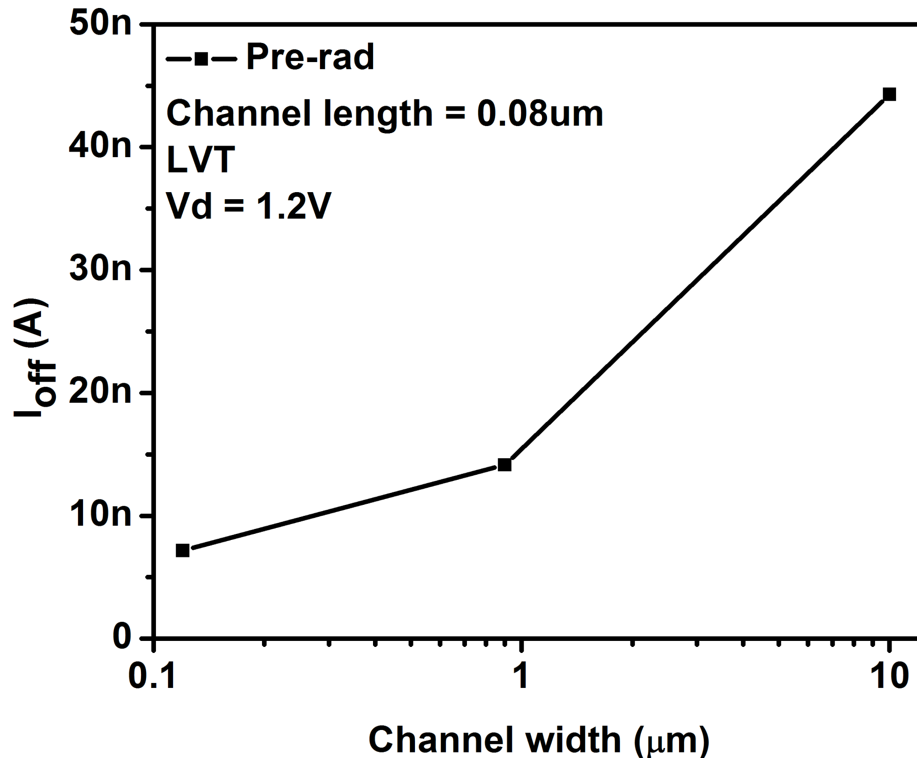

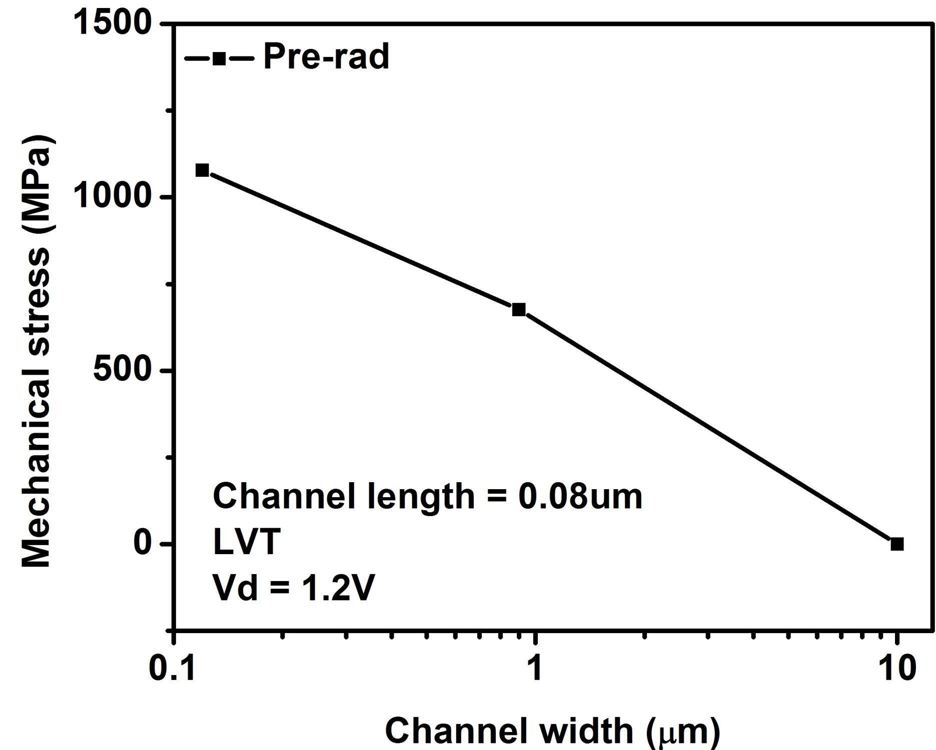

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Conclusion

- TID-induced leakage current increase with increasing active-to-isolation spacing
- Mechanical stress reduces impurity diffusion in the channel region, affecting the TID sensitivity
- The enhanced radiation sensitivity for narrow devices may be related to the influence of stress in the STI oxide on the amount of positive trapped charge

Future work:

- Estimate the amount of stress a the STI sidewall for different SA spacing and channel width using process simulations