The Effects of STI Topology and Sidewall Doping on TID-induced leakage current

Nadia Rezzak, M.Alles, R.Schrimpf

Radiation Effects Group

Vanderbilt University, Nashville Tennessee, USA

MURI, June 11th, 2009

Outline

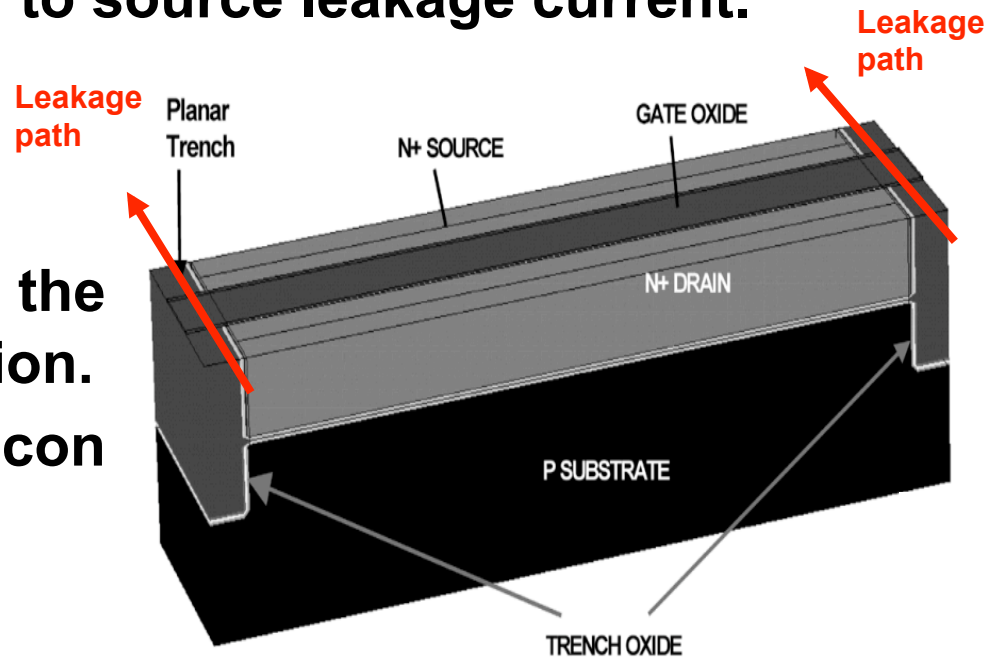
Vanderbilt Engineering

- Motivation
- Background
- STI topology 3D, and 2D views
- Effect of sidewall doping
- TID response vs. trench recess depth
- Summary

Motivation

Vanderbilt Engineering

- Thinner gate oxide shifted dominant TID effect to charge buildup in the STI.
  - dominant off state drain to source leakage current.



- <u>Key parameter:</u>
  - STI edge topology at the active to isolation transition.
  - Doping of the active silicon along the sidewall.

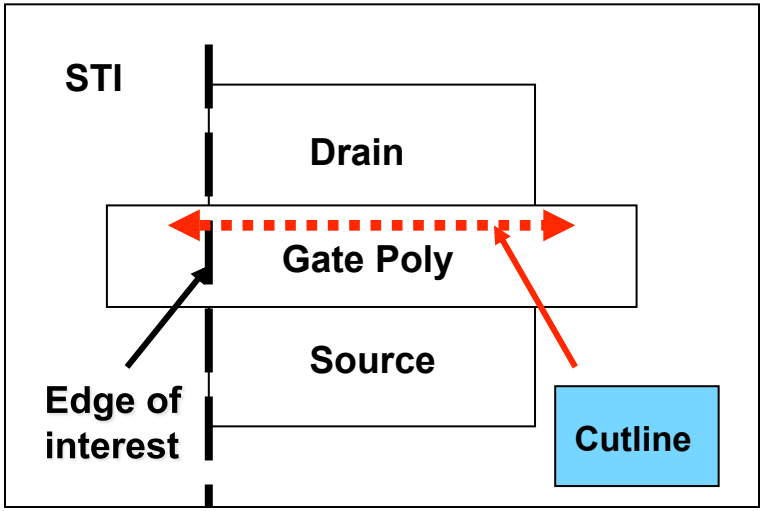
- Understand and quantify the sensitivity of TID response to STI profile, with varying sidewall doping, at the 90-nm CMOS node.

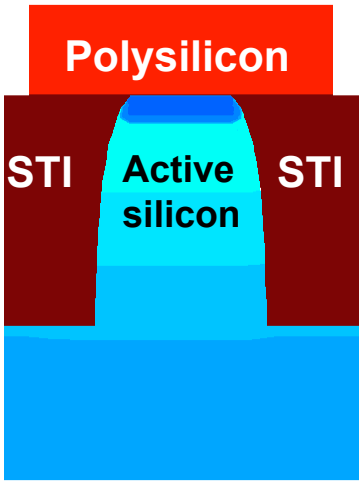
Motivation

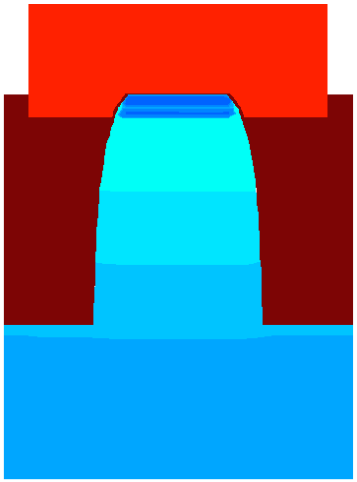
Vanderbilt Engineering

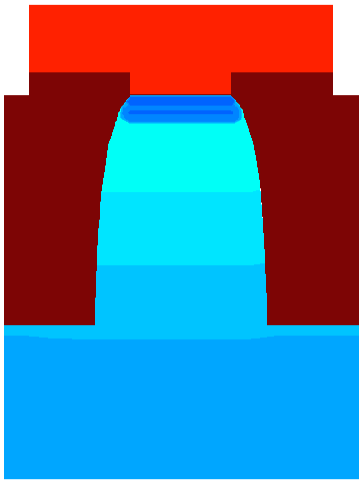
Methodology:

- Apply 3D TCAD simulations to study the effects of variation in the degree of STI trench recess on resulting TID response for a range of sidewall doping.









Planar trench

Recessed trench

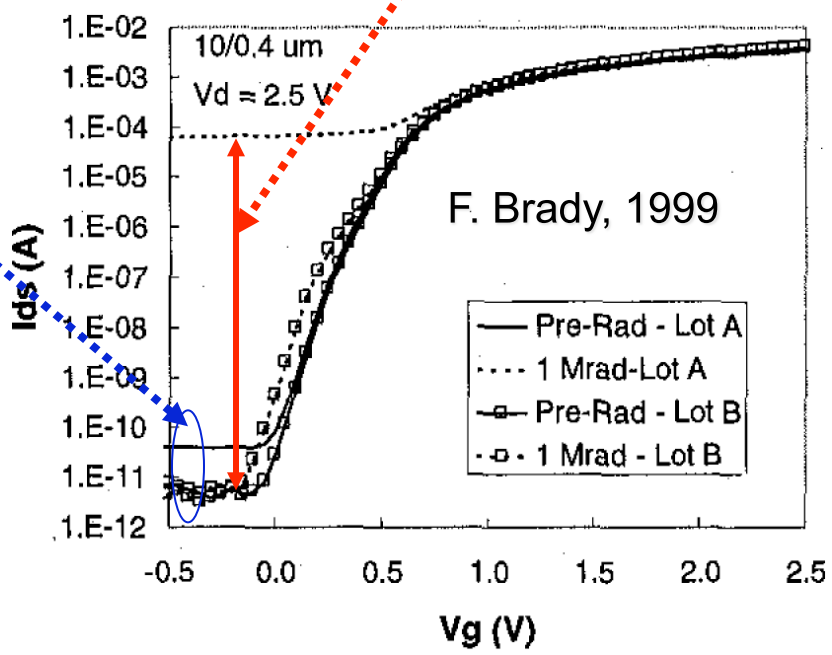
Overfilled trench

Background: STI Variability

- Unhardened, "identically" processed lots: Similar, acceptable pre-rad; much different hardness

Variation in:

- Oxide composition
- Edge topology

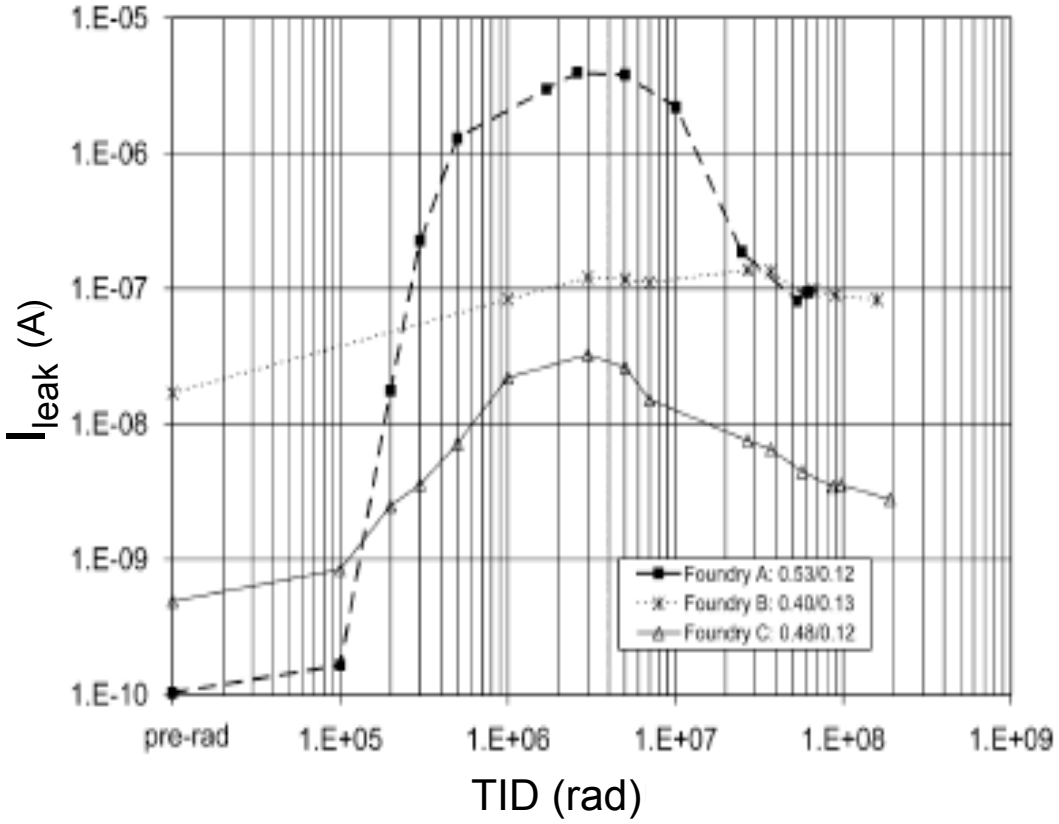


Significant consideration for use of commercial technologies in rad-hard applications

Background: TID response Variation

Vanderbilt Engineering

- TID response may vary from foundry to foundry [1].
- Amount of recess may vary across a wafer or from lot to lot.
- Process variants may affect TID response e.g., high performance vs. low power.



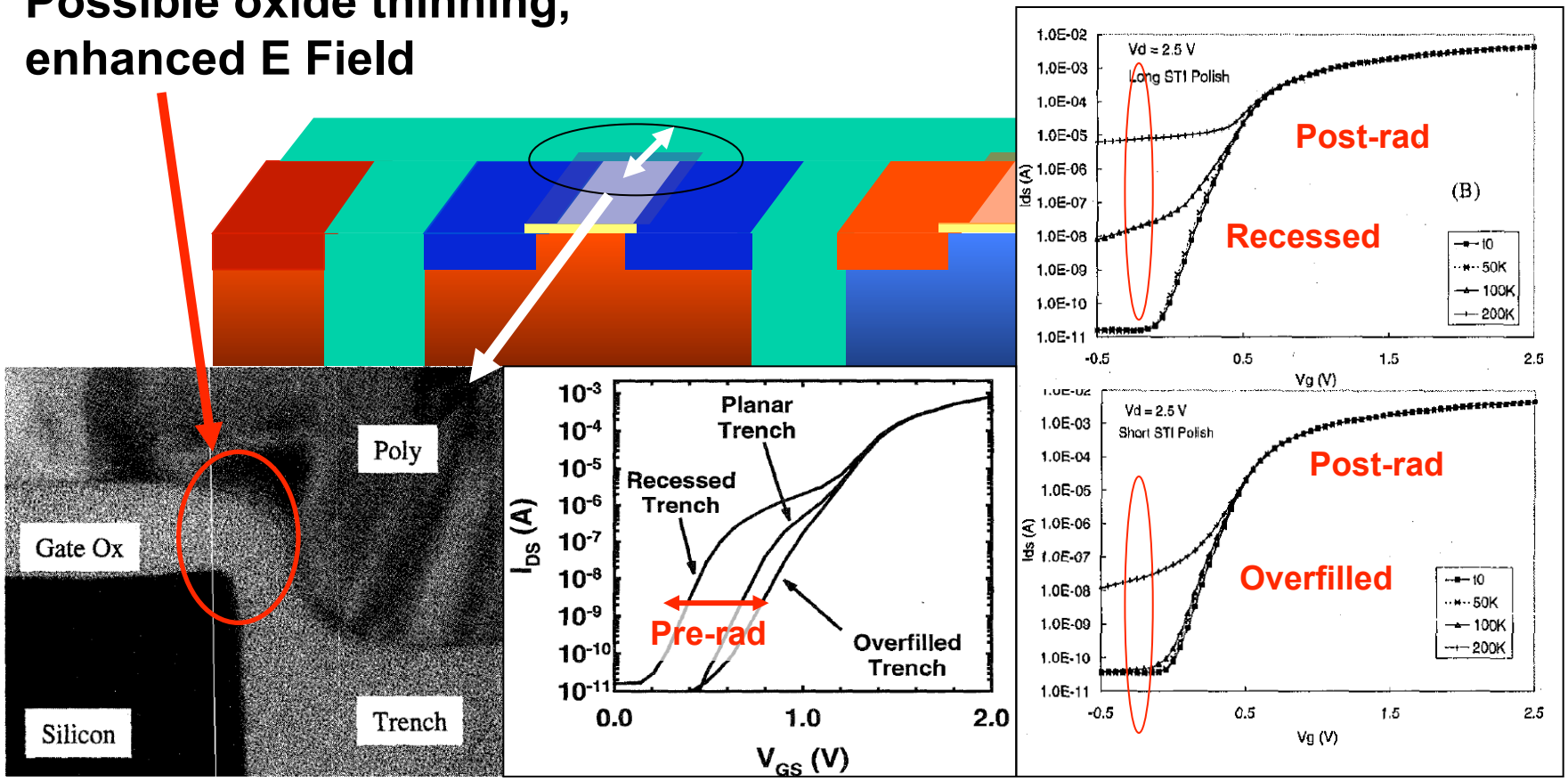
Leakage current evolution with TID of NMOS core transistor from each foundry [1].

[1]. Gonella, F. Faccio, M. Silvestri, S. Gerardin, D. Pantano, ." Nuclear Instruments and Methods in Physics Research A 582 (2007), pp.750-754.

Background: STI Edge Topology

Vanderbilt Engineering

Possible oxide thinning, enhanced E Field

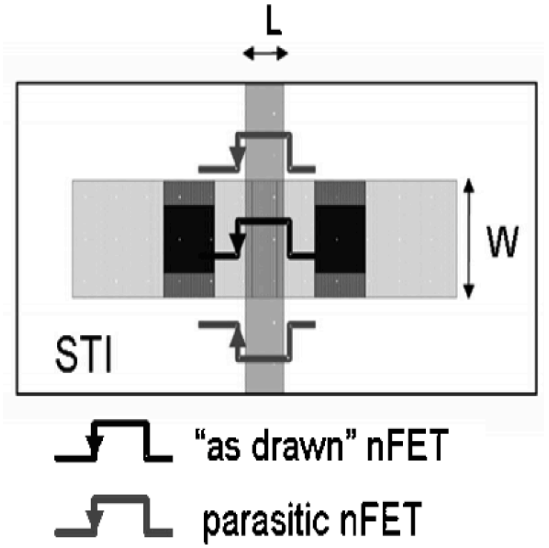


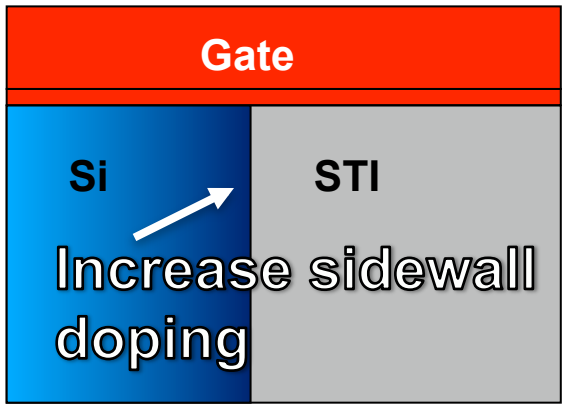
Topology of transition at gate edge important for leakage (including pre- and post-rad)

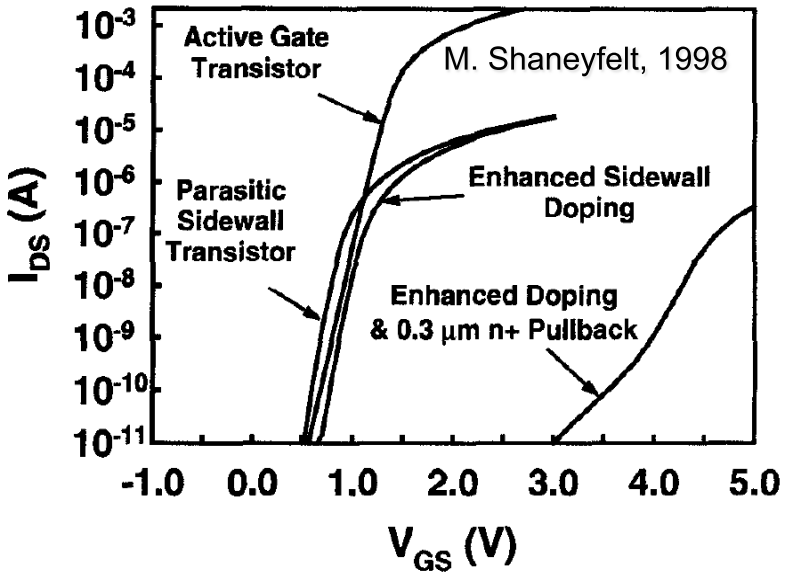
Background: Sidewall Doping

Vanderbilt Engineering

- The primary cause for off-state drain-to-source leakage is:
  - The reduction in the threshold voltage
  - The increase in current for the parasitic n-channel MOSFET associated with the edges of the "as drawn" device.
- Doping impacts leakage due to parasitic sidewall transistor.

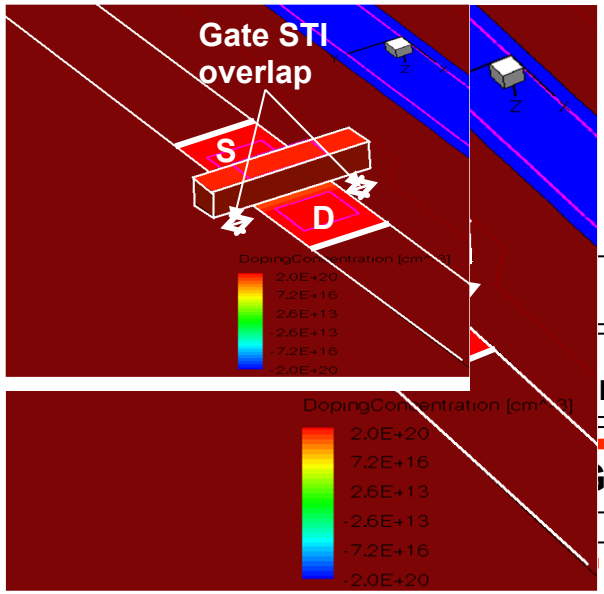






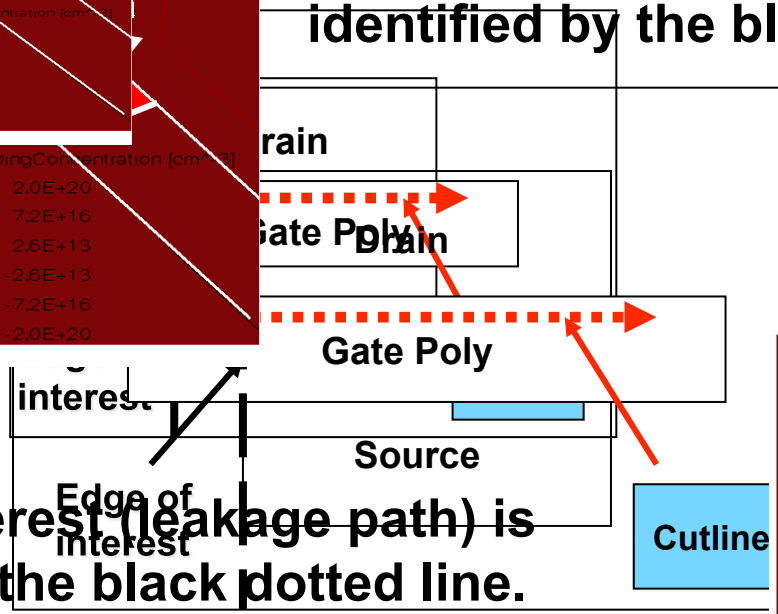
Edge leakage path

Vanderbilt Engineering



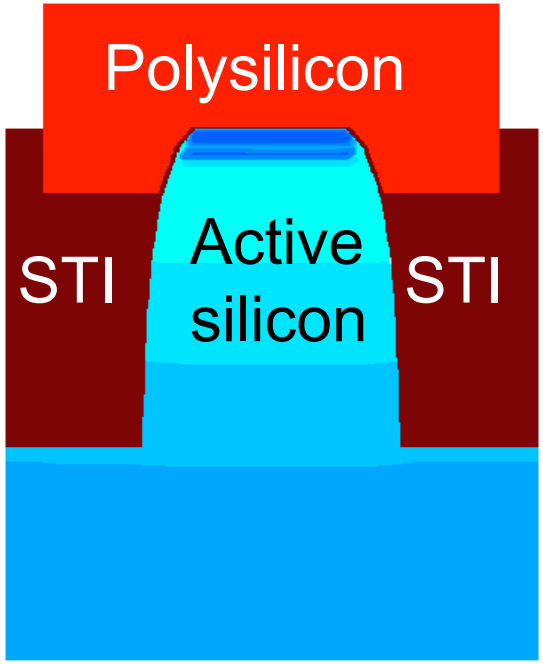
• 3D TCAD view of a 90-nm NMOS device with recessed trench.

• Edge of interest (leakage path) is identified by the black dotted line.



• Edge of interest (leakage path) is identified by the black dotted line.

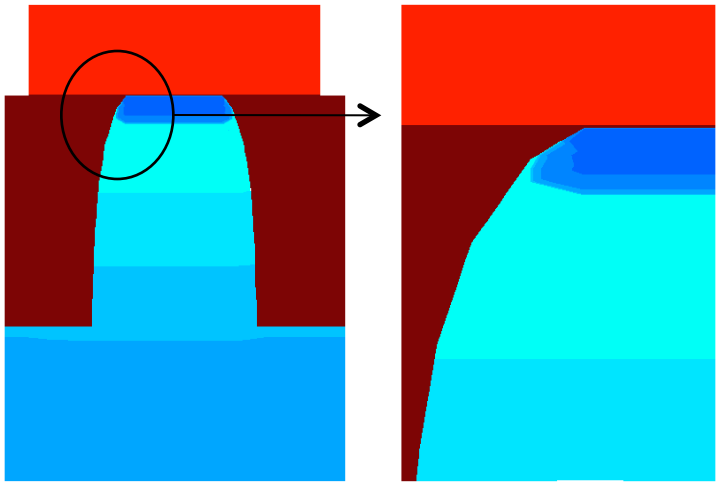
•The red dotted line will serve as the cut-line for future figures.



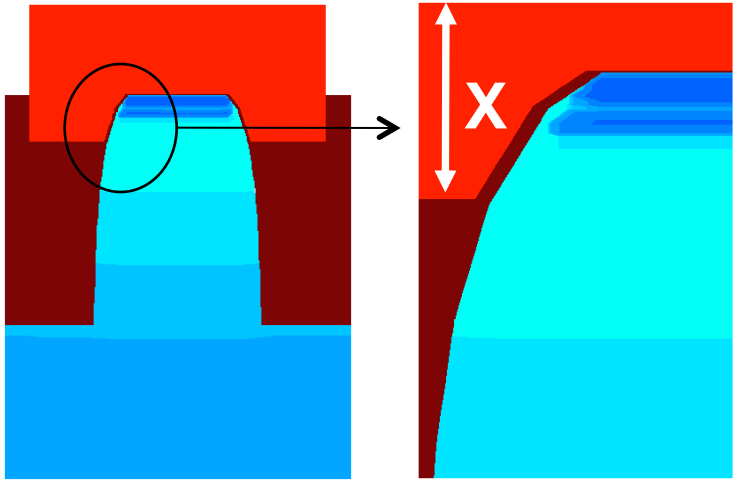
Planar vs. Recessed trench

Vanderbilt Engineering

- Planar geometry with chamfered (angled) edges to depict the silicon/oxide interface at the sidewall.

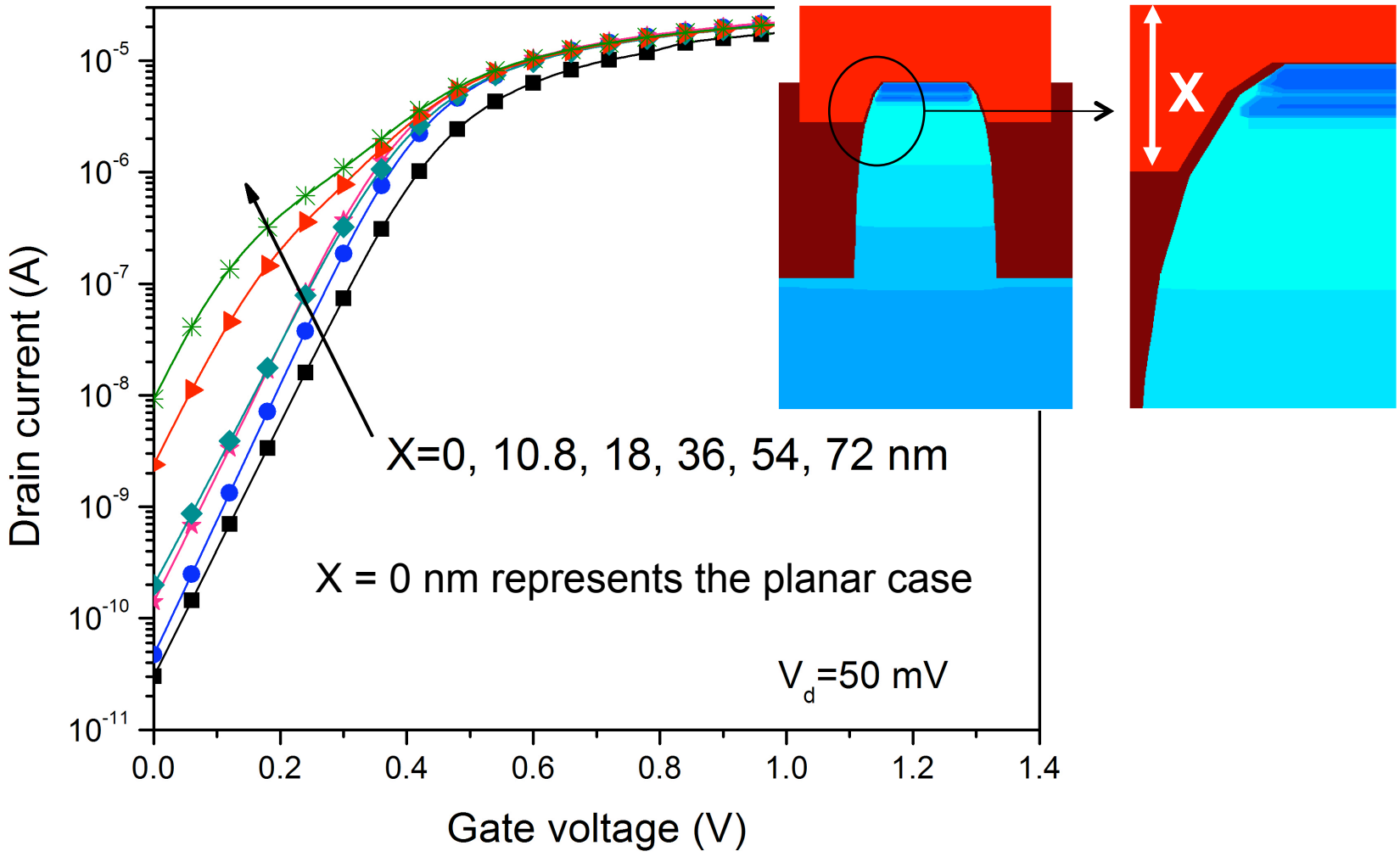


- Trench recessed by X = 72 nm with oxide thinning at the sidewall corner.



Pre-Rad: Trench Recess Depth

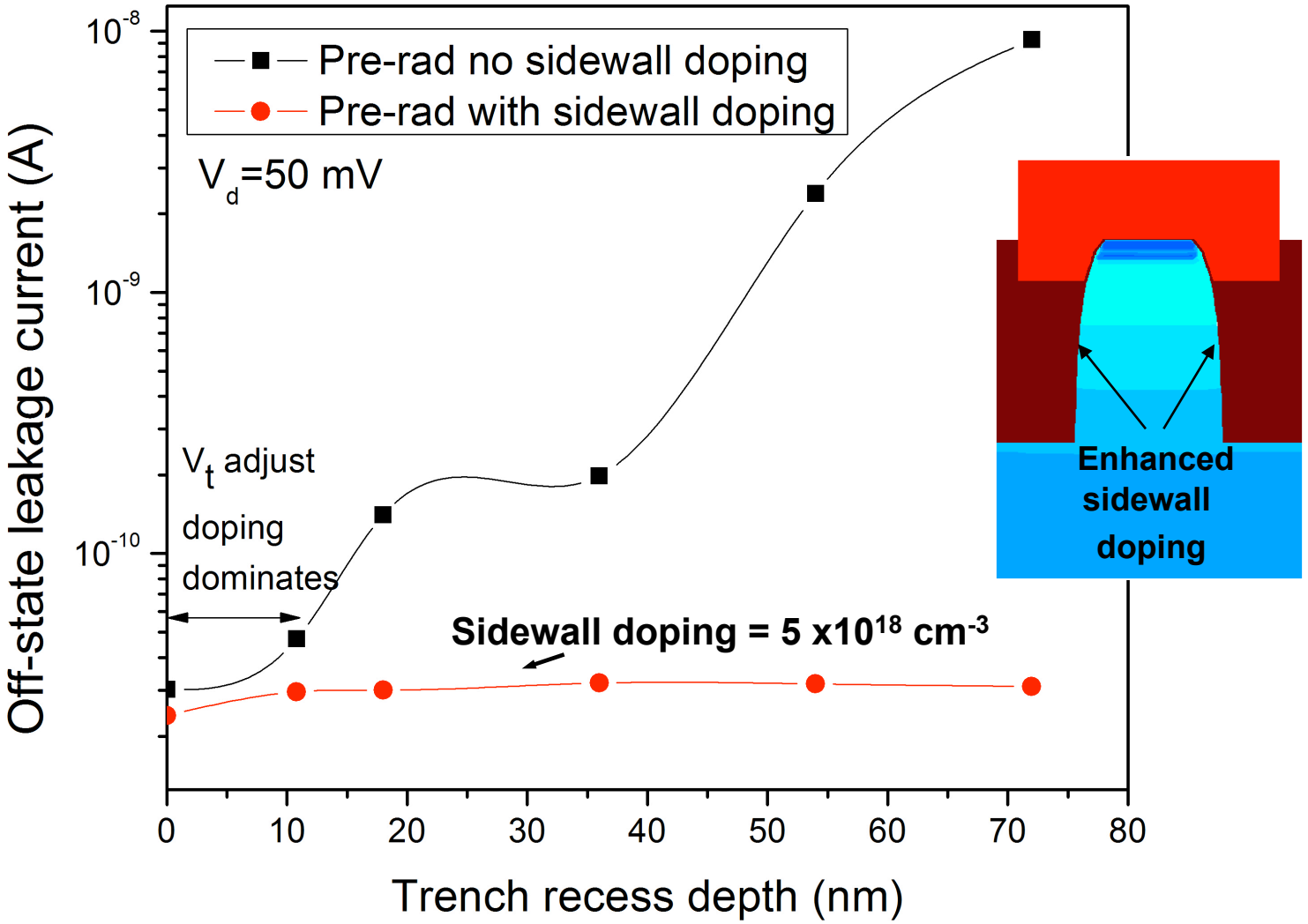
Vanderbilt Engineering



Pre-rad leakage increases with increasing recess (as expected)

Pre-Rad: Sidewall Doping

Vanderbilt Engineering

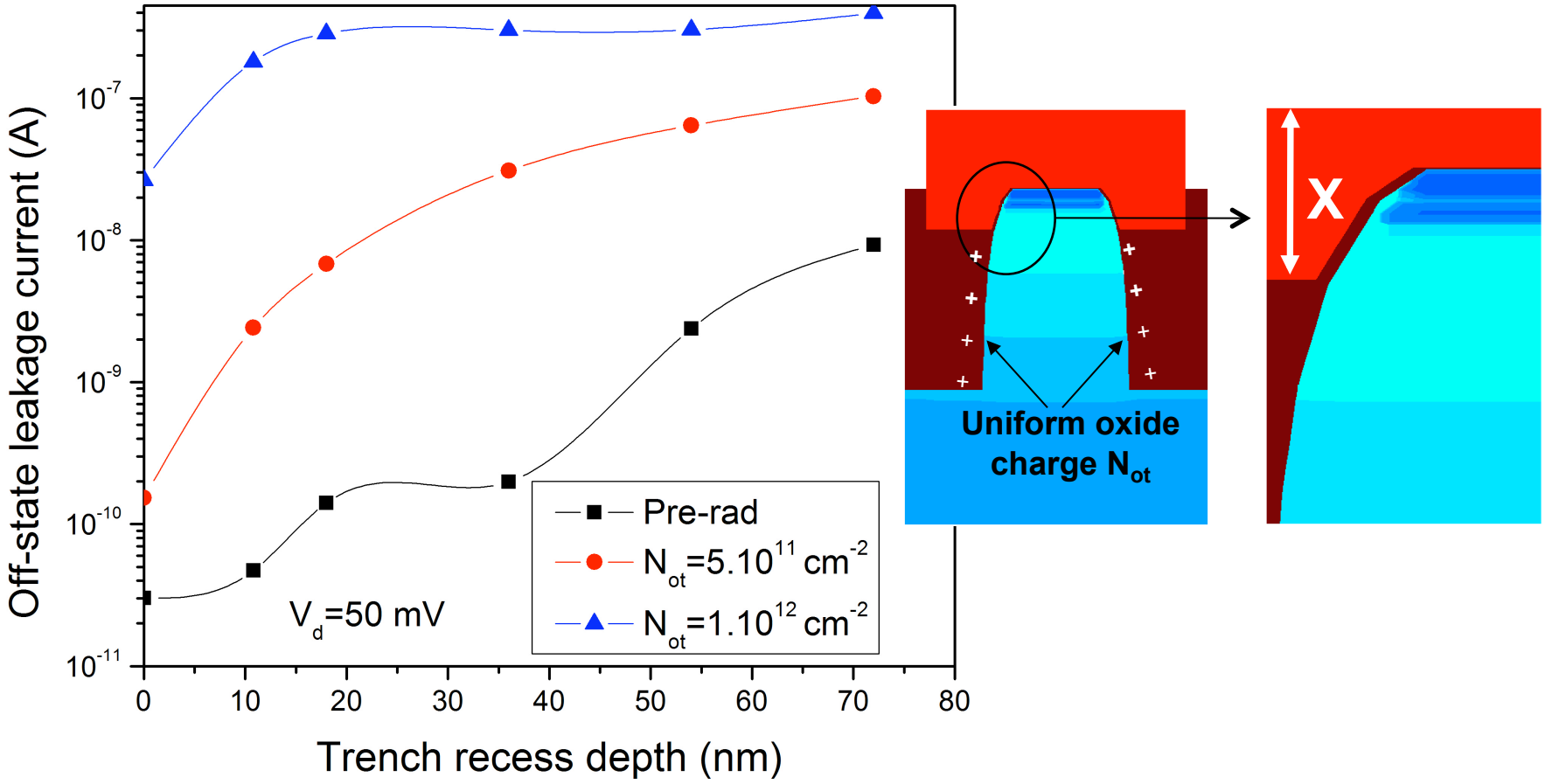


Lowest well doping level : 10^{17} cm^{-3}

Post-Rad: Trench Recess Depth

Vanderbilt Engineering

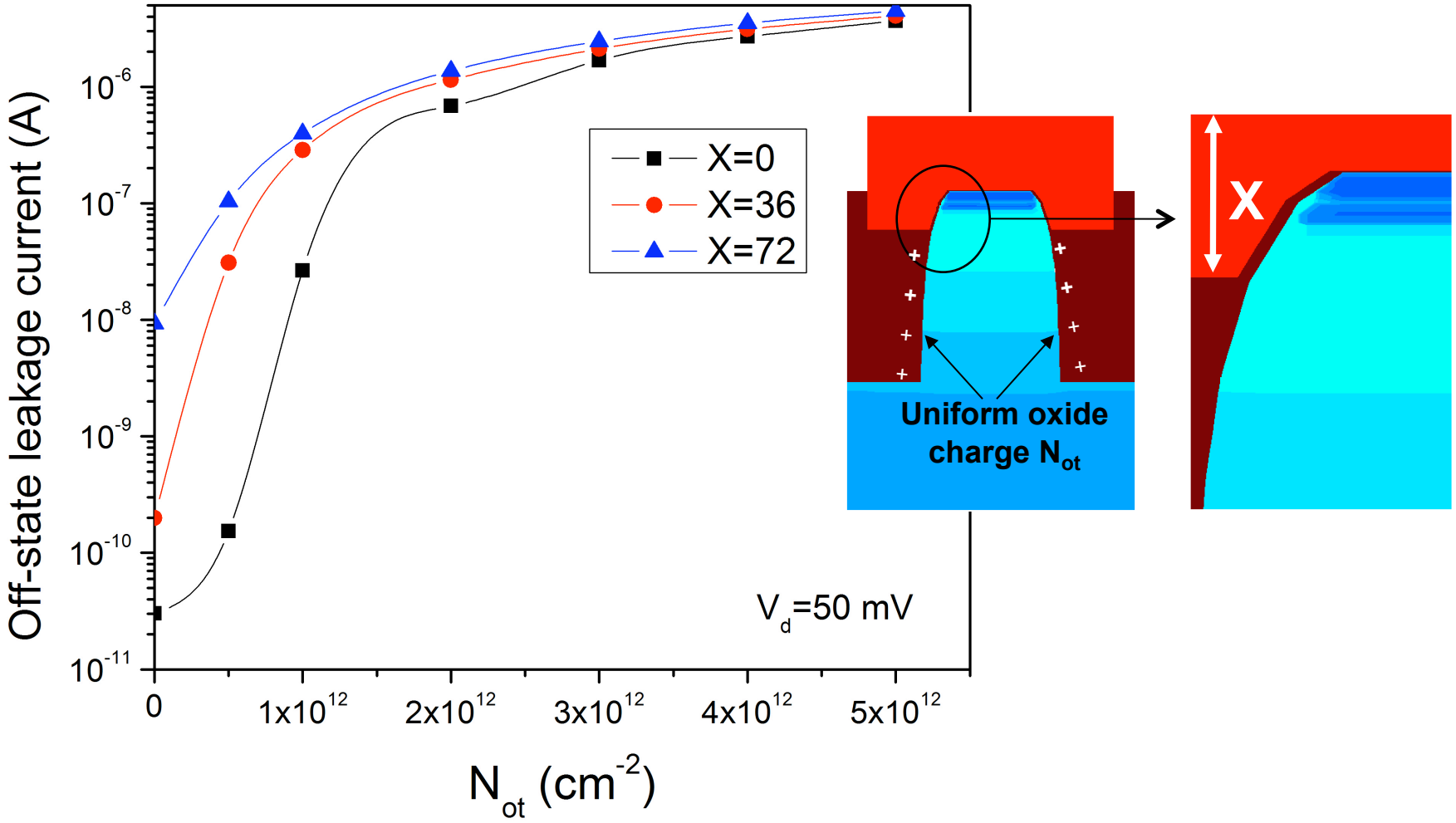
TID simulated by uniform oxide trapped charge density at the silicon/STI interface (N_{ot}) along the entire STI sidewall.



Post-Rad: Trench Recess Depth

Vanderbilt Engineering

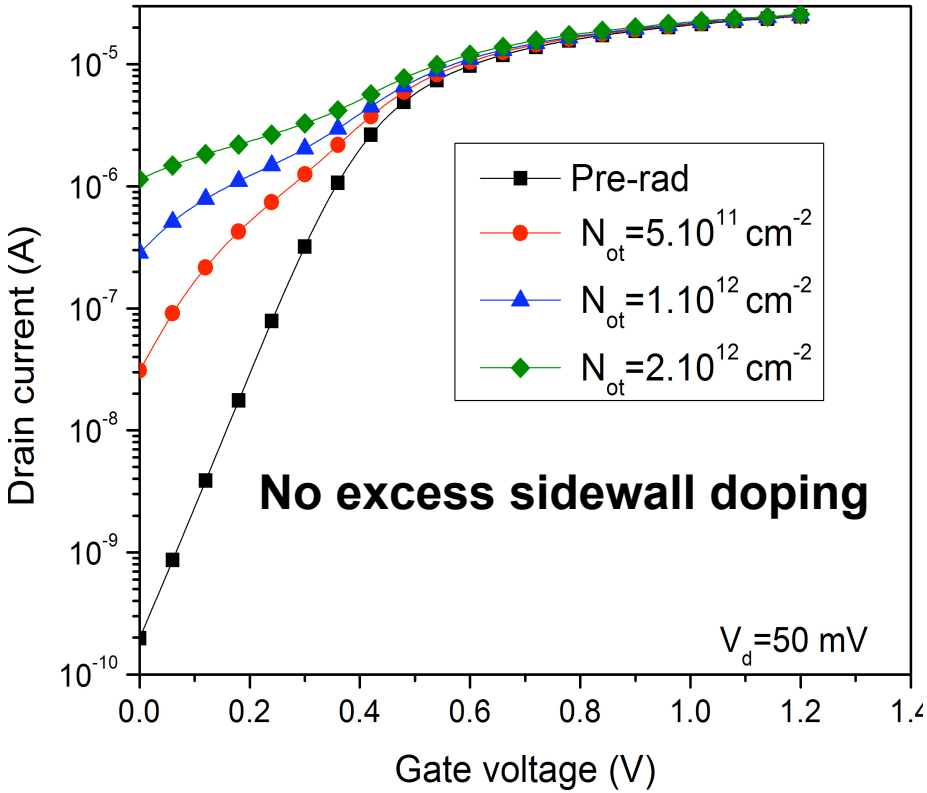
TID simulated by uniform oxide trapped charge density at the silicon/STI interface (N_{ot}) along the entire STI sidewall.

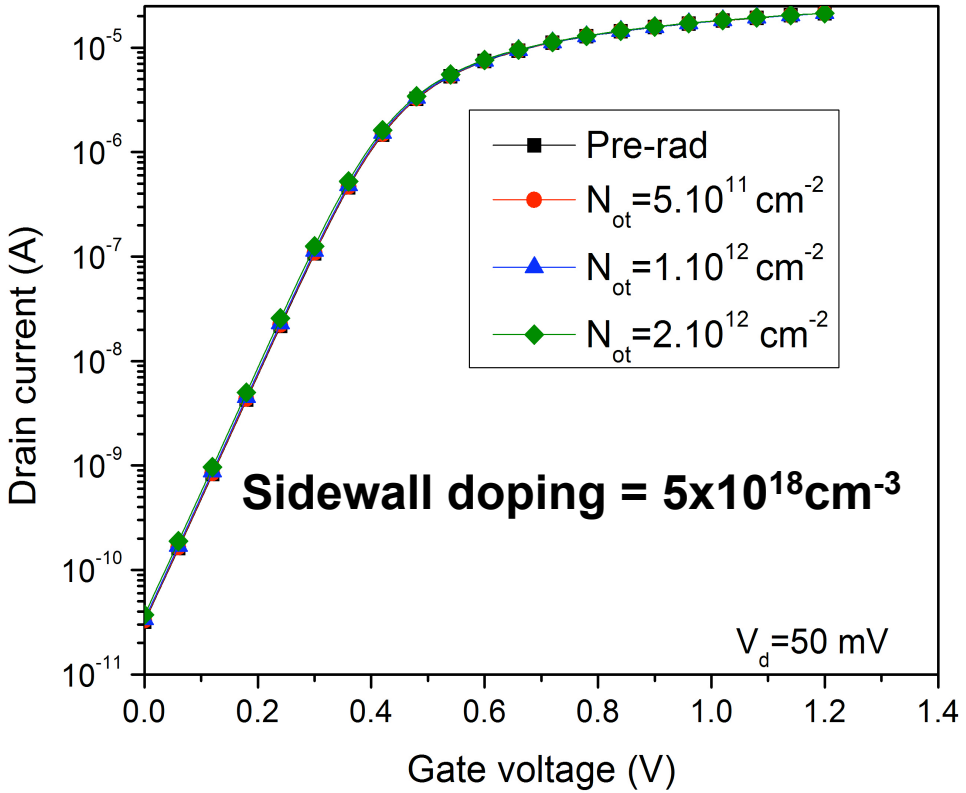


Post-Rad: 36 nm Recess with Sidewall Doping

Vanderbilt Engineering

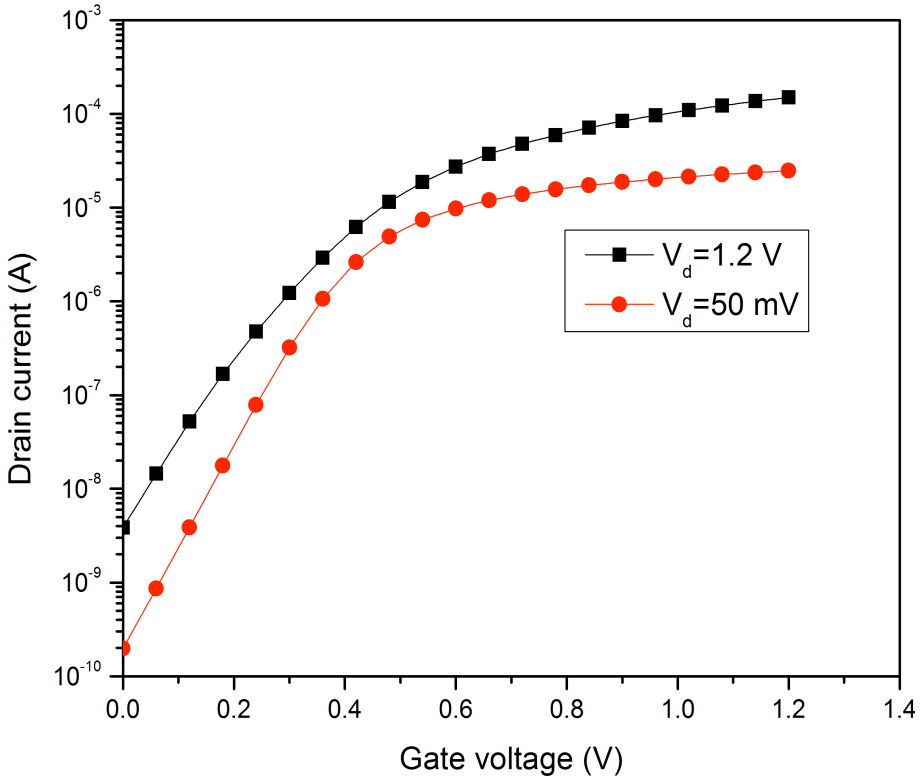
TID simulated by uniform oxide trapped charge density at the silicon/STI interface (N_{ot}) along the entire STI sidewall.

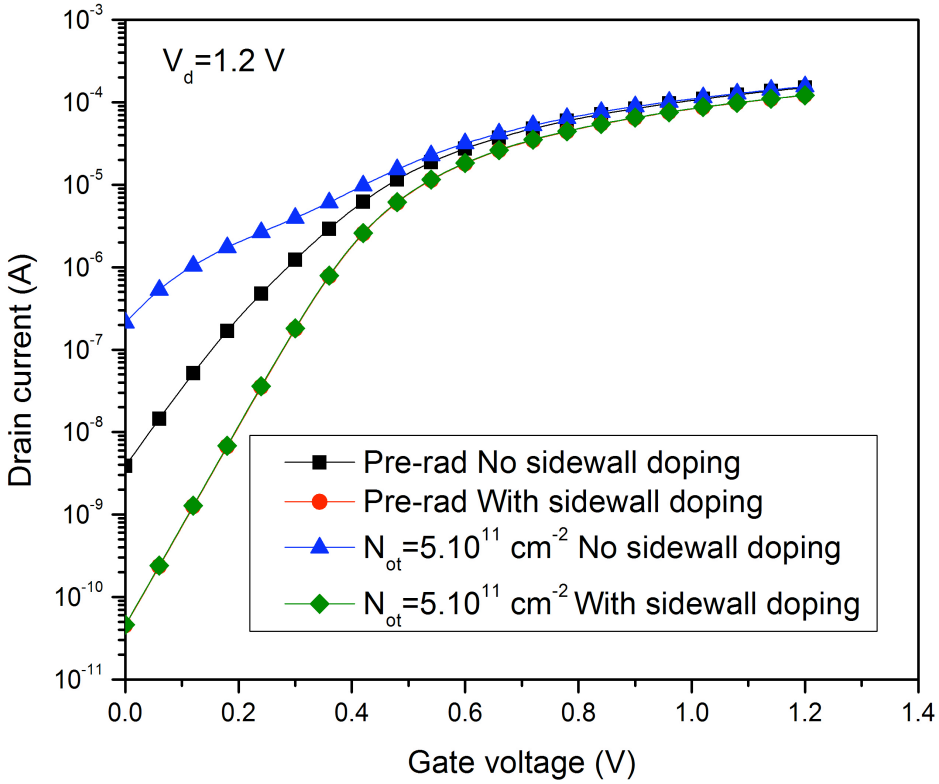




Drain Bias effect on leakage current

Vanderbilt Engineering





Pre-irradiation for 36 nm recess no sidewall doping

Pre- and Post-irradiation for 36 nm recess at V_d = 1.2 V

Summary

Vanderbilt Engineering

- Normal process variations impact leakage current on submicron technologies.
- Without excess sidewall doping, variation in the TID response may depend on variation in trench fill recess.
  - Sidewall doping >$10^{18}cm^{-3}$ eliminates sensitivity in simulations.
- **Future work:**

- Include non-uniform charge distributions (w/ H. Barnaby).
  - TID testing of devices with purposefully varied trench recess if/when available
  - Consider significance in SOI devices.