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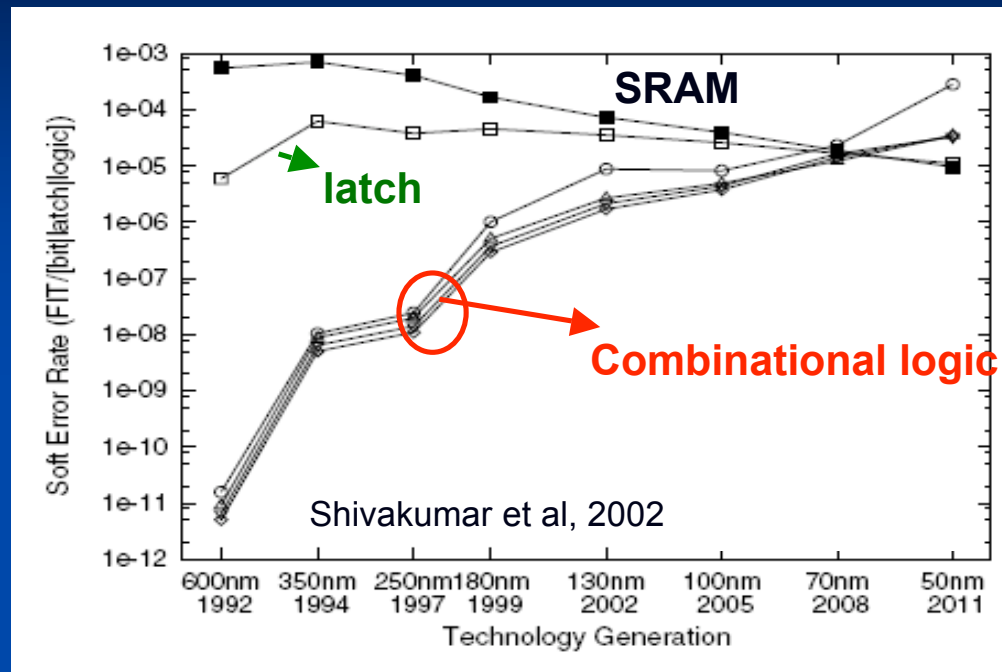
Single-Event Transient Pulse-Width Measurements in Advanced Technologies

Balaji Narasimham

MURI Review Meeting
May 13, 2008

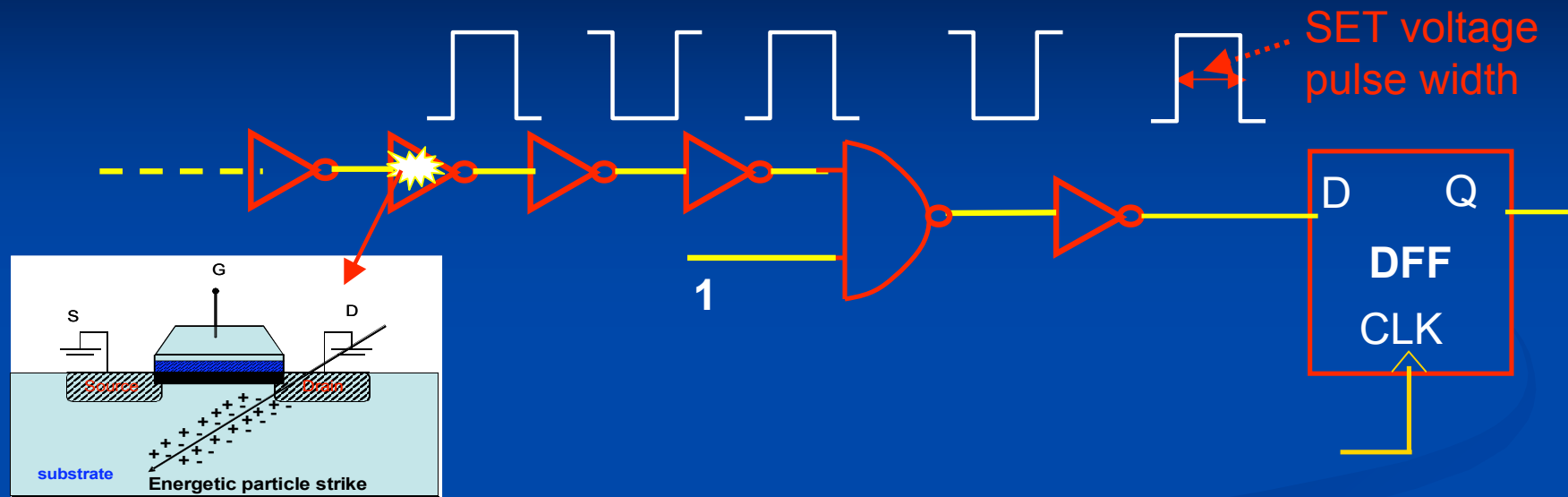
Supported in part by the DTRA Rad-Hard Microelectronics Program

Motivation



- Combinational logic soft errors – major reliability issue in advanced CMOS processes
- Knowledge of SET pulse widths – key to determining error rates
- Novel test circuit used for measurements of heavy-ion, neutron, proton and alpha SET widths in 130-nm and 90-nm
- Results indicate SET widths increase with scaling and are comparable to legitimate logic signals

Background



- SET pulse width & clock frequency determine circuit vulnerability
- Measurement difficulty
 - Pulse width in pico-second time scales – external measurement complex/costly
 - Random nature of ion strikes – external trigger signal cannot initiate measurement
- Developed on-chip self-triggered pulse measurement
- Statistical distribution of SETs measured in 130-nm and 90-nm with heavy-ions, neutrons, protons and alpha particles

Autonomous SET capture

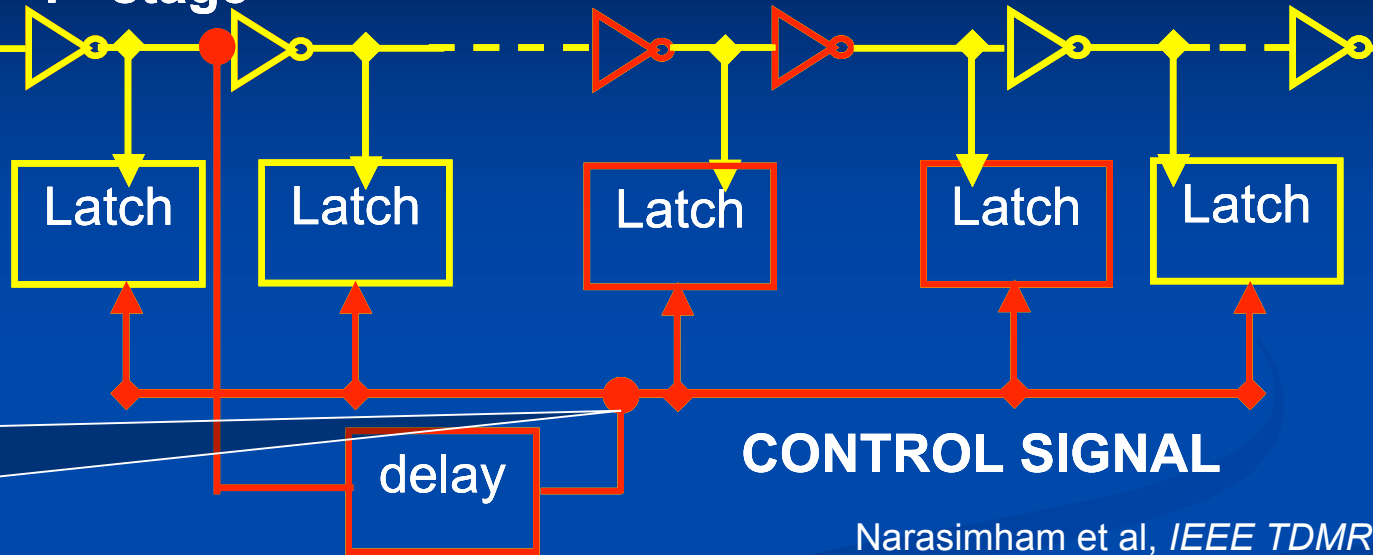


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1st stage



Autonomous or self-triggered SET pulse measurement

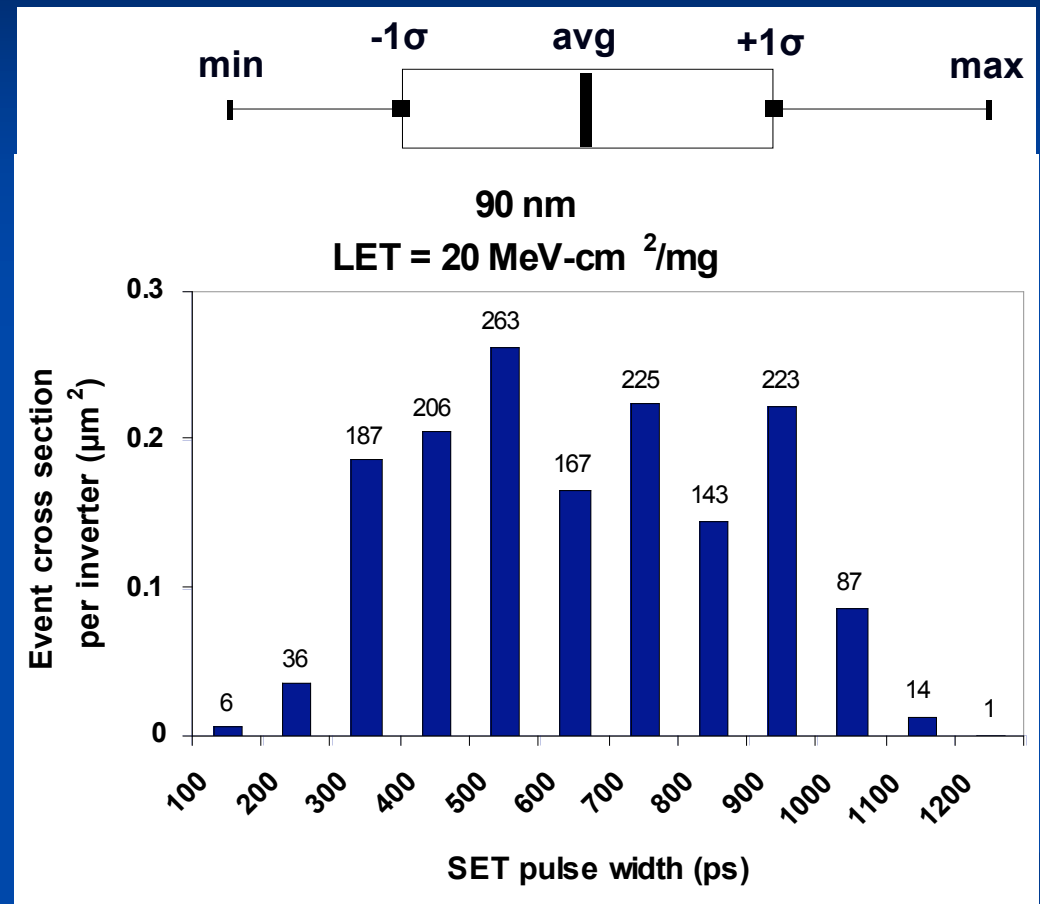
Narasimham et al, *IEEE TDMR*, 2006

- SET generated in custom inverter target circuitry – propagates and triggers measurement
- Pulse width is proportional to number of switched states (measured in units of inverter delays)
- Upsets after the trigger stage are not measured
- Most single latch upsets (due to direct strikes on the latch) are identifiable and SET width data not affected

Broad Distribution in SET Widths



- Width of SET pulses depend on several factors
 - Energy of incident ion
 - Location of strike with respect to sensitive drain
 - Technology effects of pulse generation (charge collection characteristics)
 - Circuit effects on pulse propagation
- Results in broad distribution of SET pulses for each radiation environment
- Our technique precisely characterizes this statistical distribution of SET pulse widths

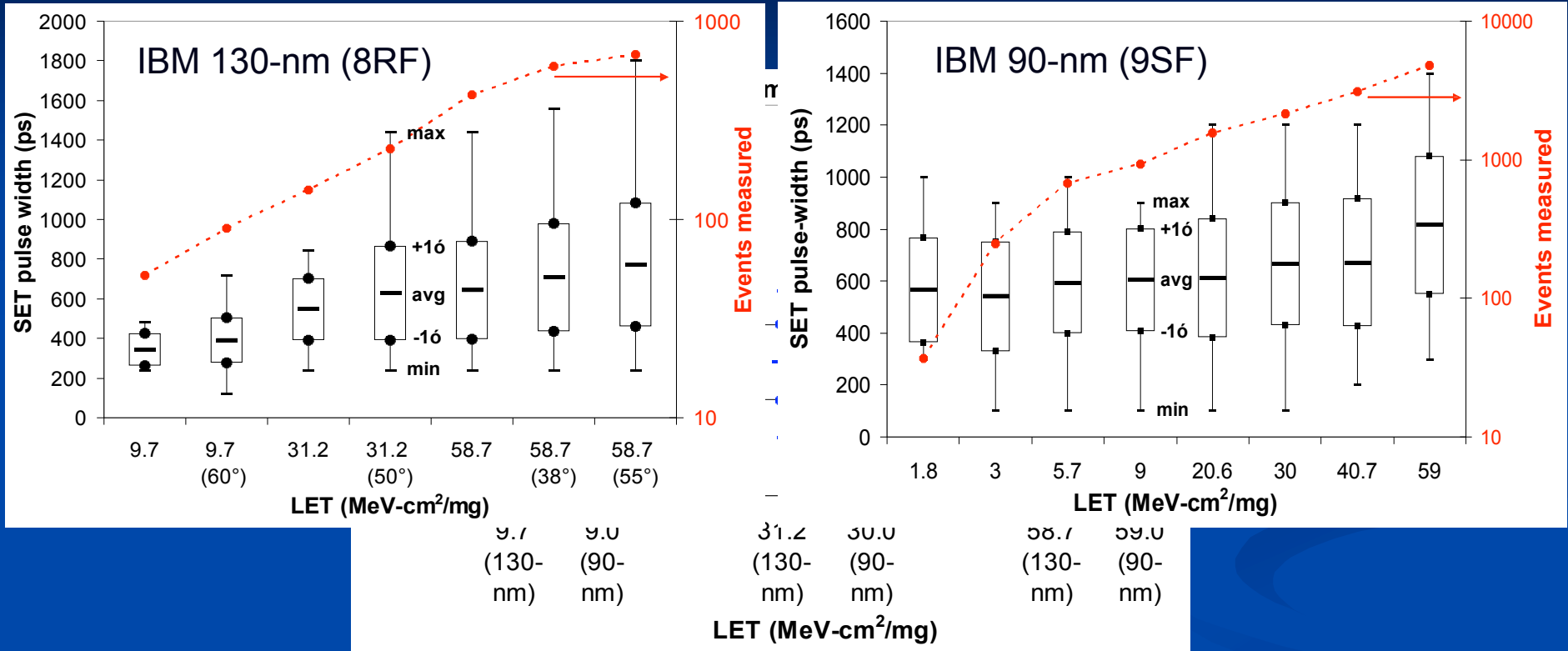


Heavy-Ion – 130-nm & 90-nm



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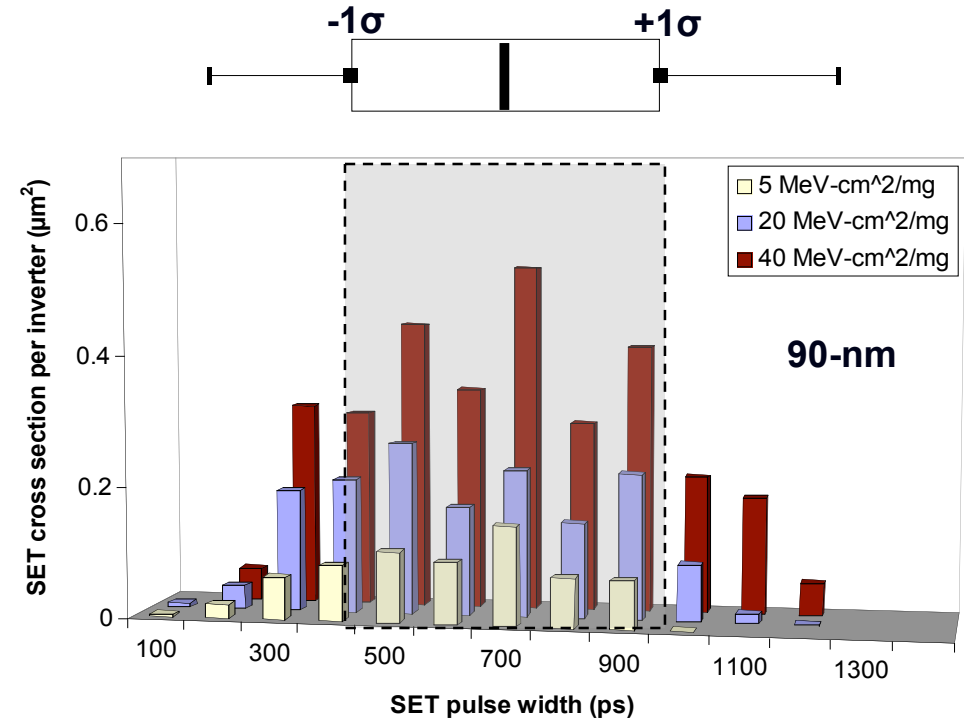
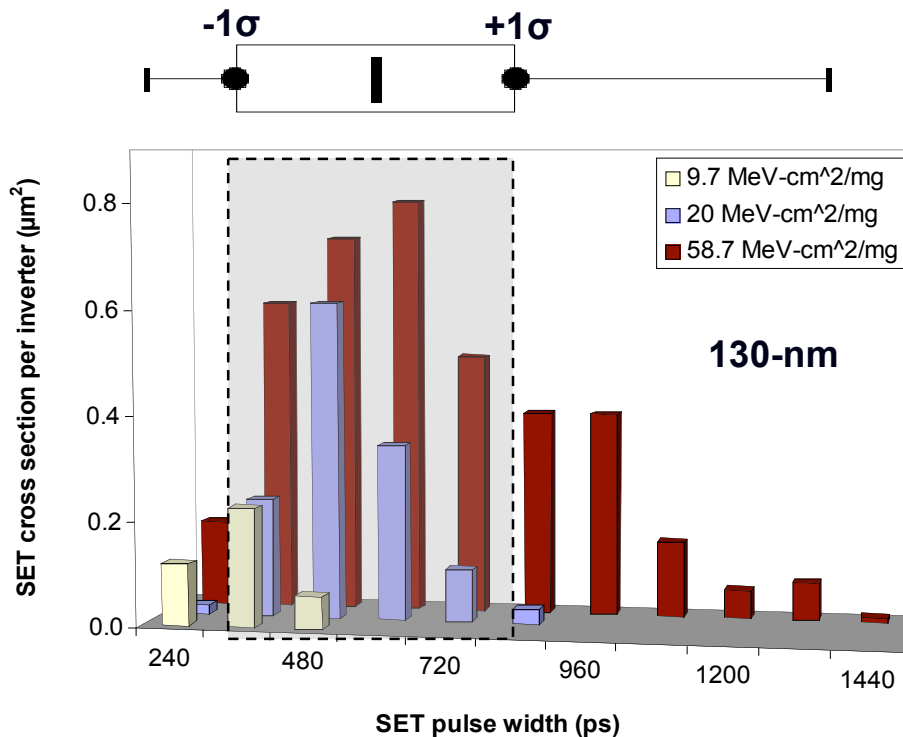
- Results indicate increasing SET pulse widths with scaling → important as latch setup/hold times decrease with scaling → more SETs latched as error

Cross Section Comparison



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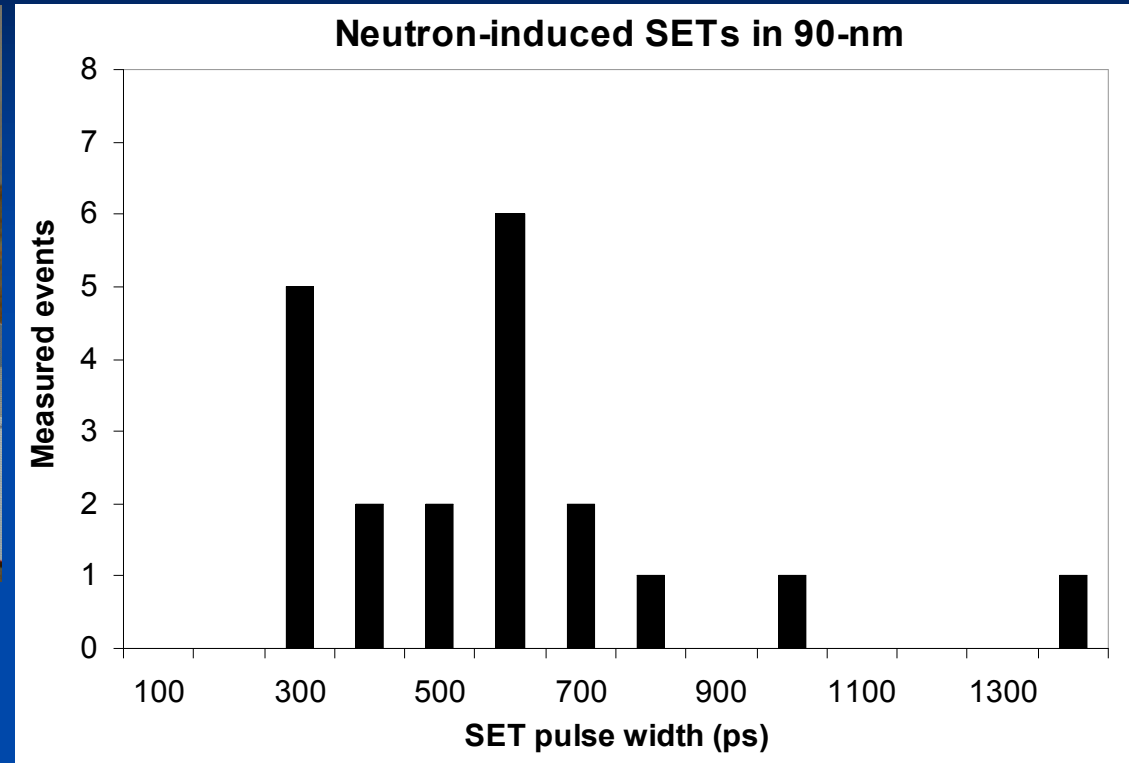
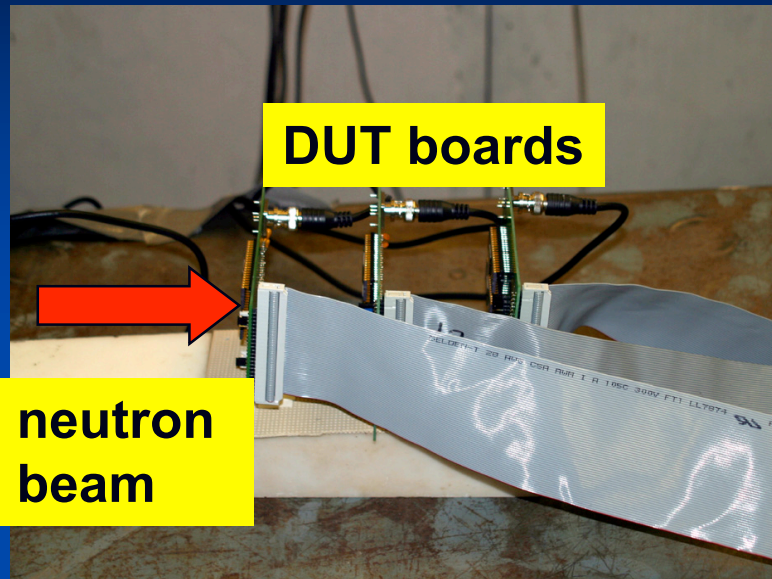
- Event cross section dominated by pulses between
 - 300 ps to 700 ps in 130 nm
 - 400 ps to 900 ps in 90 nm
- Increase in wider transients translates to higher error rates with scaling



Neutron-Induced SETs

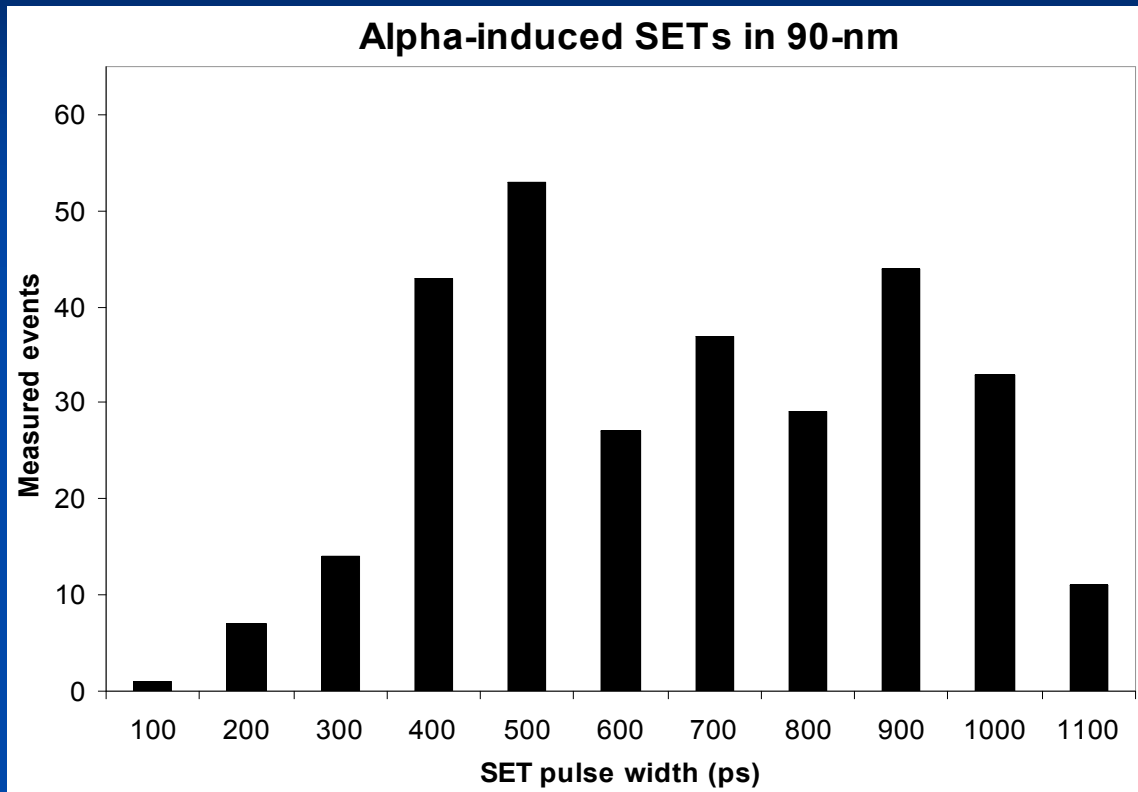
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- Tested six 90-nm ICs at WNR facility at LANL
- Energy spectrum matches sea-level spectrum for energies from 10 to 500 MeV
- Neutron fluence 1.33×10^{11} neutrons/cm²
- Neutron SET cross-section $\sim 2.5 \times 10^{-6}$ $\mu\text{m}^2/\text{inverter}$

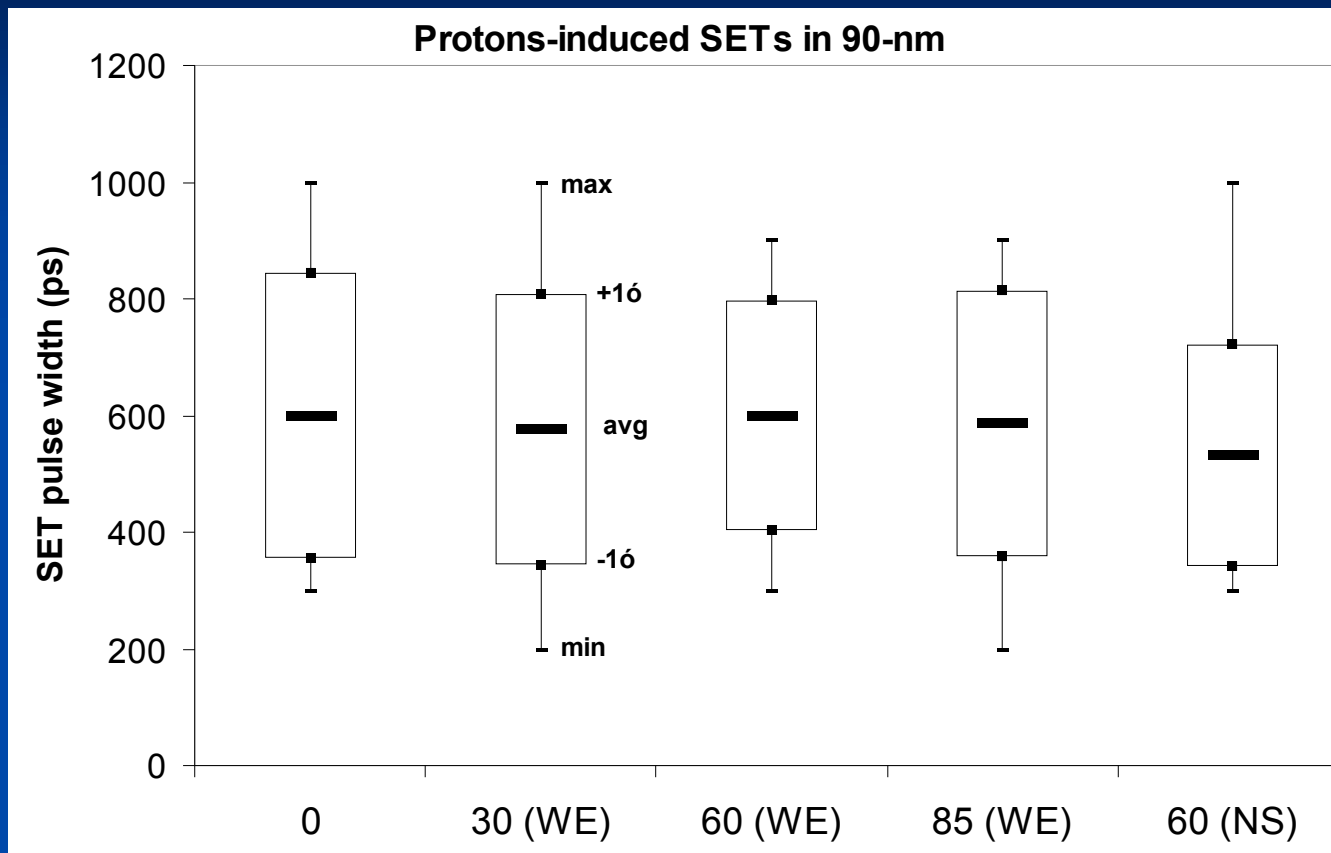
Alpha-Induced SETs



- Alpha tests at TI using foil of Am^{241}
- Energy ~ 5.5 MeV
- Fluence $\sim 4.45 \times 10^{10}$ alphas/cm²
- Total events measured ~ 300

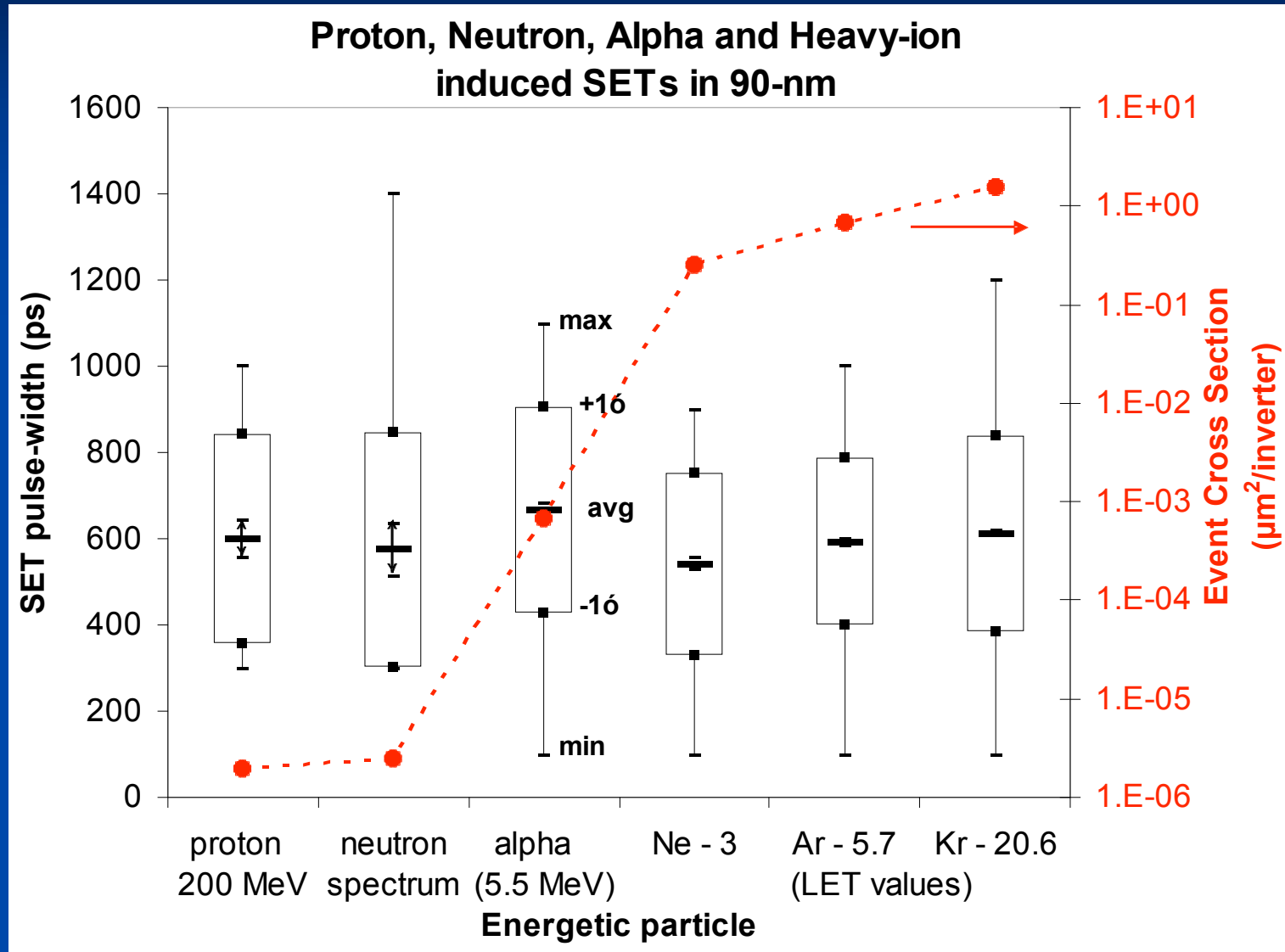
- Alpha SET cross section $\sim 6.74 \times 10^{-4}$ $\mu\text{m}^2/\text{inverter}$

Proton-Induced SETs

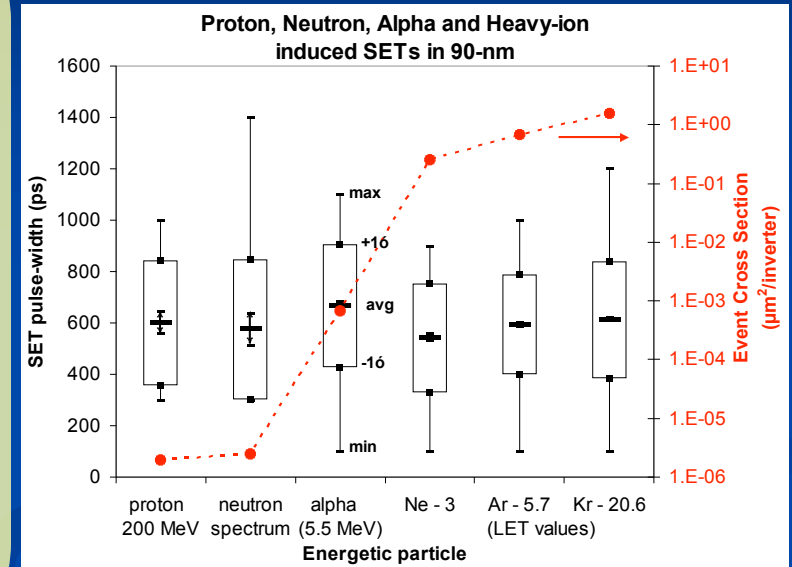
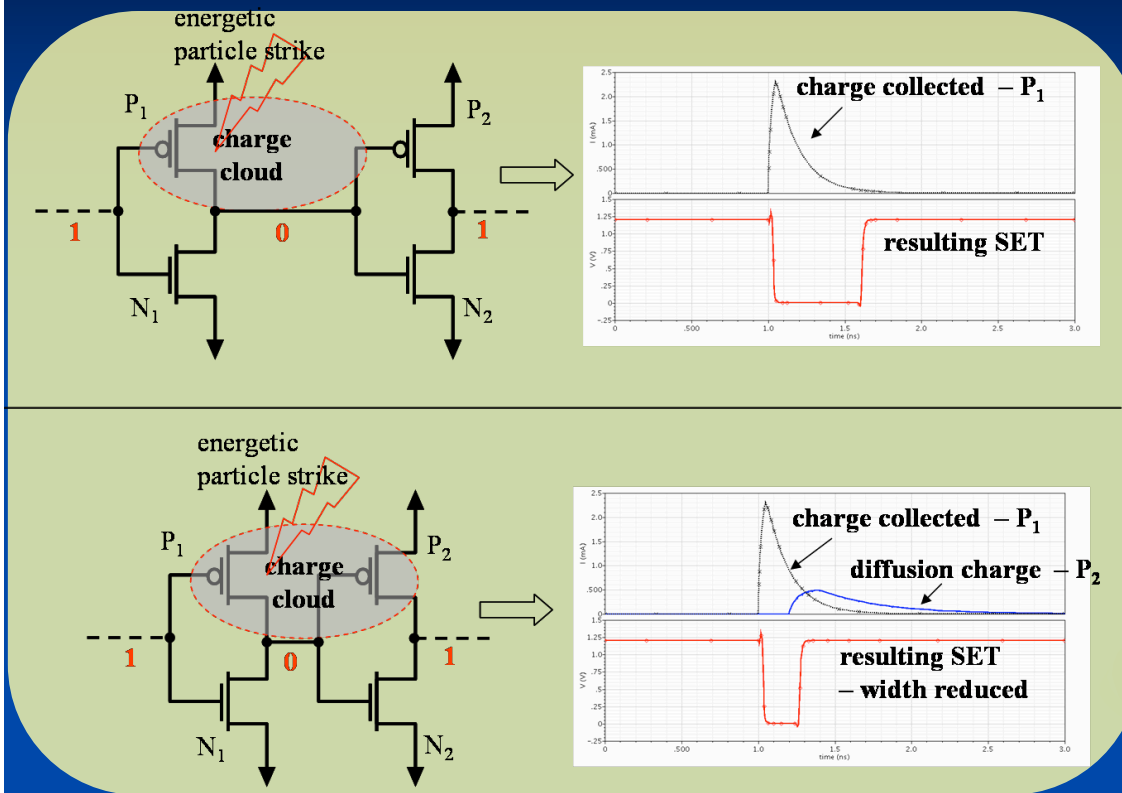


- Tests conducted at Indiana Univ with 200 MeV protons
- Proton SET cross-section $\sim 2 \times 10^{-6} \mu\text{m}^2/\text{inverter}$
- Results indicate that proton angle of incidence does not affect SET width distributions

Comparison – Energetic Particles



Similarity in SET Distributions



- Less variation in SET pulse widths for different particle types – probably due to carrier redistribution and charge sharing effects
- Preliminary simulations indicate charge spread and diffusion collection by subsequent gate may limit SET widths

Other Applications



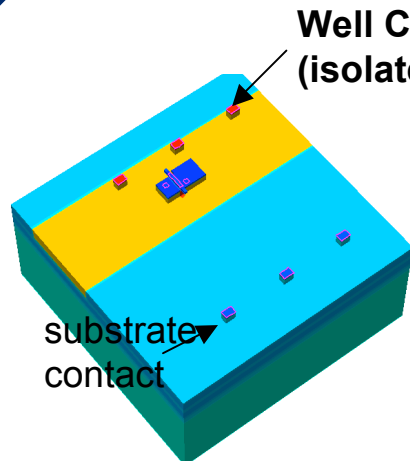
- **Test circuit can help quantify effects of process or layout variations on single events**
 - Circuit was used for quantifying effect of guard bands in mitigating long SETs
- **Characterization of effect of charge spread on SET width distributions**
 - Tested with ions incident from different directions with respect to n-well layout
 - Interleaved inverter chains have been designed to further analyze charge spread effect

Well Contacts and Guard Bands

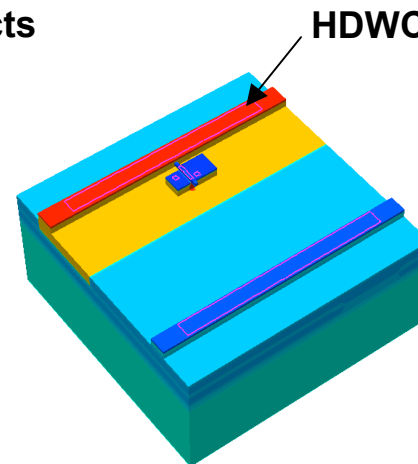


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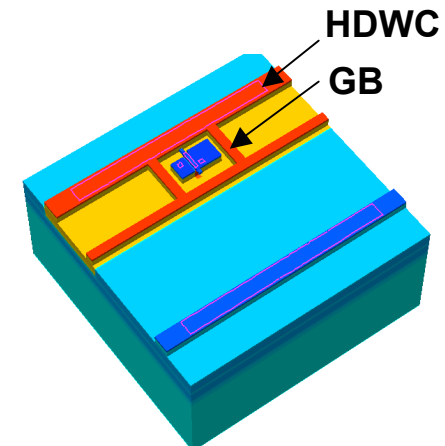
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Conventional Layout – Isolated Well Contacts

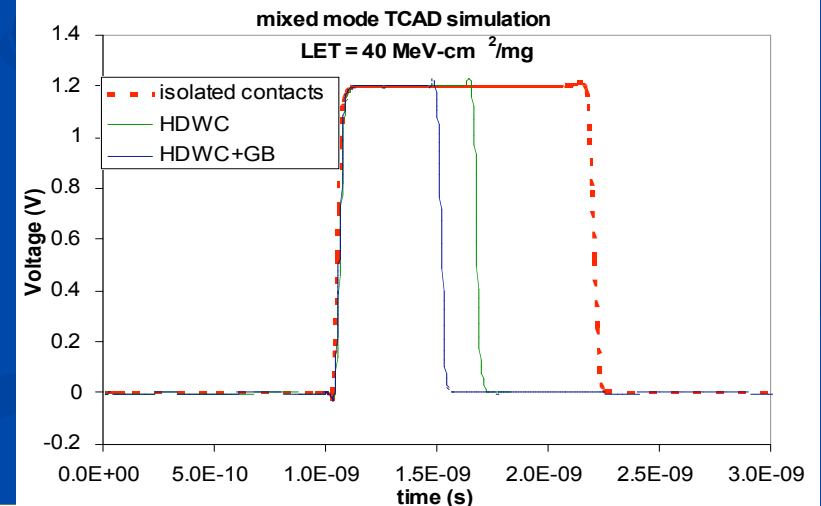


High Density Well Contacts (HDWC)



HDWC + Guard Band (GB)

- Strikes within n-well lead to long SETs due to parasitic bipolar effect
- Mixed mode simulations using calibrated 130-nm process – show effect of GB and HDWC in mitigating long SETs

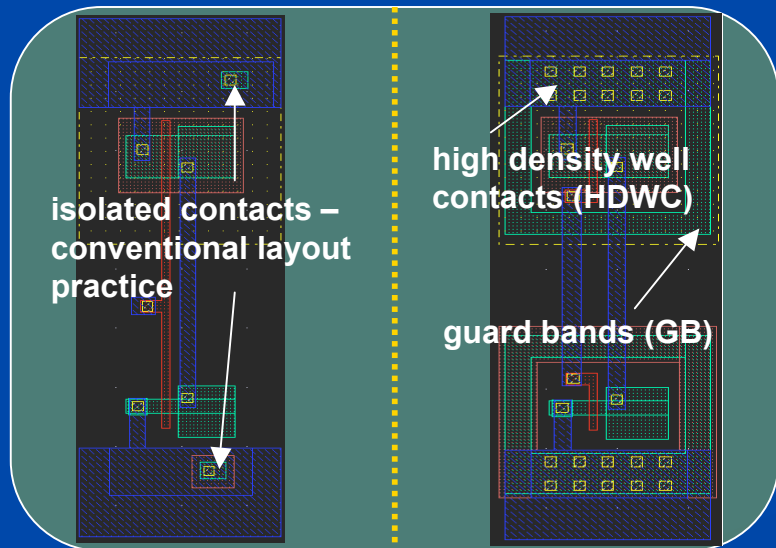
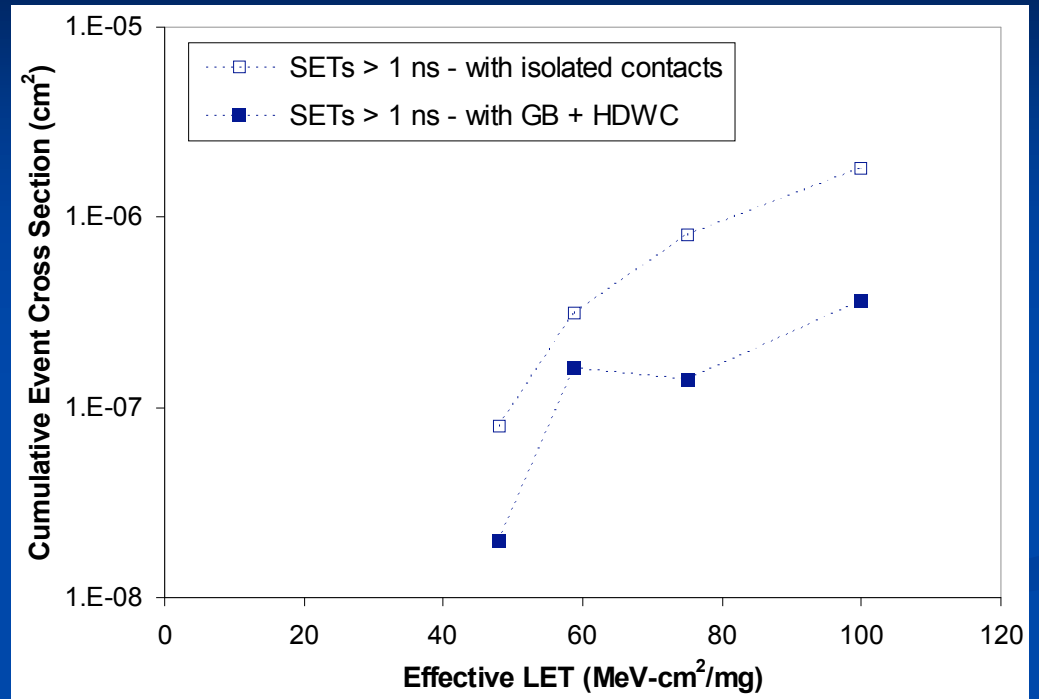
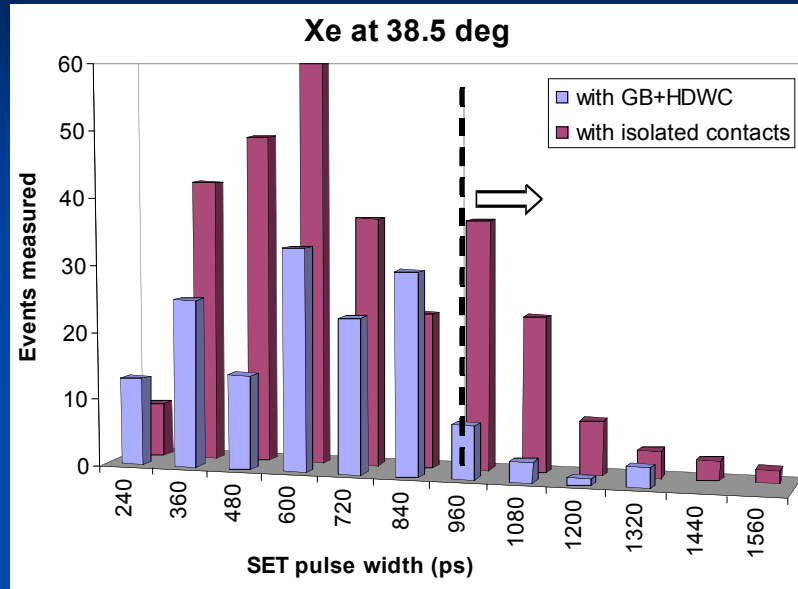


Characterizing Guard Bands



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- Events > 1ns reduced by ~72% for circuits with GB + HDWC
- Reduction in frequency and max SET width attributed to reduction in parasitic bipolar effect

Impact



- **Resolve controversy on expected pulse widths**
- **Quantify technology trends in SET pulse widths**
- **Characterize effect of RHBD structures such as multiple well contacts and guard bands on SET pulse widths**
- **Determine effect of charge sharing on SETs**
- **Technique can also be used to measure other spurious signals such as cross-talk pulses**

Conclusion



- **Autonomous SET characterization technique developed and implemented to obtain precise distributions of heavy-ion, neutron, proton and alpha induced SET widths in 130-nm/90-nm CMOS**
- **Width and range of dominant SETs increase with scaling**
- **Neutron and alpha particle induced SETs are of order of legitimate logic signals – concern for commercial applications**
- **High density well contacts and guard bands helps reduce more than 70% of SETs longer than 1 ns**