Fin-Width Dependence of Ionizing Radiation-Induced Degradation in 100-nm Gate Length FinFETs

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OUTLINE

- **FinFETs**
- **Previous work**
- **Experimental details**
- **Experimental results and discussion (A)**

▪ *The impact of the number of fins on the I_d-V_{gs} of multi fins FinFETs*

- **Experimental results and discussion (B)**

▪ *The threshold voltage (V_{th}) decreases with the fin width in irradiated FinFETs*

▪ *The subthreshold Swing (SS) increases with the the fin width in irradiated FinFETs*

- **Conclusion**
- **Future work**

SILICON ON INSULATOR FINFETS

Better Subthreshold Swing

Better control of short channel Effects

BOX

Gate

Fin

Source

Drain

26013 W#6061312D-19

018 5.0kV 5.5mm x120k SE(M) 7/27/2006

Better SEE response

Better Control of the floating body effects

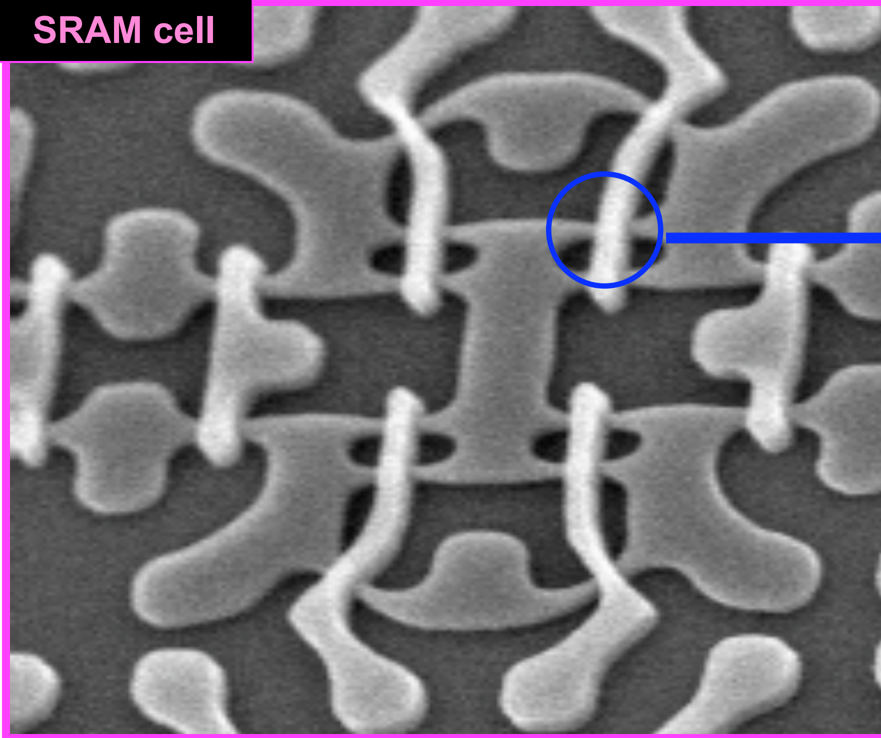
PREVIOUS WORK

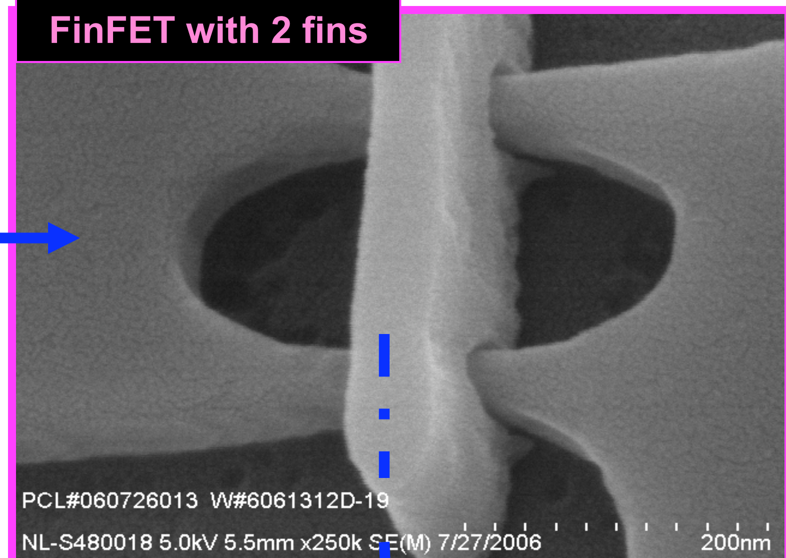
Narrower FinFETs with very long gate length (10 µm) are more tolerant to TID effects than wider FinFETs

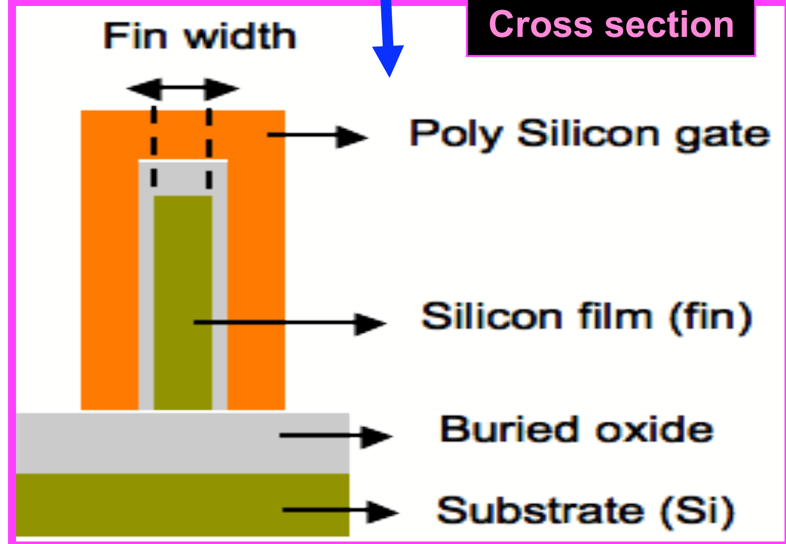
[2] M. Gaillardin, R. Paillet, V. Ferlet-Cavrois, O. Faynot, C. Jahan, and S. Cristoloveanu, "Total ionizing dose effects on triple-gate FETs," *IEEE Trans. Nucl. Sci.,* vol. 53, pp. 3158-3165, Dec 2006.

EXPERMENTAL DETAILS (1/2)

Device details







Number of fins **:** 2 and 20.

Fin Width : 40 nm, 65 nm and 80 nm

Gate length : 100 nm for FinFETs

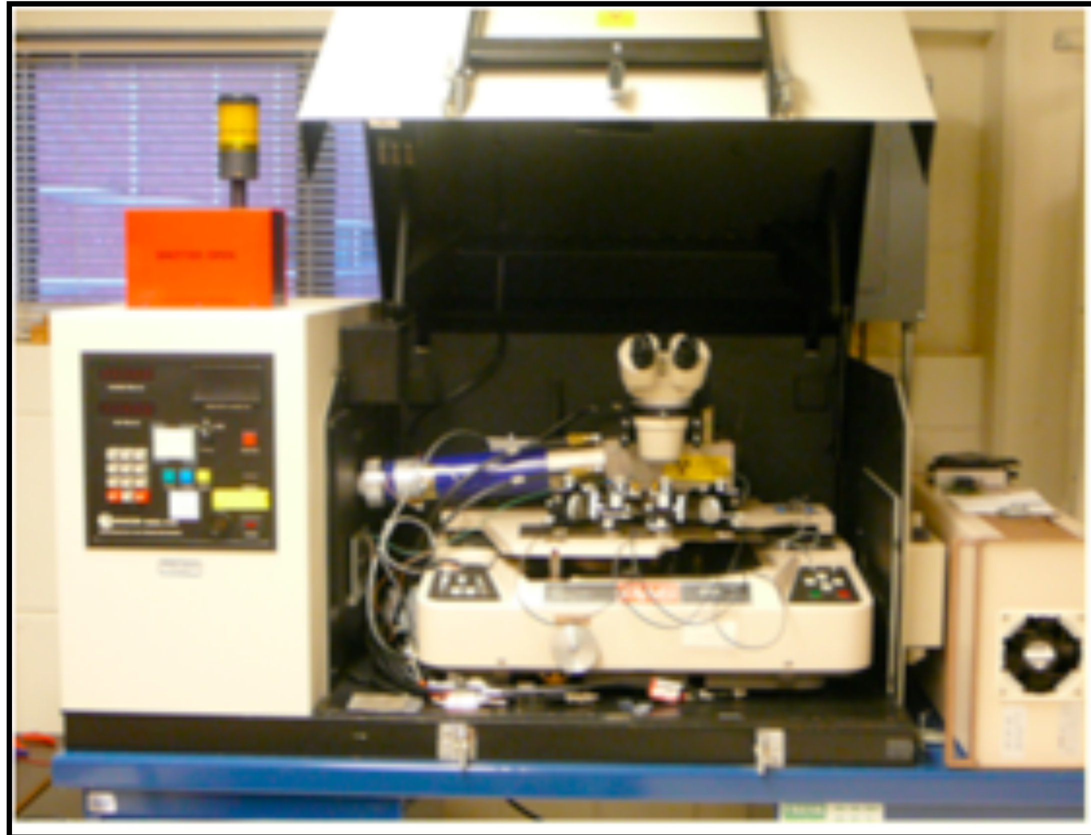
Gate oxide thickness : 2 nm

BOX thickness : 150 nm

Silicon film thickness : 58 nm

EXPERMENTAL DETAILS (2/2)

Measurement conditions



In-situ irradiations and I-V measurements for all FinFETs were performed without removing the probes from the wafers.

EXPERIMENTAL RESULTS AND DISCUSSION (A)

EXPERMENTAL RESULTS (A1)

Measurement conditions:
Back gate and source terminals = 0.0 V
Drain bias = 1.0 V

20 fins

2 fins

NUSS

FW/L = 65/100

Drain Current (I_{ds})

Gate Voltage (V_{gs})

0.01, 1E-3, 1E-4, 1E-5, 1E-6, 1E-7, 1E-8, 1E-9, 1E-10, 1E-11, 1E-12

-0.8, -0.6, -0.4, -0.2, 0.0, 0.2, 0.4, 0.6, 0.8

A Non Uniform Subthreshold Slope (NUSS) in the I_d-V_{gs} slope has been observed in some of the 2 fins FinFETs for the 100 nm gate length devices.

EXPERMENTAL RESULTS (A2)

Measurement conditions:
Back gate and source terminals = 0.0 V
Drain bias = 1.0 V

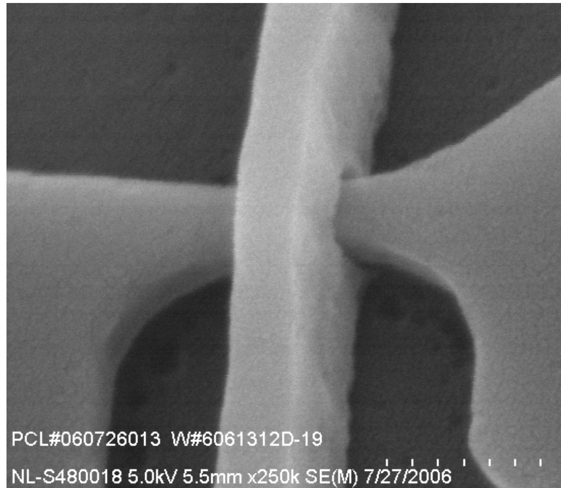
20 fins
2 fins
NUSS
FW/L = 65/90

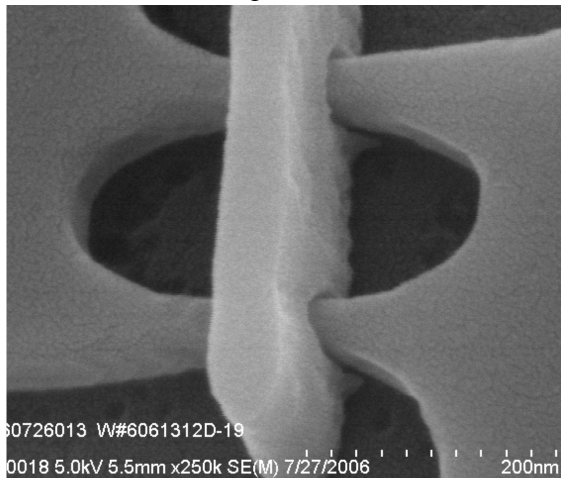
Drain Current (I_{ds})
0.01
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12

-0.8 -0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8
Gate Voltage (V_{gs})

A Non Uniform Subthreshold Slope (NUSS) in the I_d-V_{gs} slope has been observed in some of the shorter (90 nm) 2 fins FinFETs as well.

FIN TO FIN VARIABILITY (1/2)

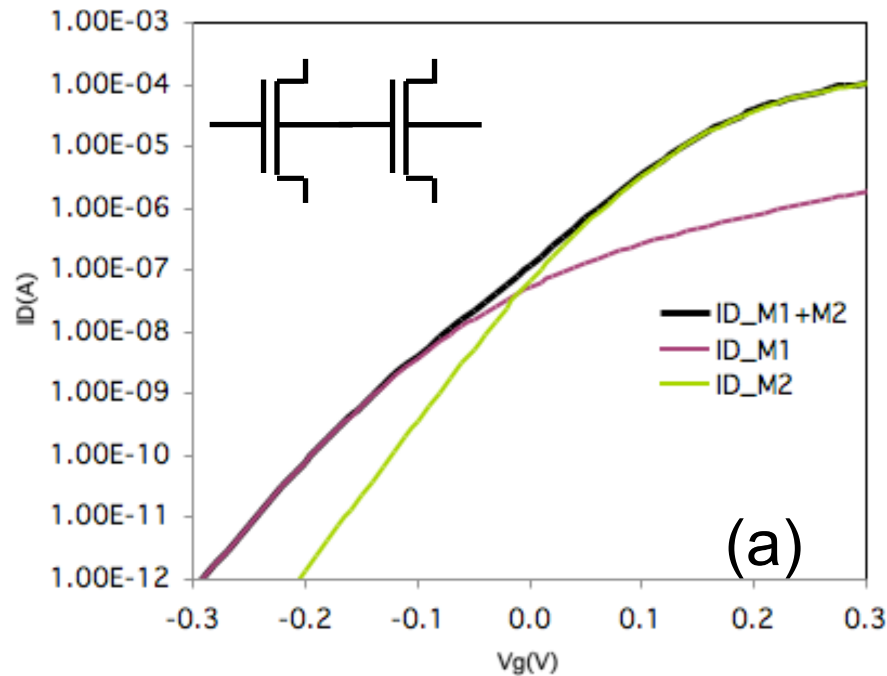


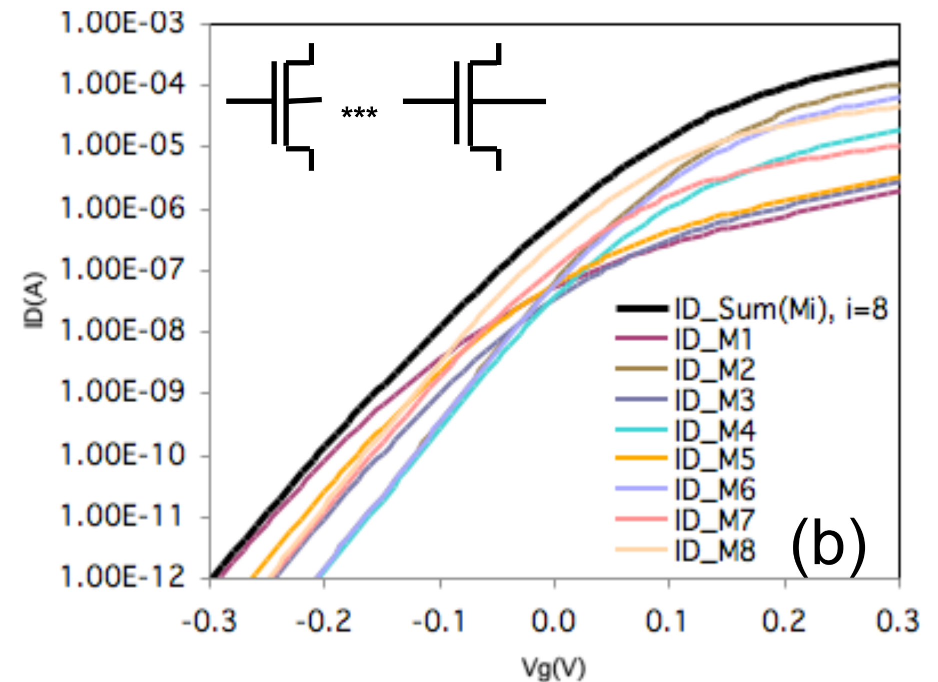


Hypothesis:

Due to fin to fin variability in multi fins FinFETs, different fins (transistor) start conducting at different times which Induces the Observed non uniform subthreshold slope in the I_d-V_{gs} Curves In the previous slides.

FIN TO FIN VARIABILITY (2/2)



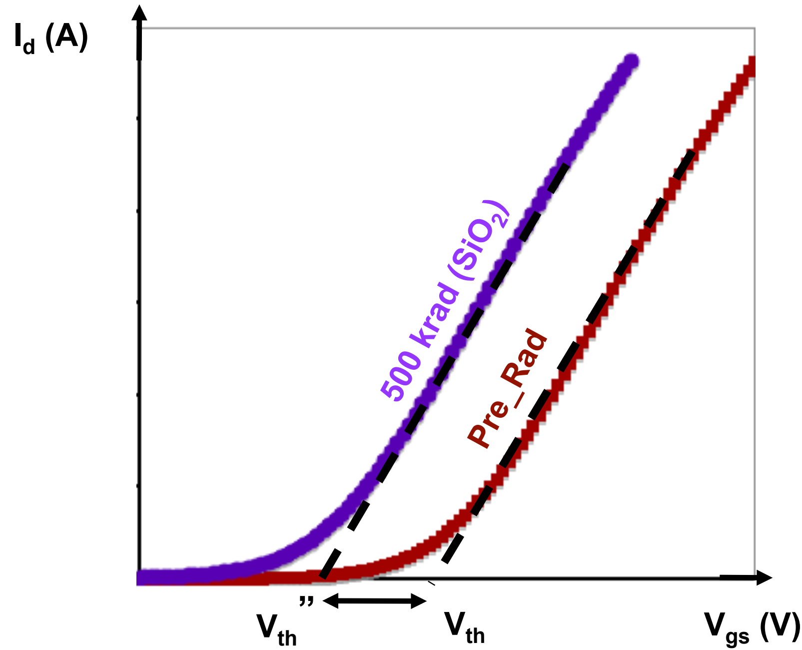


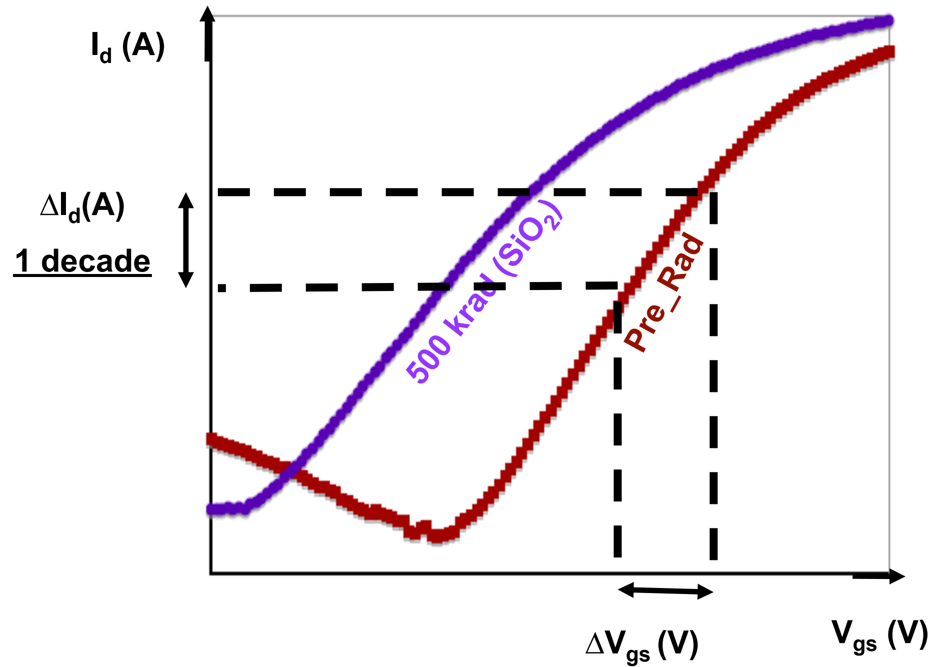
- ❑ Composite I_d-V_{gs} of two parallel (Fig. a) and 8 (Fig. b) planar NMOS SOI transistors simulated using T-Spice.
- ❑ In these simulations the transistor width (W), the threshold voltage (V_{th}) and the channel length (L) were varied.

W_min	50 n
W_max	3 µm
Vth_min	0.3 V
Vth_max	0.4 V
L_min	1 µm
L_max	1.15 µm

EXPERIMENTAL RESULTS AND DISCUSSION (A)

RECALLS..





Subthreshold Slope: $\Delta I_d/\Delta V_{gs}$ [Decade/ V]

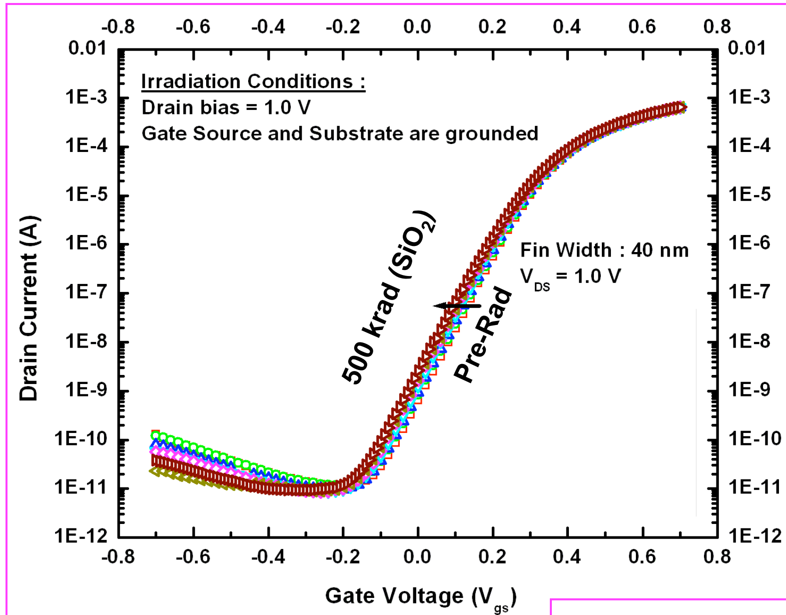
Subthreshold Swing (SS): $\Delta V_{gs}/\ \Delta I_d$ [V/Decade]

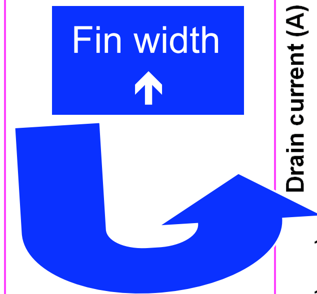
V_{th} shift = V_{th}" - V_{th}

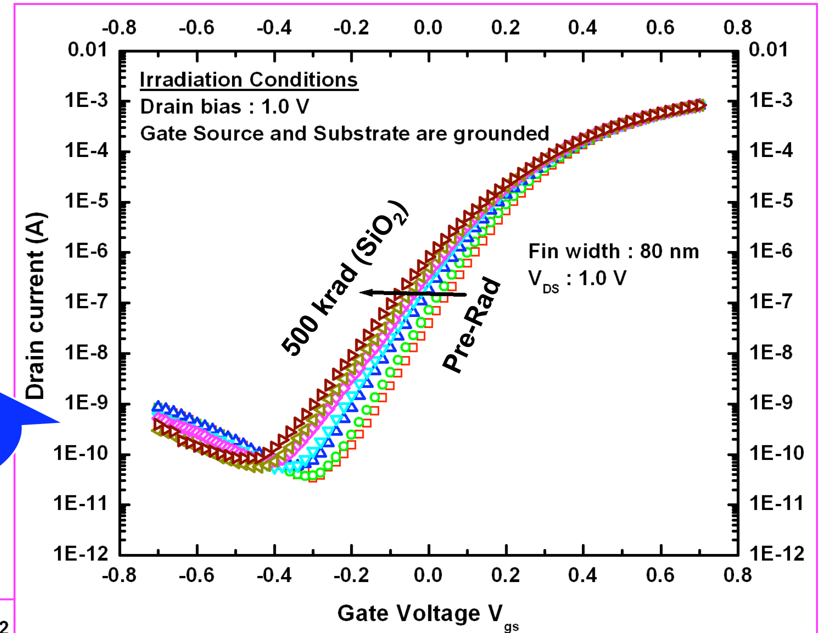
SS shift =

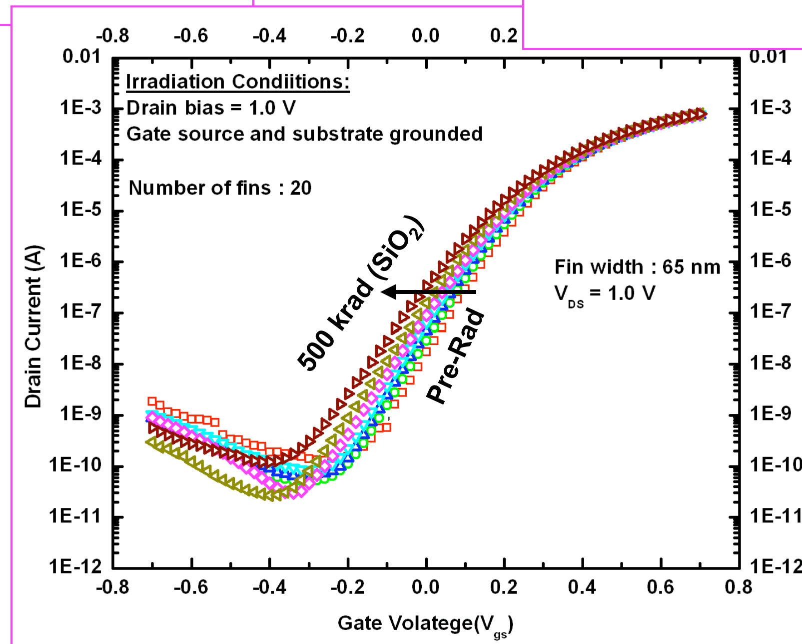
SS (Post-Rad) - SS (Pre-Rad)

EXPERMENTAL RESULTS (B)









V_{th} decrease with the fin width in irradiated FinFETs

SS increases with the fin in irradiated FinFETs

NARROWER FINFETS SHOW HIGHER TOLERANCE TO TID EFFECTS, smaller V_{th} shifts

Fin Width

80 nm

65 nm

40 nm

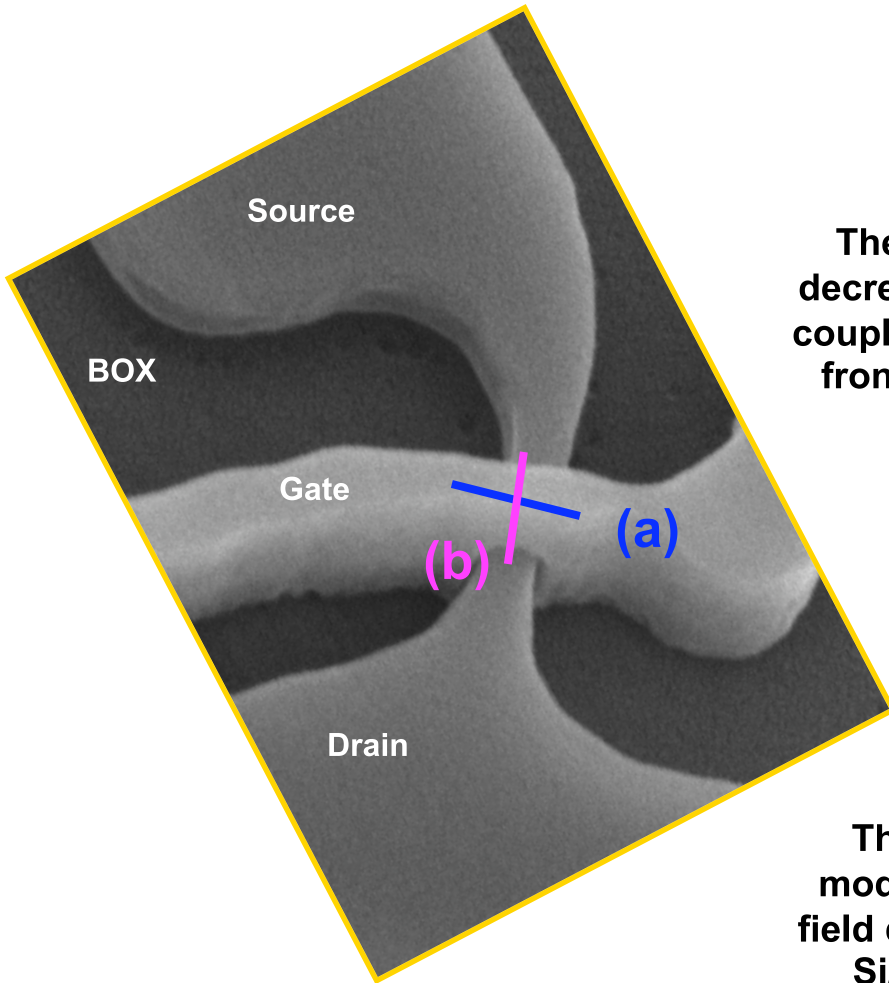
Threshold Voltage Shift V_{th}(V)

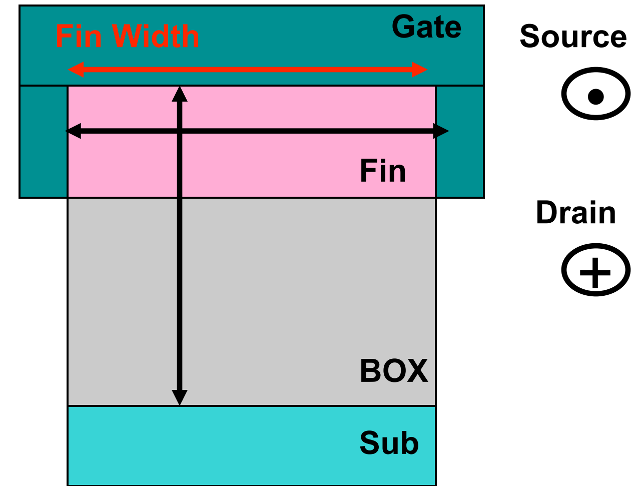
Dose (Krad (SiO_2))

0.00 0.01 0.02 0.03 0.04 0.05 0.06

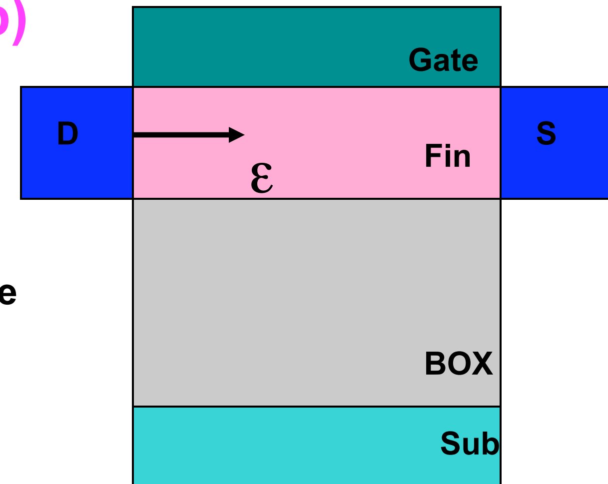
0 100 200 300 400 500

NARROWER FINFETS SHOW HIGHER TOLERANCE TO TID EFFECTS, smaller V_{th} shifts





The lateral gates decrease the vertical coupling between the front and the back gates.



The lateral gates modifies the electric field distribution in the Si/BOX interface.

NARROWER FINFETS SHOW HIGHER TOLERANCE TO TID EFFECTS, smaller SS shifts

SS Shift (mV/Decade)

Dose (Krad (SiO_2))

80 nm

65 nm

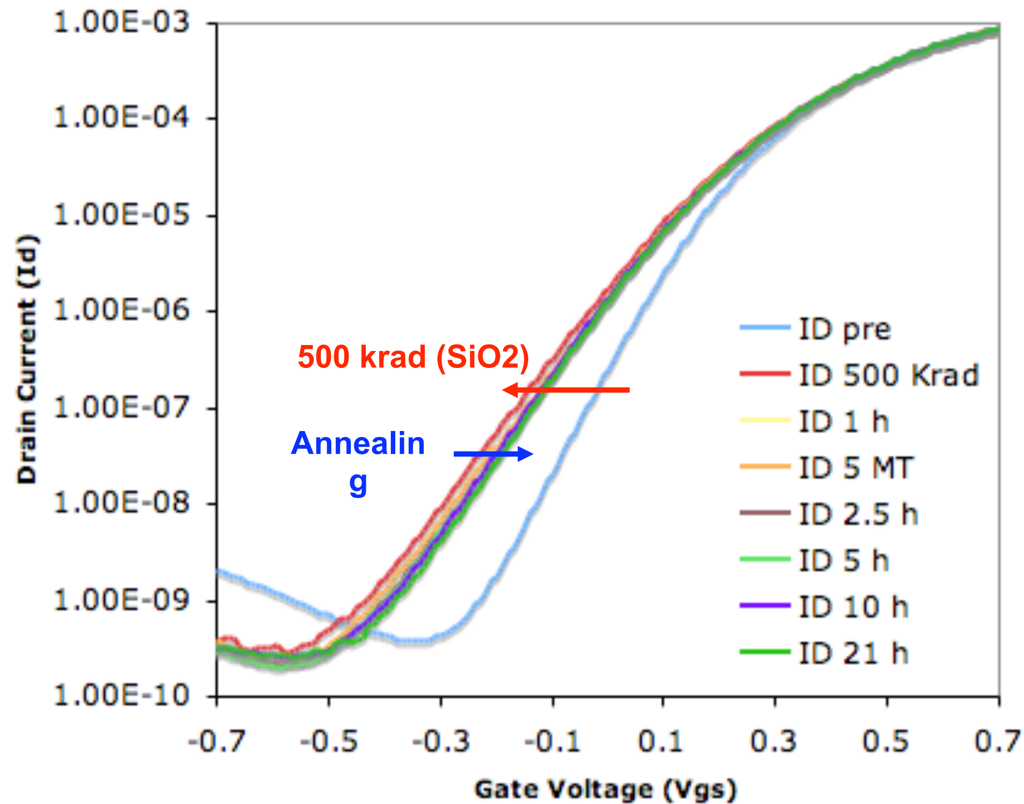
40 nm

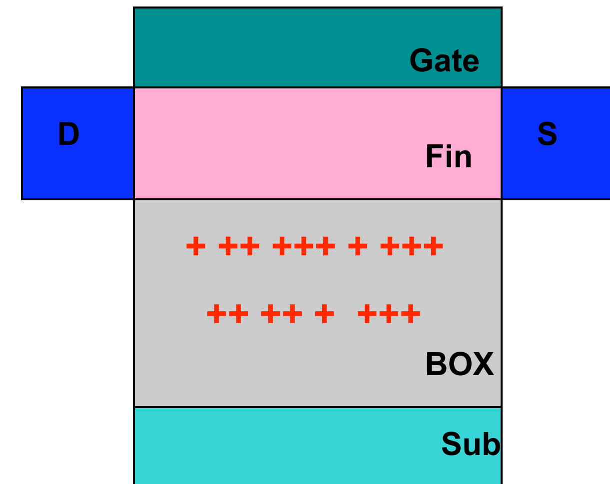
Fin Width ↑

0 100 200 300 400 500

0 10 20 30 40

ANNEALING EXPERIMENTS





The positive shift of the I_d-V_{gs} curves during annealing is a signature of the non uniform trapped charge in the BOX.

SUMMARY

- The composite I_d-V_{gs} curves in 20 fins FinFETs is averaging over a large number of fins which induces better slopes quality whereas a non uniform SS is obtained for 2 fins samples where the variability from fin to fin is affecting the maximum the device's behavior.

- FinFETs with wider fin width (80 nm) behave more like planar devices with larger threshold voltage shifts and greater subthreshold swings.

- The lateral-gates in narrower fin width devices, control the surface potential at the back interface (fin-BOX), reducing the impact of both the vertical coupling effect and the fringing fields originating from the drain terminal.

- Annealing at room temperature of irradiated FinFETs confirm that the observed stretch-out in the SS curves for wider devices is due to non-uniform radiation-induced oxide trapped charge.

FUTURE WORK

- Study the fin width dependence in irradiated P-channel FinFETs (if time permits).

- Use more convenient models (with parameters closers to the actual FinFETs parameters used in this work) to simulate the number of fins's impact on the I_d-V_{gs} curves.

Thanks