The Effects of Angle of Incidence and Temperature on Latchup in 65nm Technology

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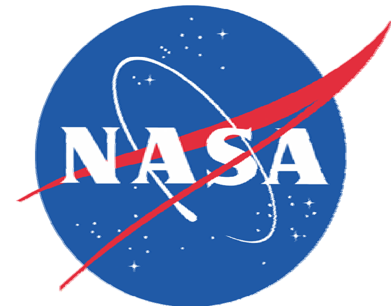
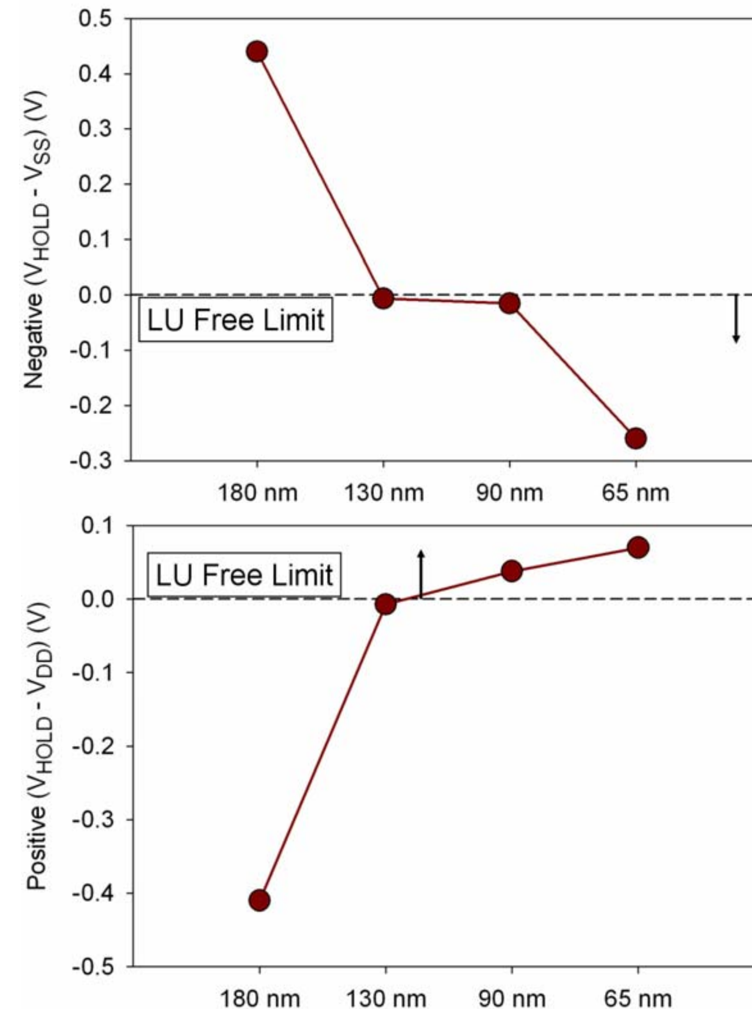


Overview – Moving Forward of Testing for Latchup in Deep Submicron Devices (NSREC '07)

- Current testing procedures for latchup
  - Test at normal angle then rotate to grazing angle along a single axis
  - Test at one or two temperatures
- Simulations in this work show
  - The orientation of grazing angle strikes can significantly impact device response
  - Temperature can determine whether the device is physically capable of entering the regenerative latchup state

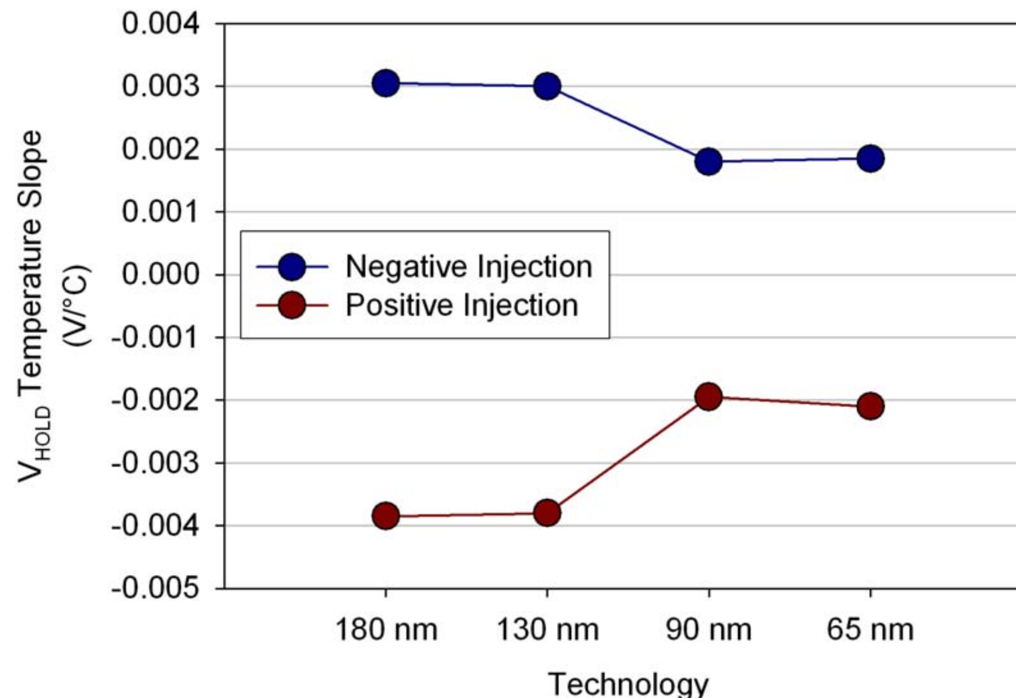
Scaling Effects on SEL – Holding Voltages

- If holding voltages are greater than what the power supply can provide, the device cannot latch
- Reduction in latchup sensitivity for newer technologies is expected to be due to a decrease in operating voltages
- Boselli shows (right) that for experimental Texas Instruments technologies, the 90 nm and 65 nm devices with minimum design rule spacing are LU free at room temperature



G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective," presented at International Reliability Physics Symposium, San Jose, CA, 2005.

Scaling Effects on SEL – Holding Voltage Variation with Temperature



- Increasing temperature causes resistances and bipolar gains to increase, resulting in reduced holding voltages
- Boselli shows changes in holding voltages due to temperature increases
  - Predicts immunity to SEL for 90 nm technology below ~320 K
  - ***Predicts immunity to SEL for 65 nm technology below ~340 K***

G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective," presented at International Reliability Physics Symposium, San Jose, CA, 2005.

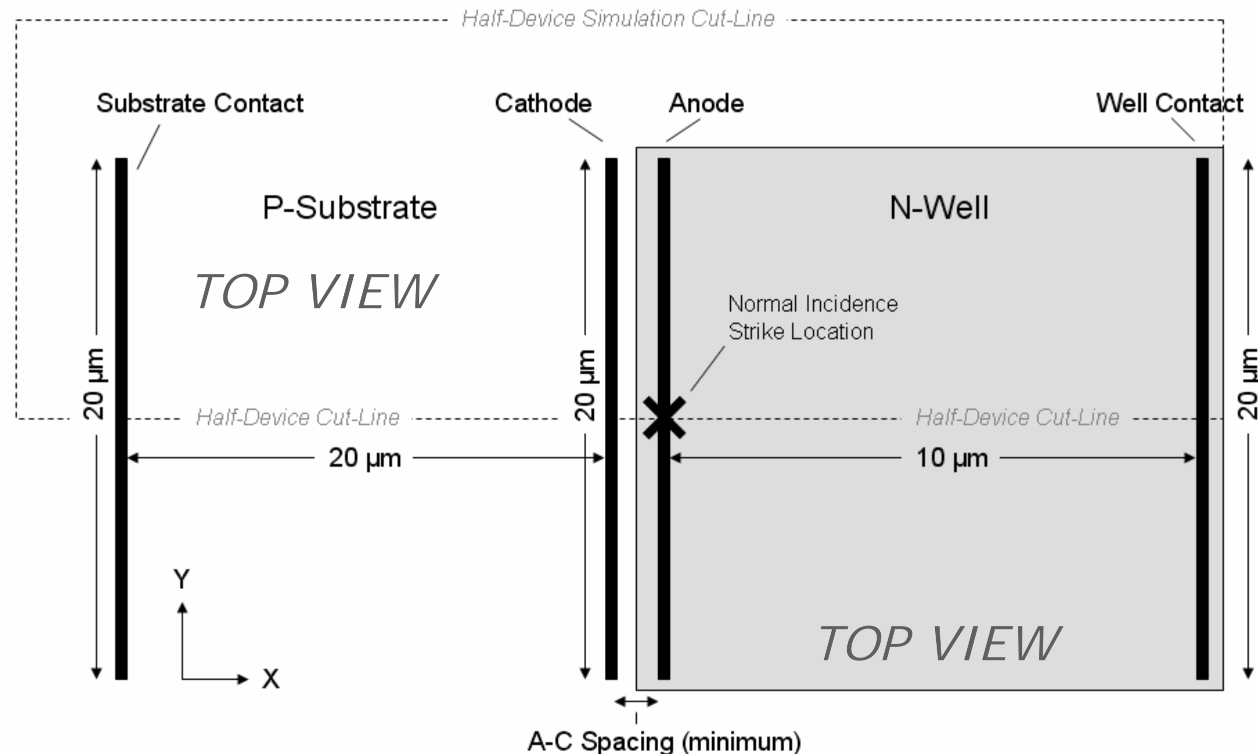
Devices: 2D for Parameter Calibration

SiO$_2$ SiO$_2$
N-Well
P-Substrate
N-Type
P-Type
Most Sensitive Region for Latchup!*
Y
X

- Profiles extracted from TI process emulation TCAD output
- Recombination is key! Varied using two parameters:
  - Surface recombination velocity (surface recombination)
  - Carrier lifetimes (bulk recombination)

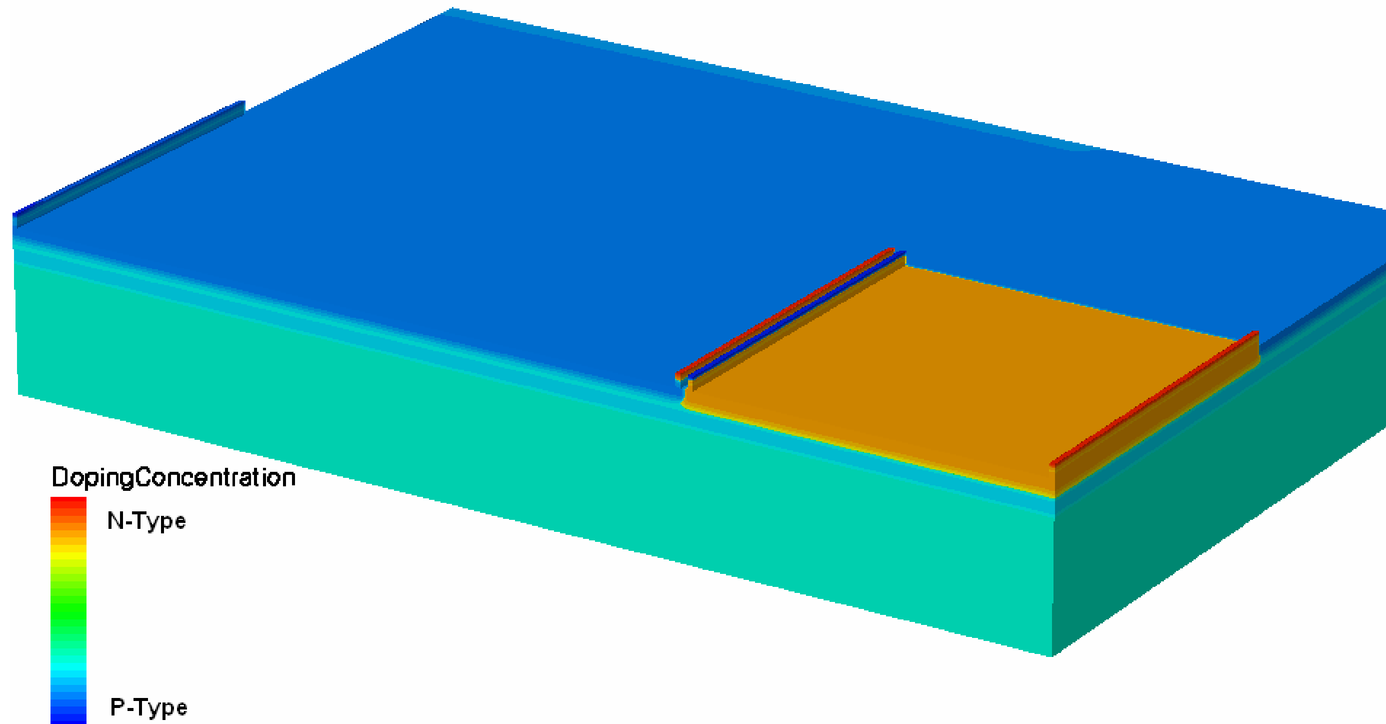
**A.H. Johnston and B.W. Hughlock, "Latchup in CMOS from single particles," IEEE Transactions on Nuclear Science, vol. 37, no. 6, pp. 1886-1893, 1990.*

3D Device for SEL Testing



- Solution to large device size: Use symmetry
  - Use half device with area for current spreading to reduce resistance
  - Use symmetry in DC and SEL tests
  - Restriction: results only reliable with strikes along x, y, z basis vectors!

3D Device for SEL Testing



- Solution to large device size: Use symmetry
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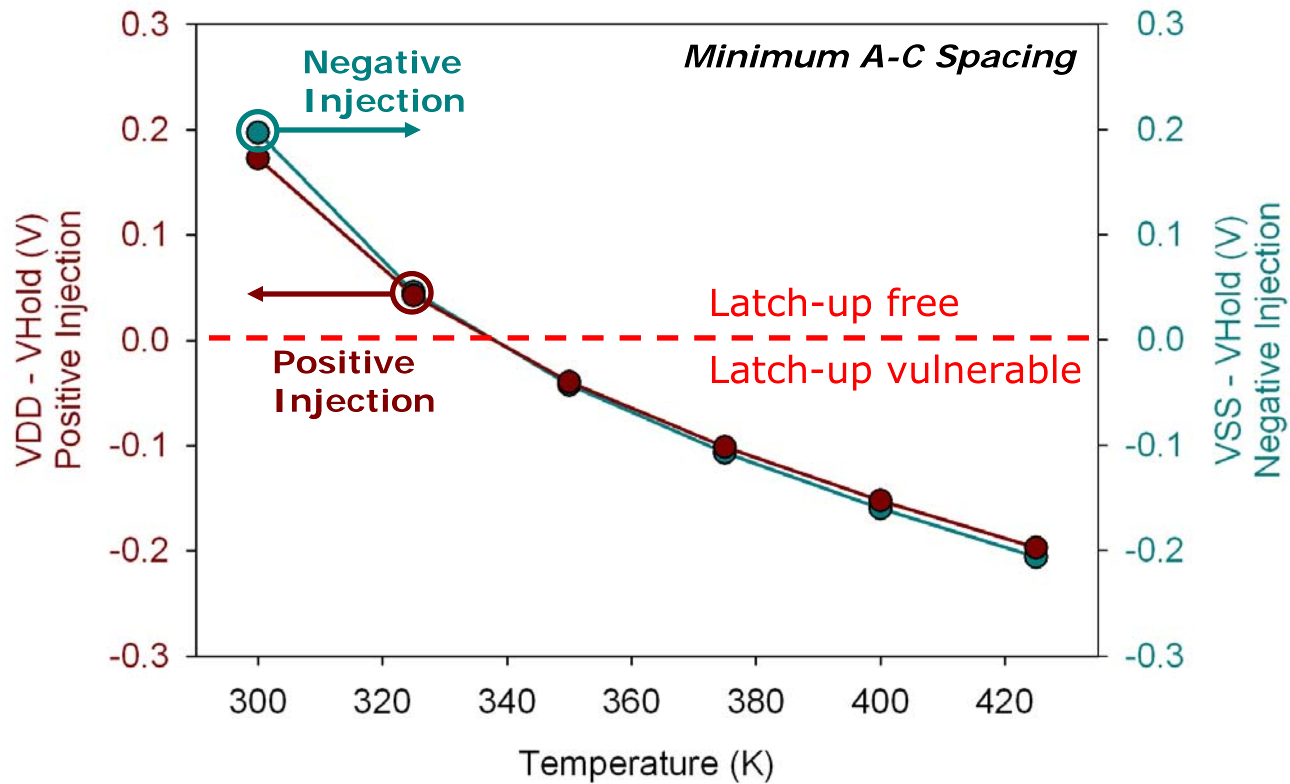
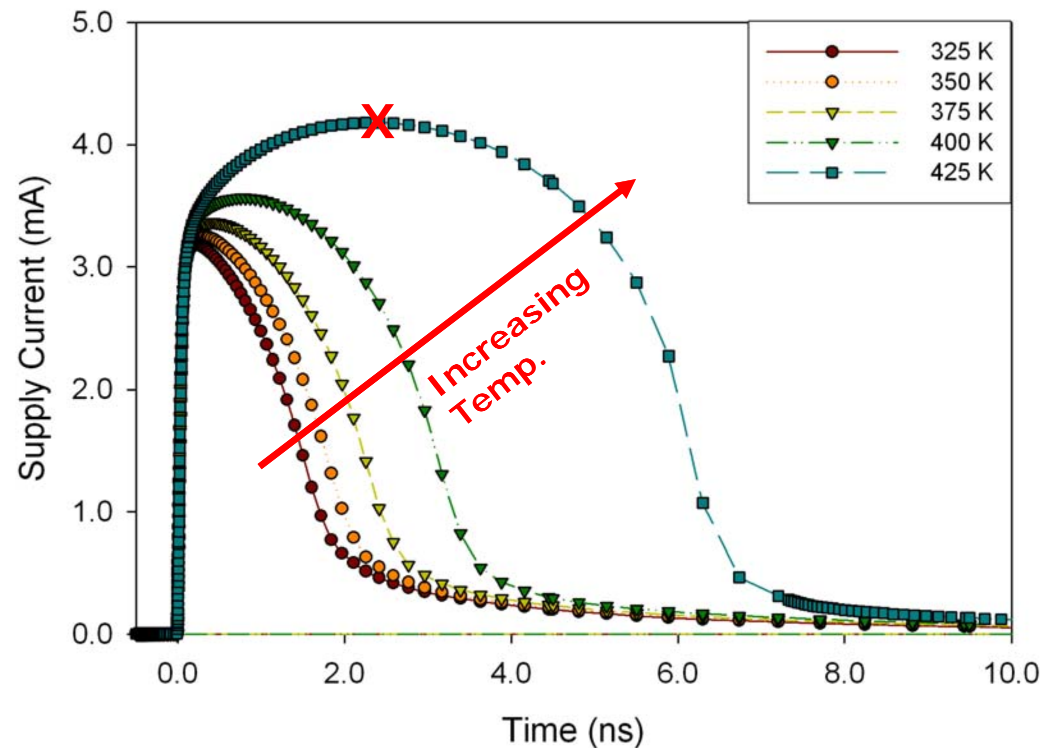
Simulation: DC Holding Voltages



- Increasing temperature increases device vulnerability due to increase in β's and increasing resistances.

With advanced technologies, temperature can determine latchup susceptibility/immunity

Simulation: Normal Incidence Strikes at Varying Temperature



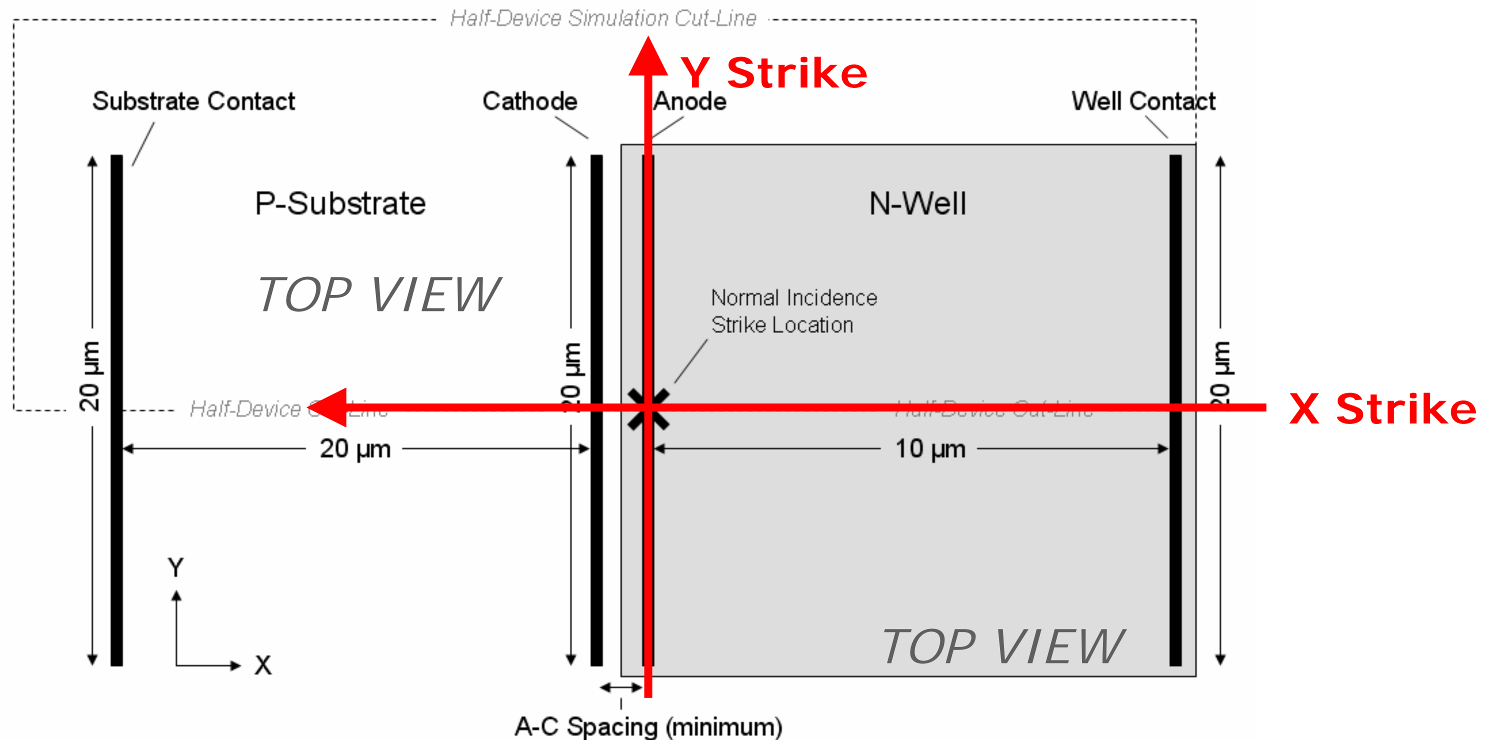
- 80 MeV-cm^2/mg ion strikes at normal incidence and t=0
- Supply current at tied N-well/P-anode contact plotted
- Structure does not latch up even at high LET and high temperature

Simulation: Normal Incidence Strikes at Varying Temperature

Electrostatic Potential
1.2
0.5

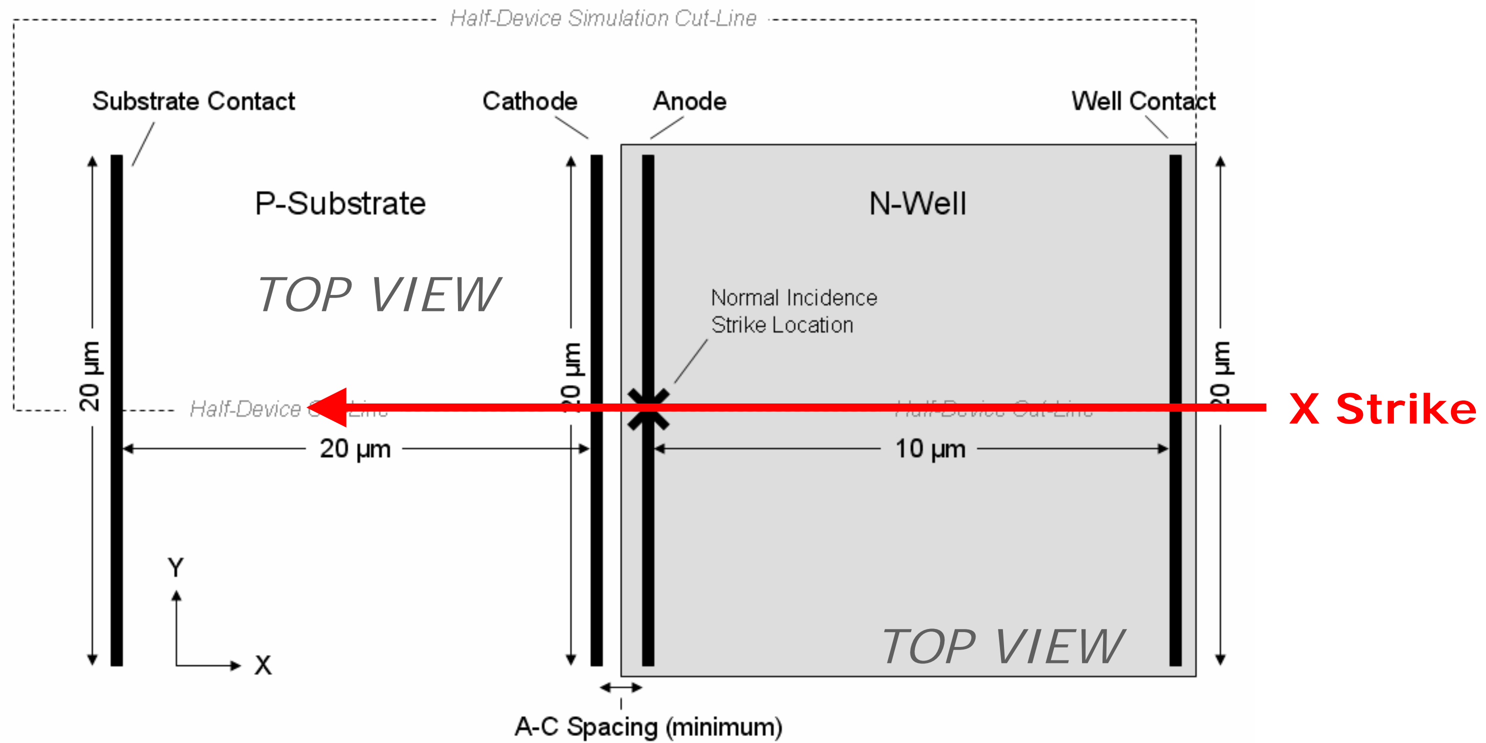
- Investigation of potentials at 425 K at transient peak shows majority of N-well/P-substrate junction in favorable latch-up condition
- Device *almost* latches, but 80 MeV-cm^2/mg is not quite enough (90 LET is)

Simulation: Grazing Angle Strikes

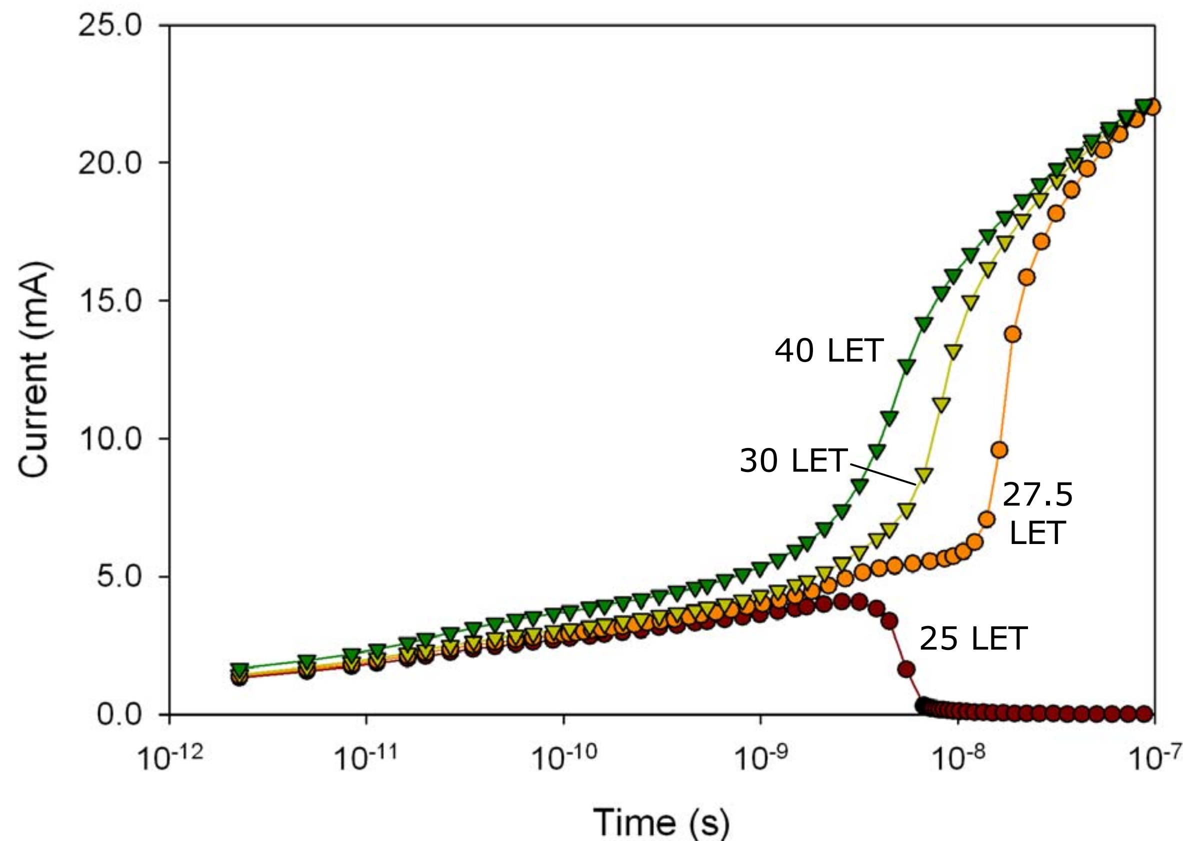


- Tests done for strikes in two grazing directions
- Symmetry used in both cases to reduce simulation volume
- More charge deposited in the N-well with due to large segment of path in N-well
- Y direction strike should be most vulnerable

Simulation: X-Direction Grazing Angle

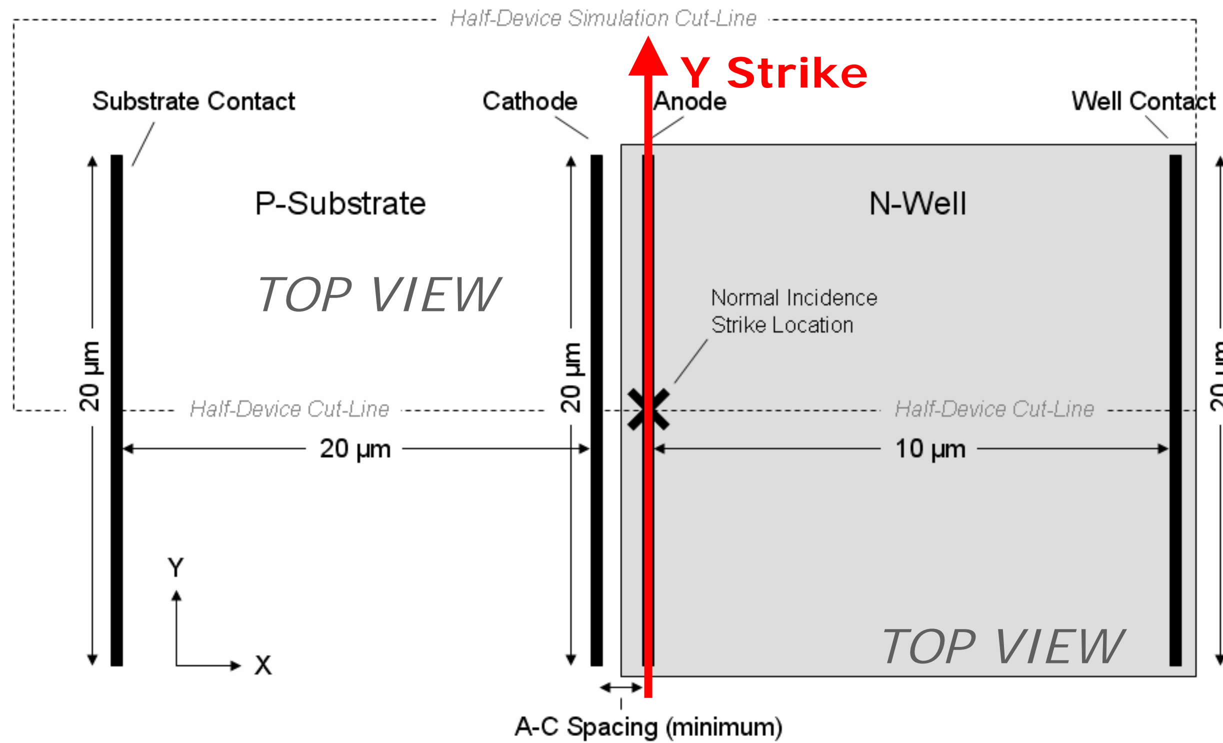


Simulation: X-Direction Grazing Angle

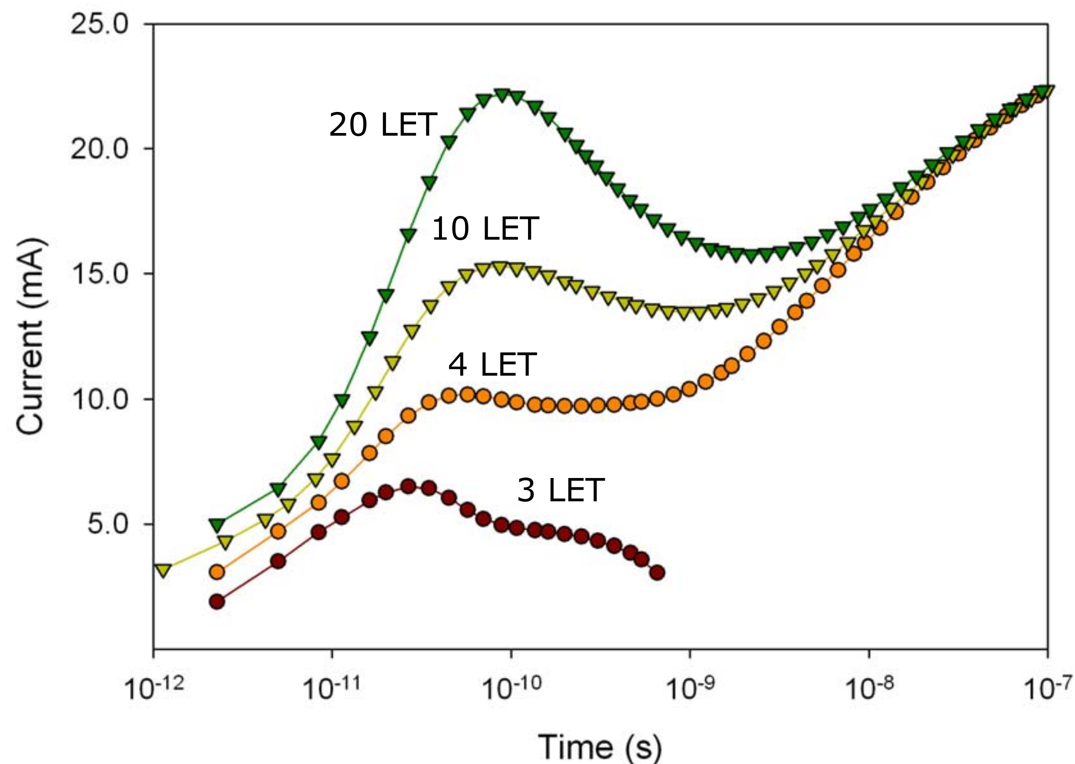


- Results are shown at 425 K with ion strikes at t=0
- Latching time for x-direction strikes is long – most of the charge has to move to the anode

Simulation: Y-Direction Grazing Angle

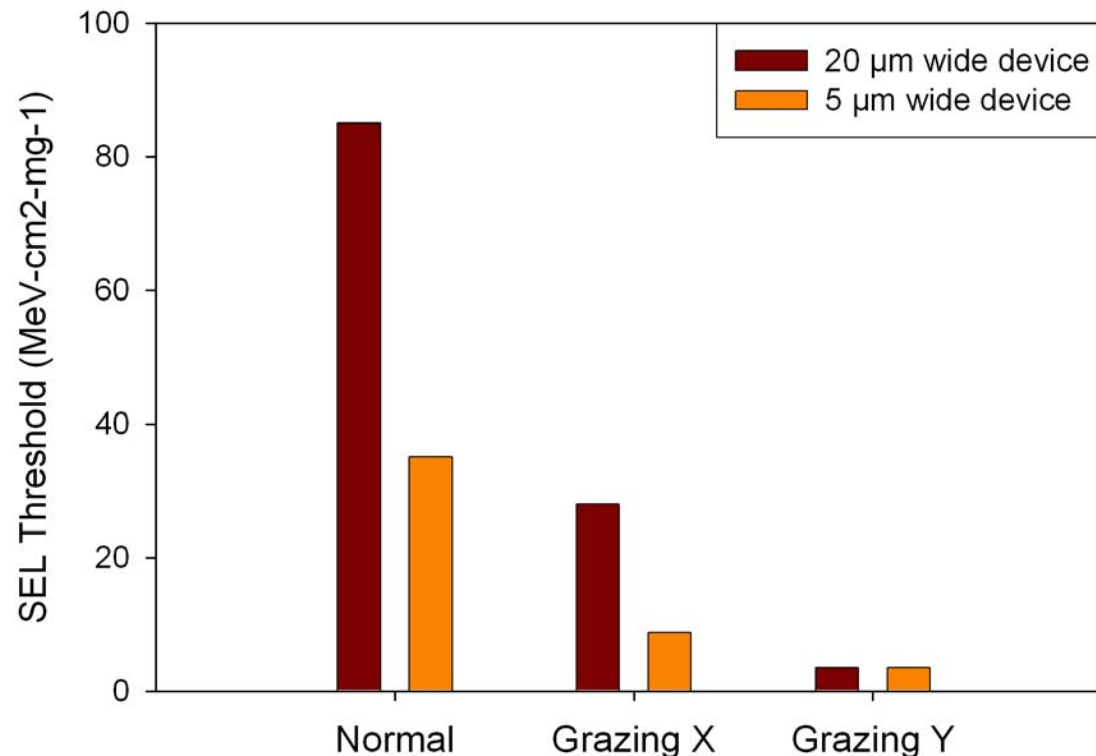


Simulation: Y-Direction Grazing Angle



- Device is far more sensitive to charge deposited directly under the anode
- Optimal placement of charge allows for potential drop in N-well directly under the anode and near the N-Well/Substrate junction

Simulation Results: Angular Effects

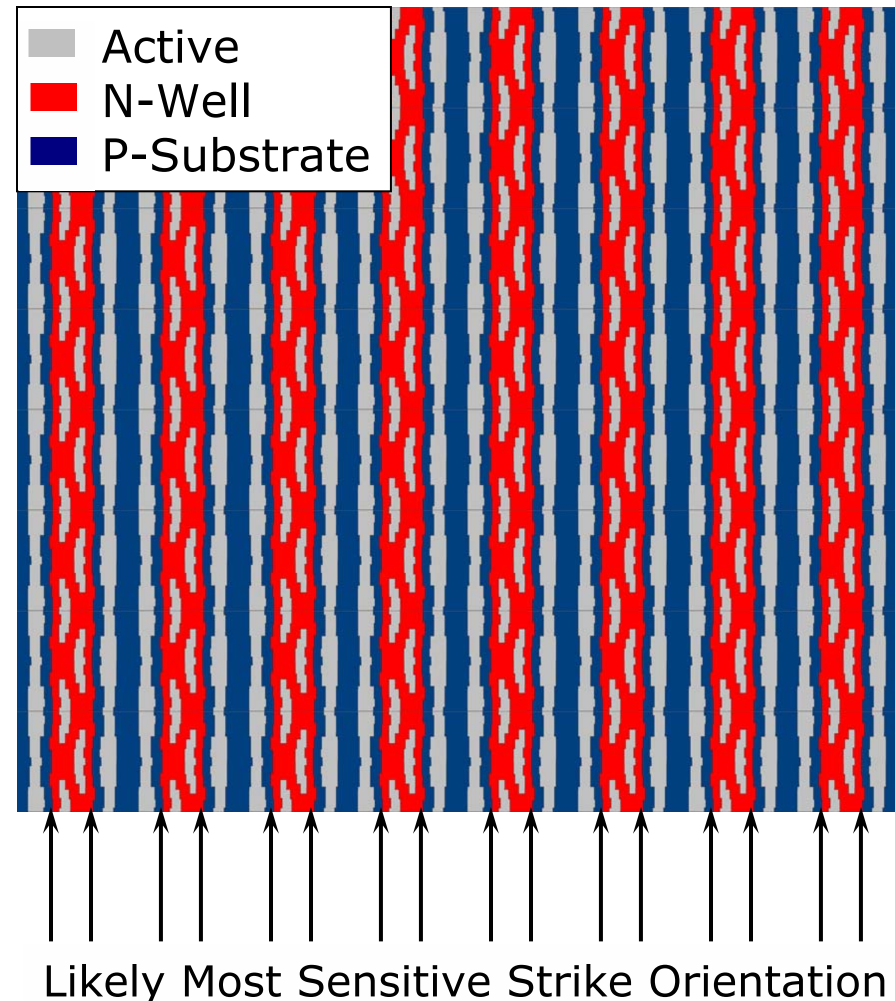


- Smaller device more sensitive to strikes that are not oriented along most sensitive region
- Significant difference in sensitivity due to angle in both devices

Potential Issues w/ JEDEC Standard SEE Testing

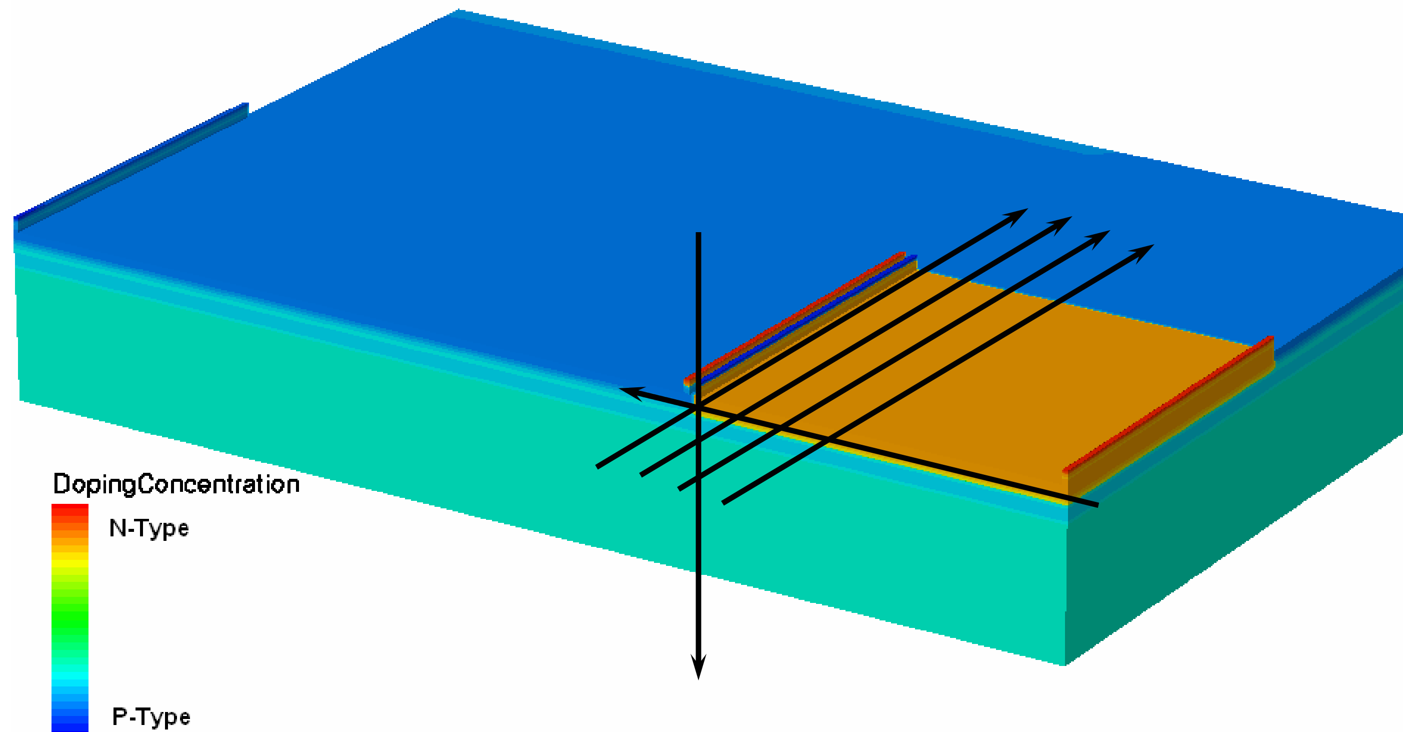
- For ions Z ≥ 2
- Suggests maximum environment temperature and maximum voltage for SEL tests
- Suggests tests at grazing angles of 60° or more from normal
- Does *not* specify the orientation of the grazing angle

- Simulations have shown increased sensitivity to strikes oriented along the N-Well/P-Substrate junction
- Typical SRAMs likely have a preferred sensitive direction



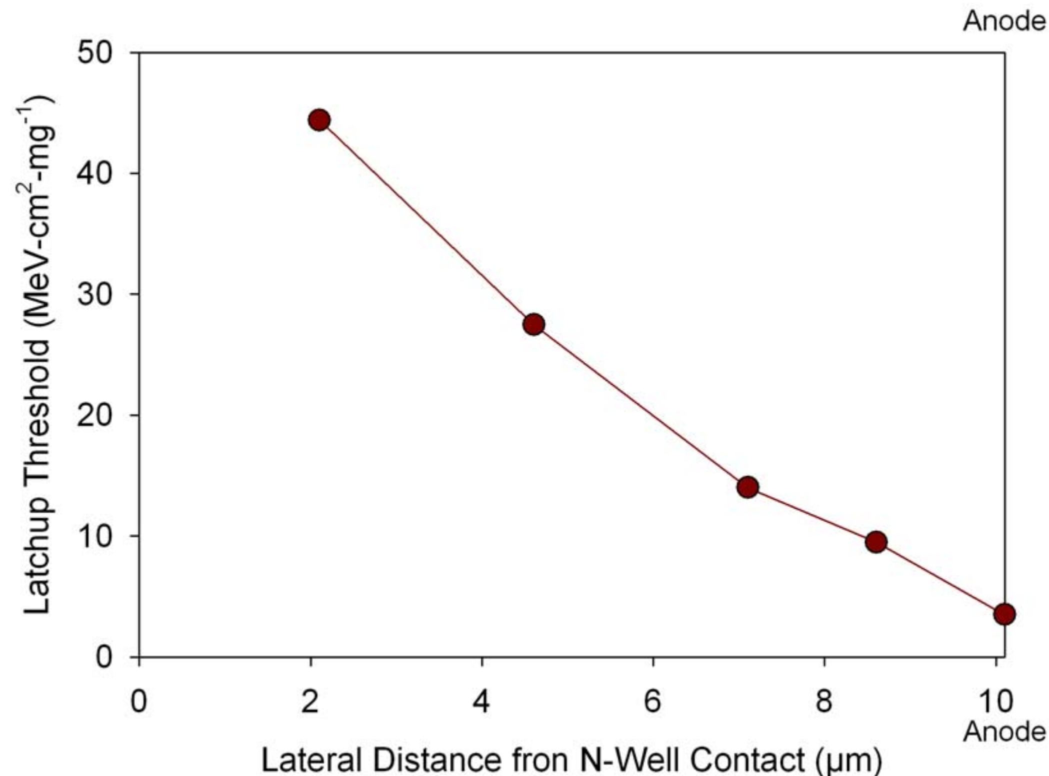
JEDEC Standard JESD57, http://www.jedec.org

Recent Work - Sensitive Volume Profile of ESD Device



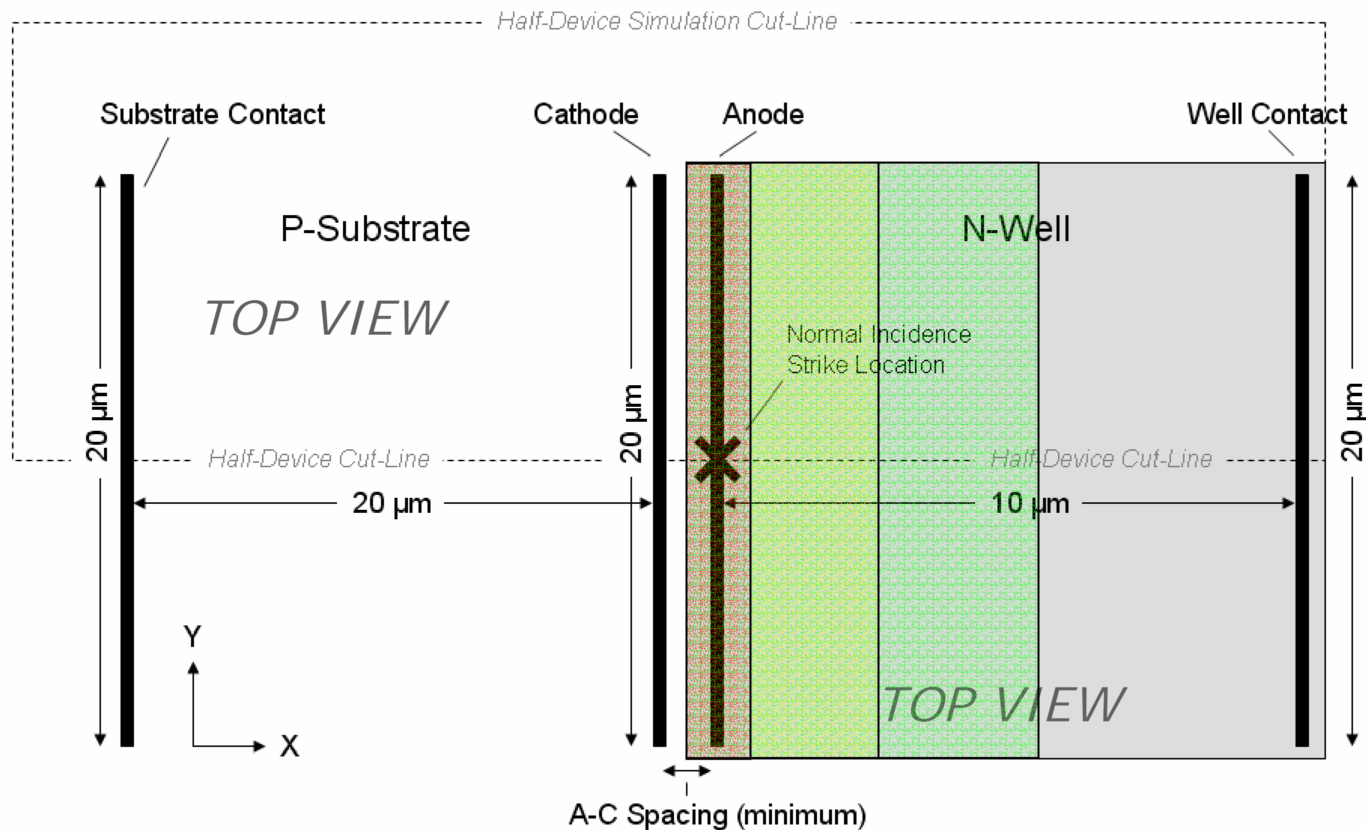
- Information from simulated strikes will be used to create a sensitive volume structure for the ESD device
- Additional Y-direction strikes will give a profile of the device sensitivity between the well contact and the anode

Recent Work - Sensitive Volume Profile of ESD Device



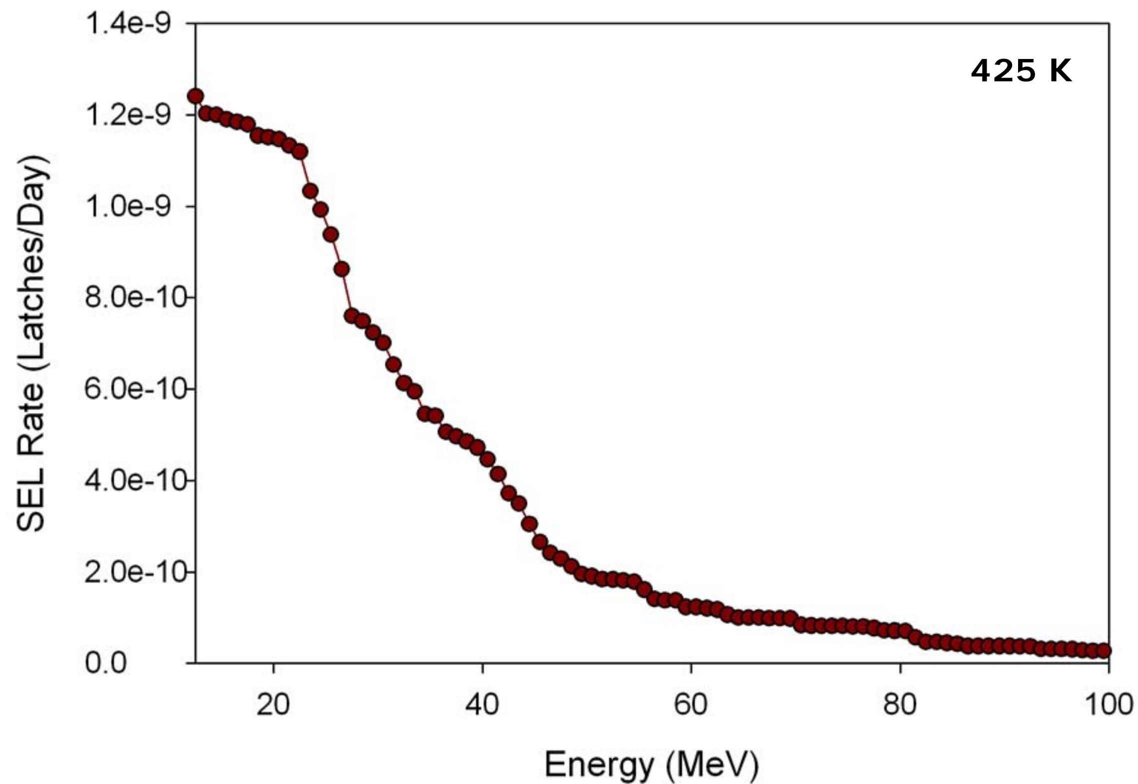
- Simulations show what would be expected from Johnston’s work
- Profile helps define weighting of sensitive volumes in MRED computations

Recent Work - Sensitive Volume Profile of ESD Device



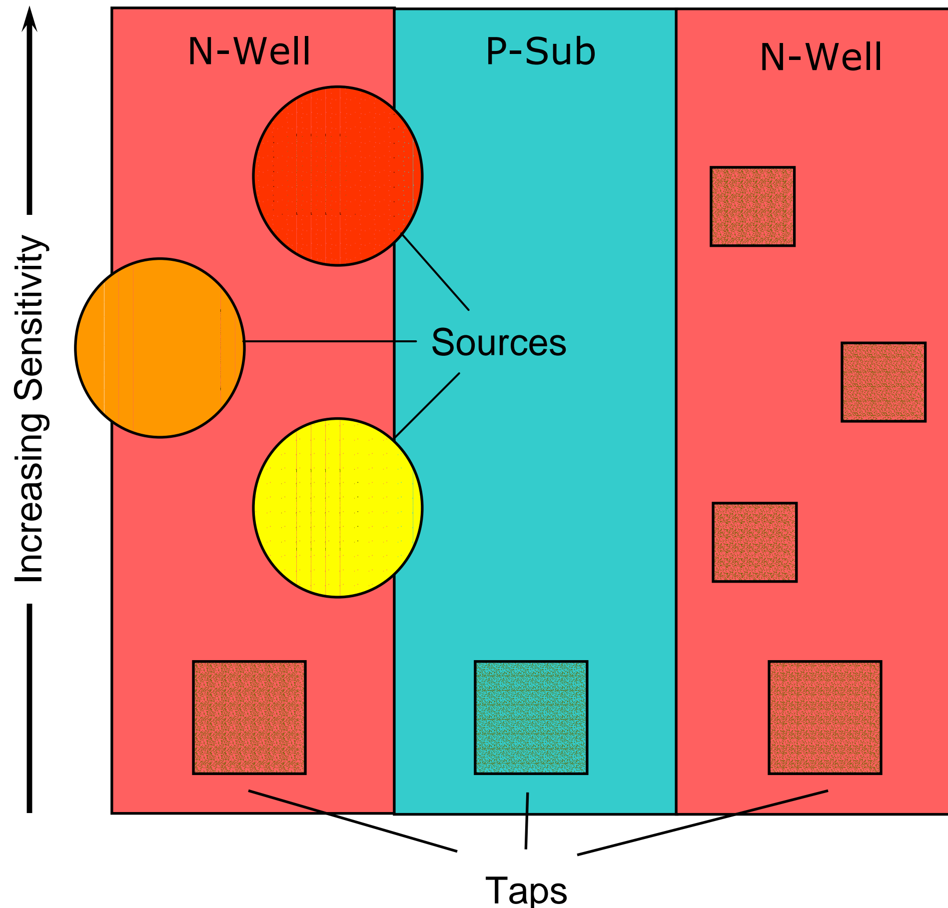
- Using information from original X-direction strike, single events will be checked for a minimum amount of energy in the N-well
- Additional weighted volumes are added based on other TCAD Y-direction strike thresholds

SCR Device Potential-Latching Event Rate



- Solar-min environment 100 mils shielding
- Error rate for single SCR device
- Minimum cut-off energy at 12.5 MeV

SRAM SEL Rate Simulation Basics



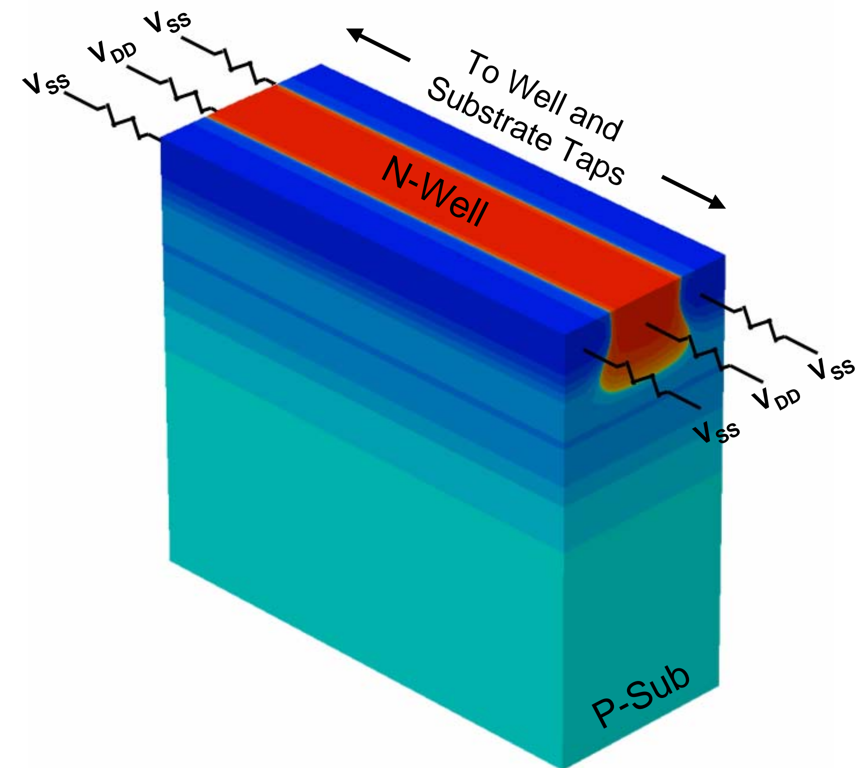
TI SRAM Sources and Taps Layout

Sensitive Volume Definition Guidelines

- First pass uses only P-sources and N-well as sensitive areas
- Sensitivity increases with distance from well contacts
- Sensitivity increases with proximity to P-sources
- Sensitivity increases with proximity to N-well/P-substrate junctions near P-sources (Circles)

Moving to a New Model - Simulation of Potential Drop in N-Well

- Uses section of N-Well column with surrounding substrate
- Variable resistances placed to simulate varying distances from taps
- Ion strikes can be simulated with varying LET and angle.
- Potential drops ≥ 0.7 V will be mapped to position and LET of strike to create a model



Conclusions

- Current and previous angle of incidence tests only rotate on one axis. Rotation on two axes should be used to fully characterize the response
- Temperature will play a large role in the impact of latchup for current deep submicron technologies
  - Temperature changes in previous works have been shown to change cross sections for latchup. Temperature is now likely to determine whether latchup is observed at all in deep submicron devices.
- SEL sensitivity should be modeled based on potential drops caused by charge deposition. This is different from SEU which is usually modeled based on charge collection.

Upcoming Work/Milestones

- NASA test boards for TI SRAMs received 10/16. Debugging is underway. Next available testing window 10/23 – 10/24
- Development of mathematical model for potential drop based on energy deposition, position in SRAM, and temperature
- Implementation of model in MRED to compare SEL rates with NASA proton testing
- Experimental results and MRED simulations to determine the impact of varying angles of incidence on SEL