Single Event Latchup in 65 nm CMOS SRAMs

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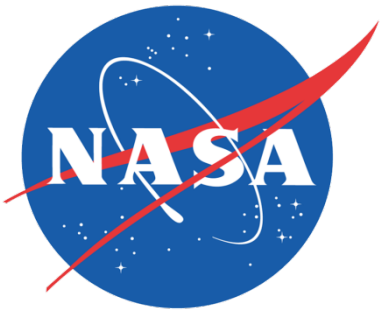
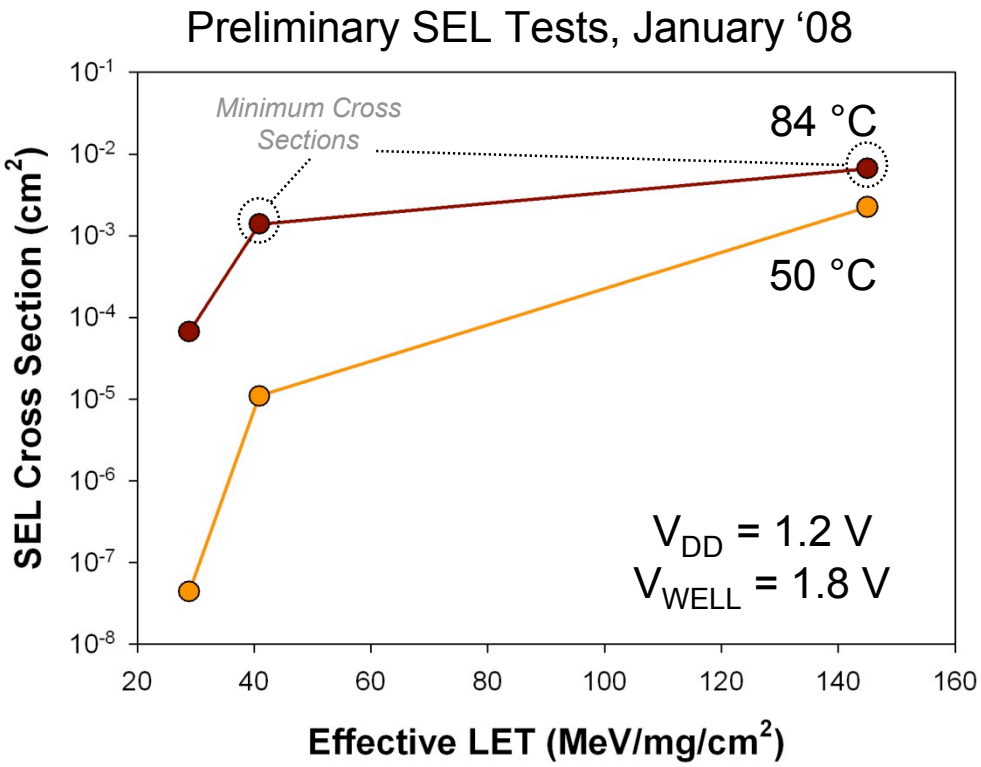


TI 65 nm SEL Project Goal

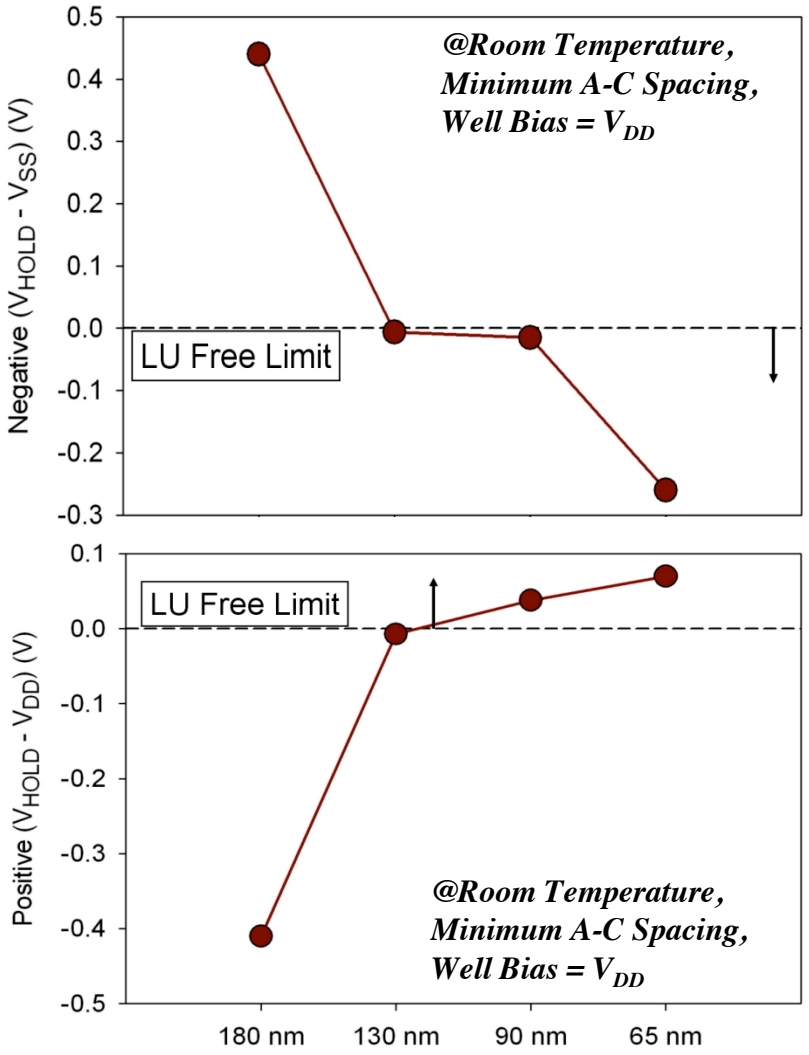
- Understand the sources and mechanisms of SEL in a deep submicron technology for the purpose of engineering a predictive technique for SEL rate
  - Experimental work to provide both a technical foundation and validation of predictive techniques
  - TCAD simulations to provide a sensitivity map of the device layout based on potential SEL triggering events
  - Validate model on existing ion SEL data
  - Development of model and results of model should lead to insight into angular, temperature, and biasing effects for SEL



Latchup observed in a 65 nm commercial test part!

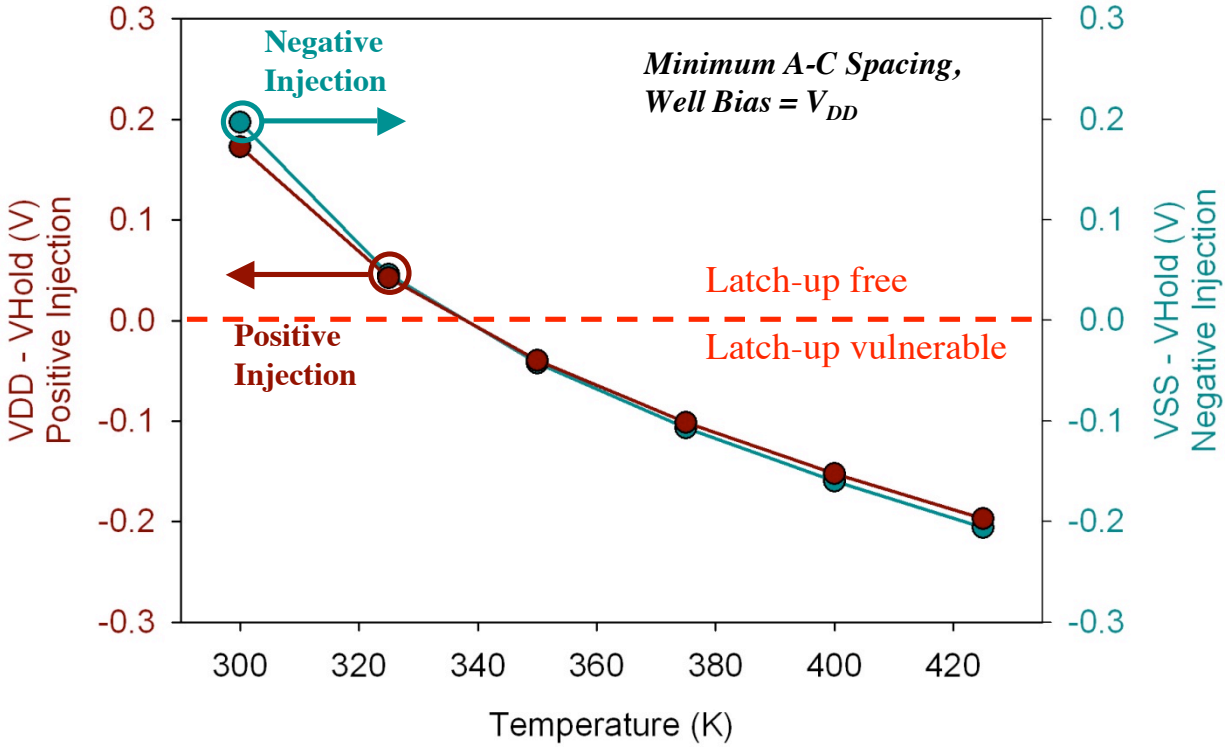
Scaling Effects on SEL – Holding Voltages

- If holding voltages are greater than what the power supply can provide, the device cannot latch
- Reduction in latchup sensitivity for newer technologies is expected to be due to a decrease in operating voltages
- Boselli shows (right) that for experimental Texas Instruments technologies, the 90 nm and 65 nm devices with minimum design rule spacing are LU free at room temperature



G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective," presented at International Reliability Physics Symposium, San Jose, CA, 2005.

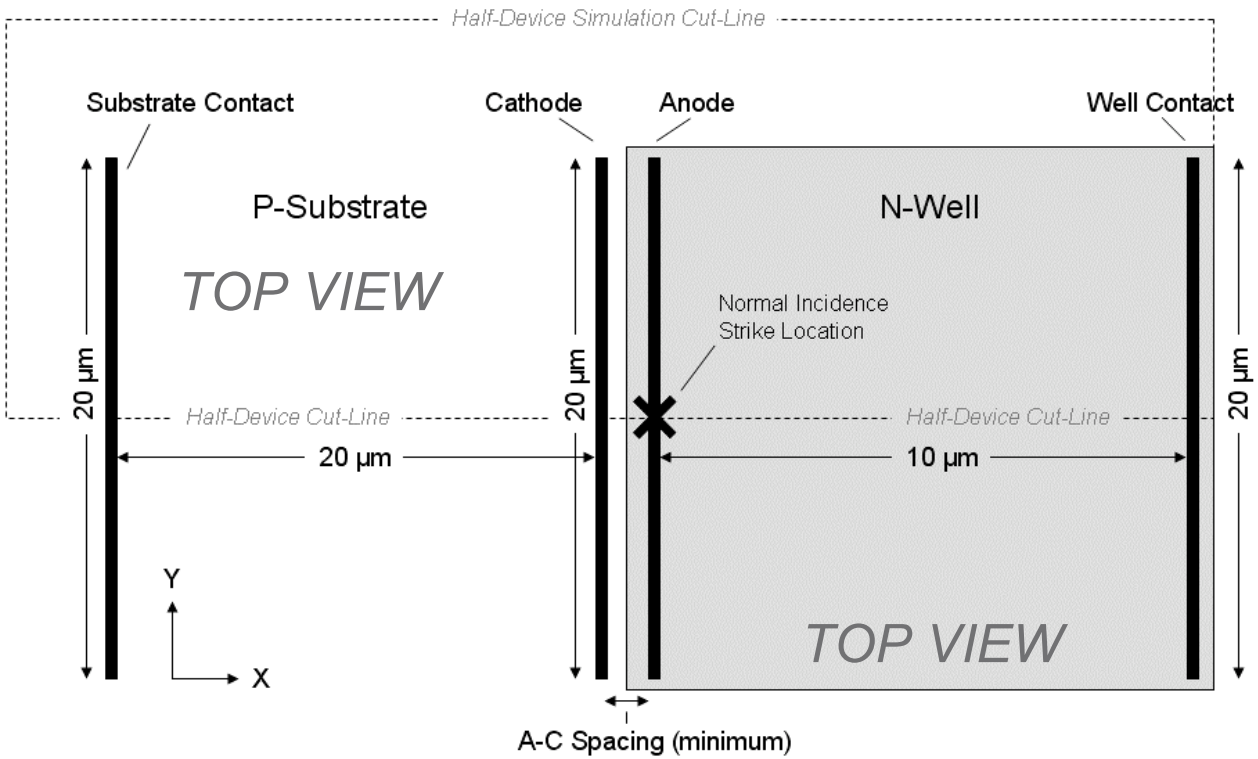
Scaling Effects on SEL – Holding Voltage Variation with Temperature



- Increasing temperature increases device vulnerability due to increase in β's and increasing resistances.

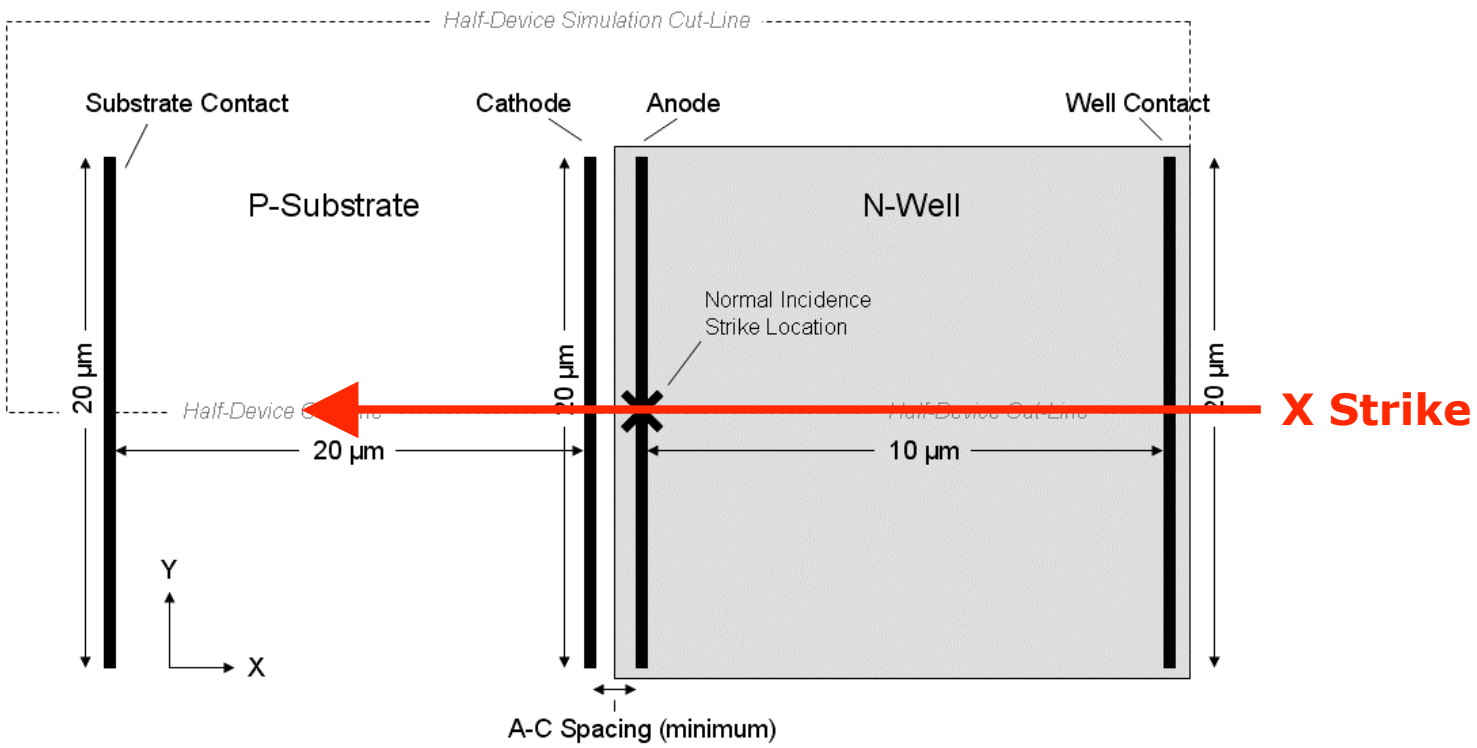
With advanced technologies, temperature can determine latchup susceptibility/immunity

3D Device for SEL Simulations

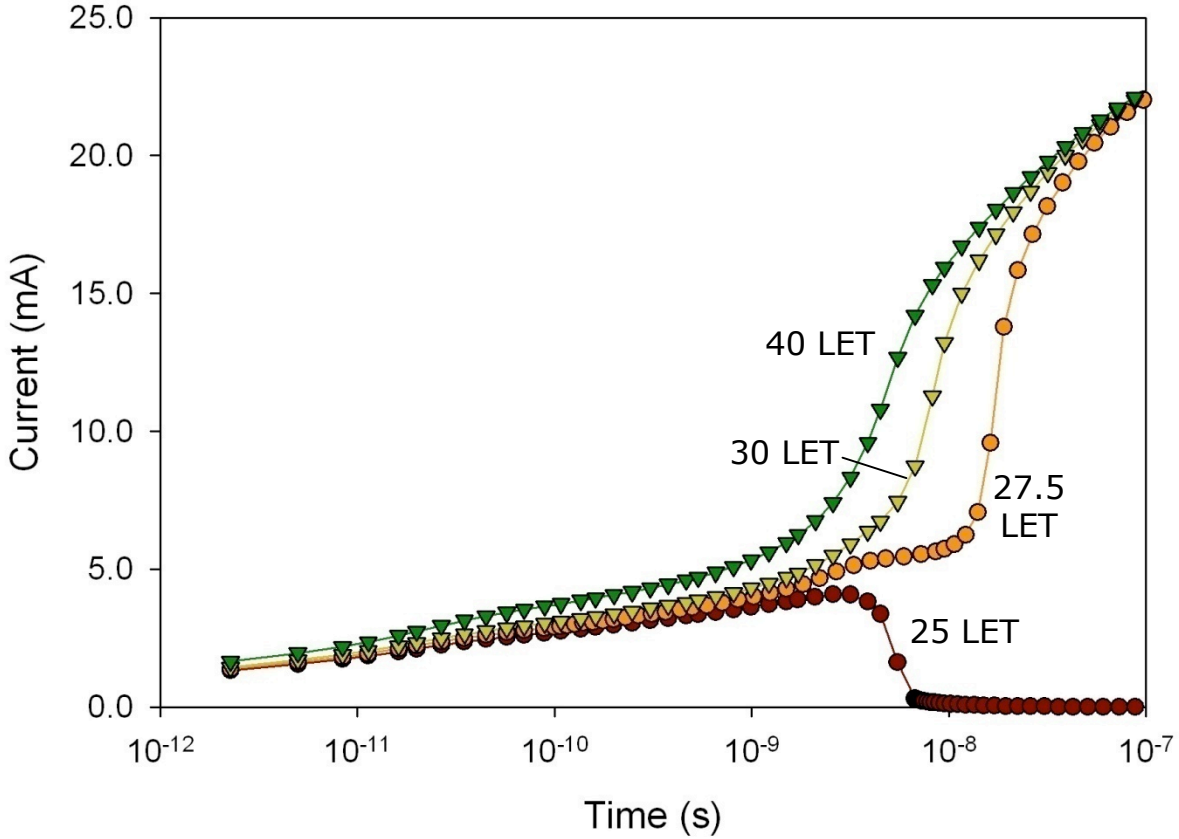


- Solution to large device size: Use symmetry
  - Use half device with area for current spreading to reduce resistance
  - Use symmetry in DC and SEL tests
  - Restriction: results only reliable with strikes along x, y, z basis vectors!

Simulation: X-Direction Grazing Angle

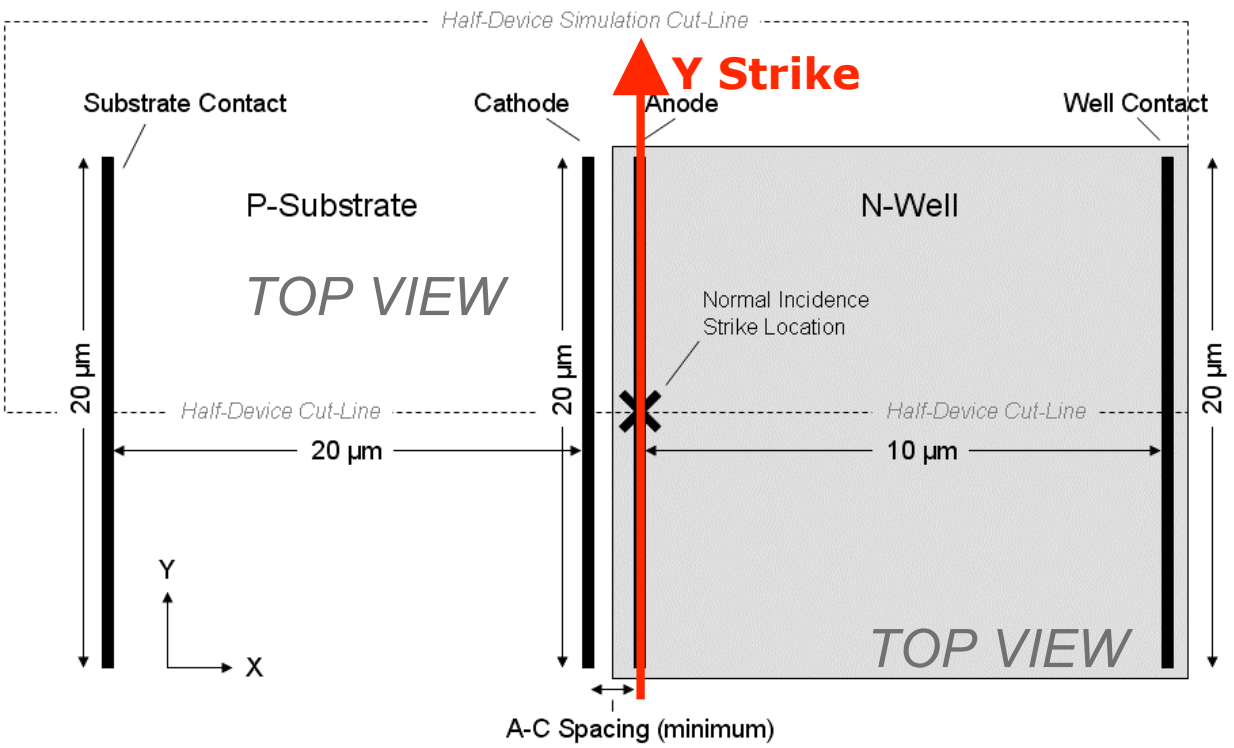


Simulation: X-Direction Grazing Angle

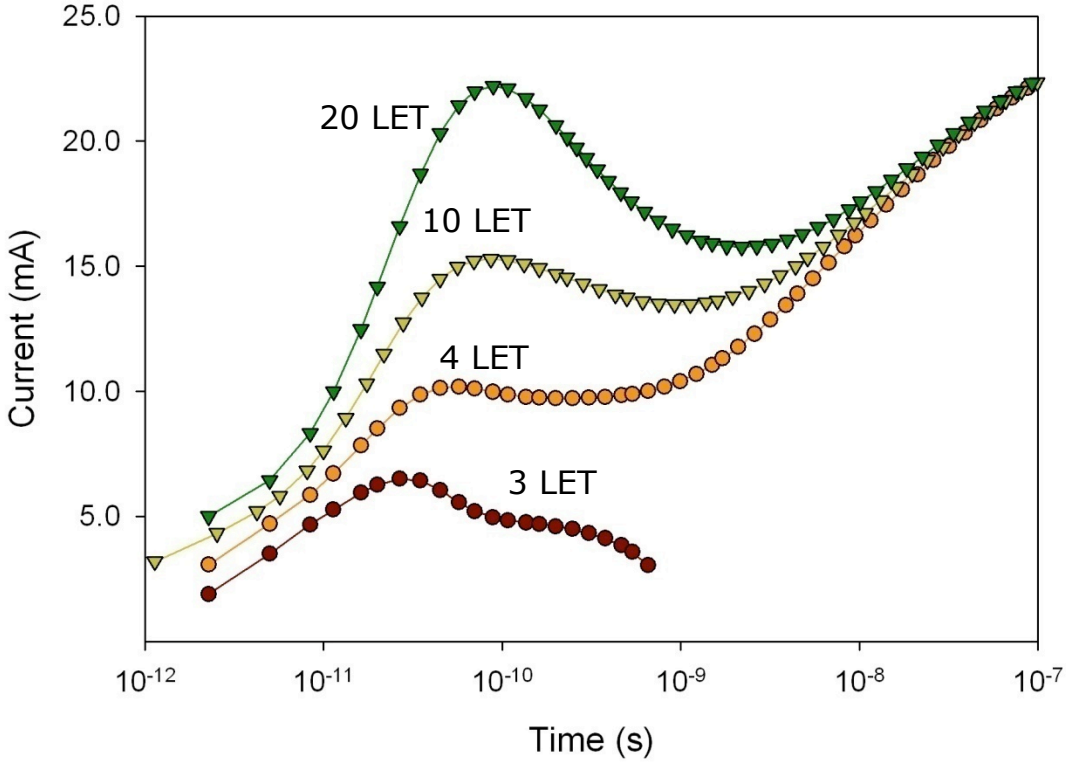


- Results are shown at 425 K with ion strikes at t=0
- Latching time for x-direction strikes is long – most of the charge has to move to the anode

Simulation: Grazing Angle Strikes



Simulation: Y-Direction Grazing Angle



- Device is far more sensitive to charge deposited directly under the anode
- Optimal placement of charge allows for potential drop in N-well directly under the anode and near the N-Well/Substrate junction

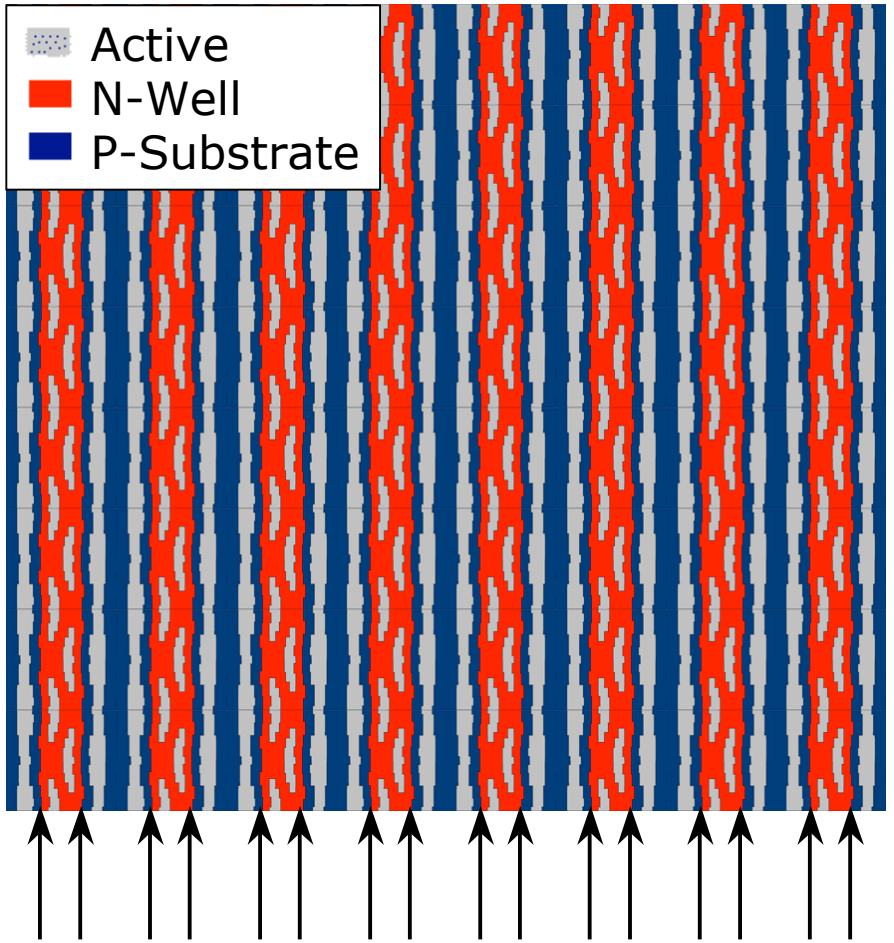
Potential Issues w/ JEDEC Standard SEE Testing

- For ions Z ≥ 2
- Suggests maximum environment temperature and maximum voltage for SEL tests
- Suggests tests at grazing angles of 60° or more from normal
- Does *not* specify the orientation of the grazing angle

- Simulations have shown increased sensitivity to strikes oriented along the N-Well/P-Substrate junction
- Typical SRAMs have a preferred sensitive direction

JEDEC Standard JESD57, http://www.jedec.org

Typical High-Density SRAM Layout



Likely Most Sensitive Strike Orientation

Experimental Data

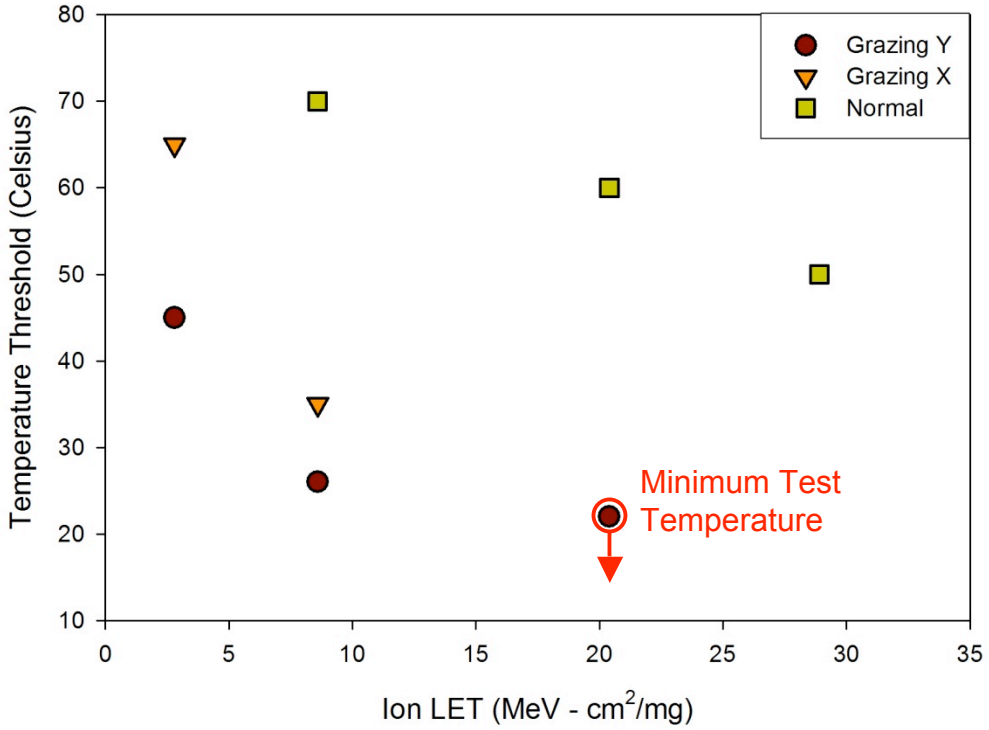
Heavy Ion Tests Feb '08.

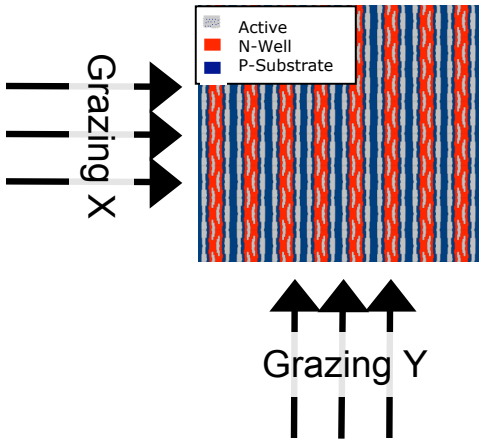
- More detailed tests showing a range of temperatures and energies
- Tests at two perpendicular grazing angles
- One run per temperature/angle/ion at up to $1x10^7$ cm^{-2} fluence or until latch observed
- Threshold LET close to what was found in original 3D TCAD Simulations
- Thermocouple on DUT to maintain chosen die temperatures

65 nm SRAMs

- 8x 1Mbit banks
  - 4x highest-density
  - 2x high-performance
  - 2x other high-density
- V_{DD} = 1.2 V, ***V_{NWELL} = 1.8 V***
- Minimal I/O circuitry @ V_{DD} = 1.2 V
- ***All banks with A-C spacing smaller than '05 Boselli test parts***

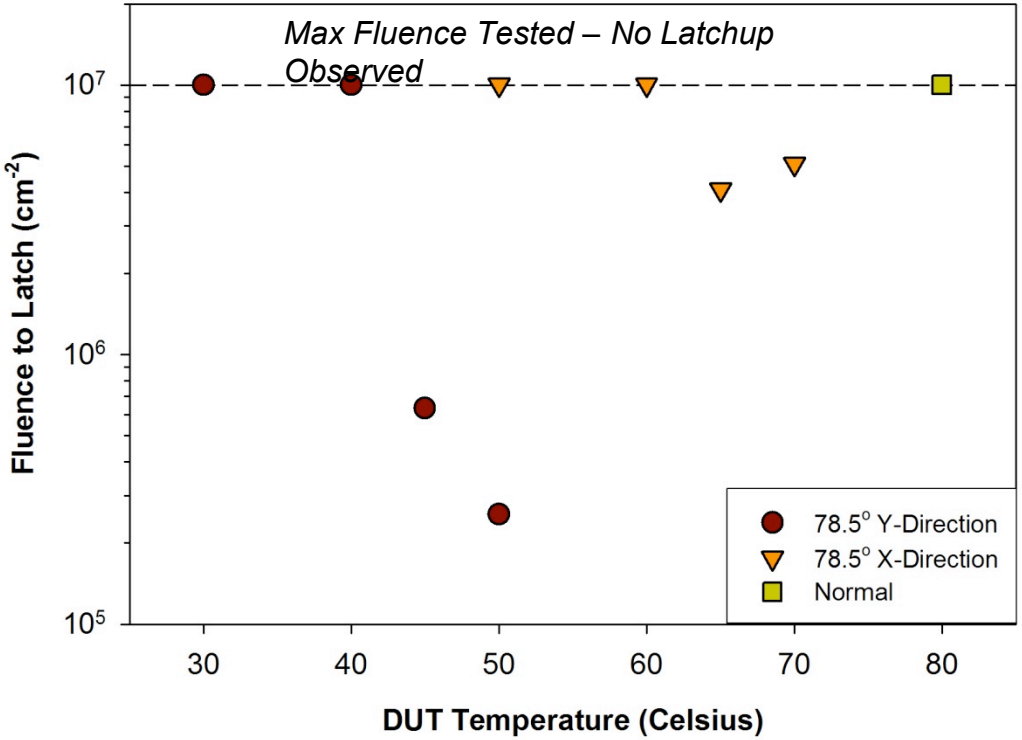
SEL Temperature Thresholds

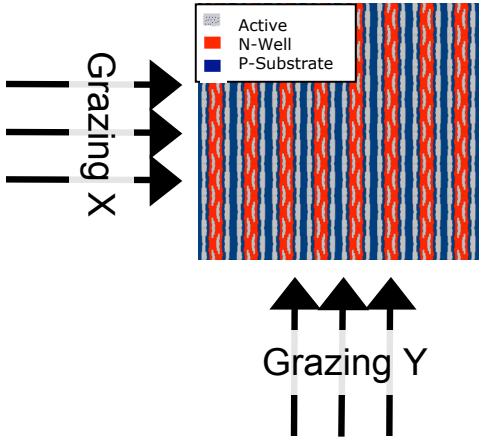




- A total fluence of up to $1x10^7$ cm^{-2} was used at temperatures from 22 °C to 70 °C with four different ions.
- Strikes in the grazing-Y direction are significantly more susceptible to latchup than strikes in the grazing-X direction.

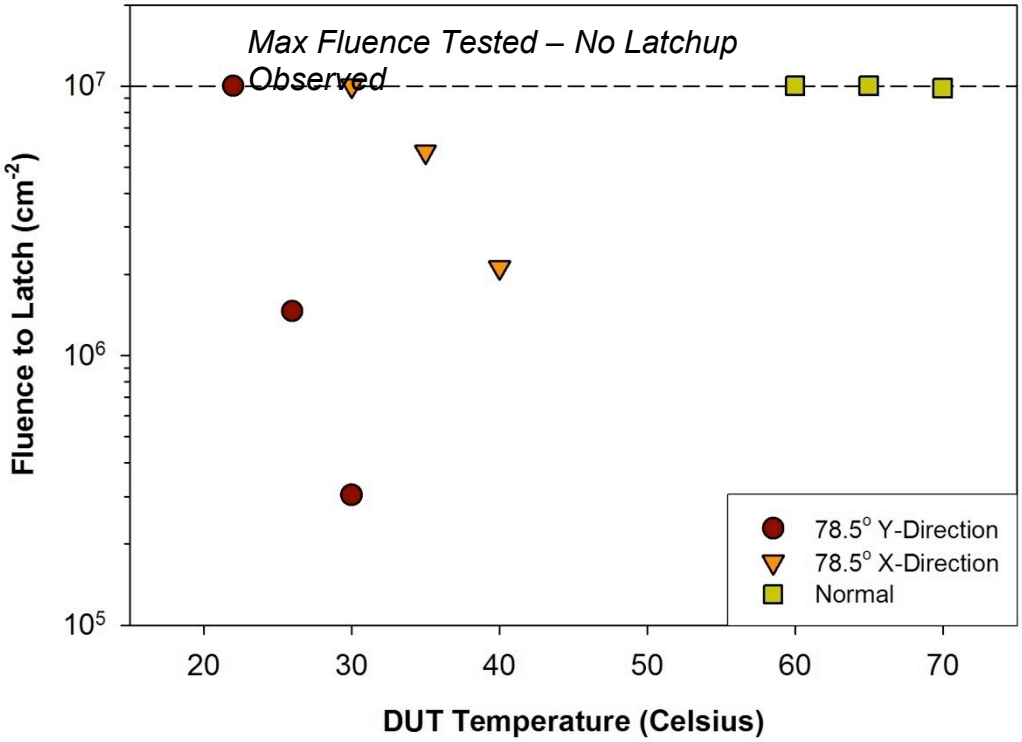
Neon 2.8 MeV-cm^2/mg

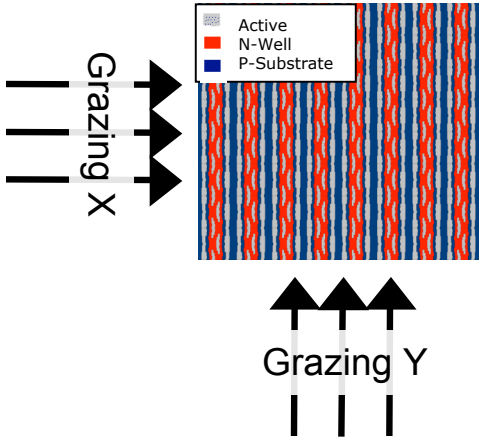




- Grazing-Y direction for ion strikes is more sensitive than the grazing-X direction strikes
- No latchup is observed in the normal incidence tests
- The 2.8 MeV-cm^2/mg neon ions are near the predicted 3.0 – 4.0 MeV-cm^2/mg threshold suggested by simulation

Argon 8.6 MeV-cm^2/mg





- Grazing-Y direction for ion strikes is more sensitive than the grazing-X direction strikes
- No latchup is observed in the normal incidence tests until 70 °C
- Argon ion results reinforce results seen with neon.

Conclusions

- In accordance with simulated single-event latchup, SEL testing shows a difference in both temperature threshold and sensitivity based on the lateral angle of the ion beam.
  - *This must be accounted for when testing devices for latchup, especially in devices that have a repeated layout pattern.*
- SRAMs in these tests show increased susceptibility to latchup compared to the experimental and simulated devices.
  - *Due to spacing below design rules, changes in resistances seen at most sensitive anodes/cathodes, and well biasing at 1.8 V.*

Challenges from Experimental Data and Future Work

- Determine what parts on the test chip are latching up at room temperature through use of laser or IR camera
- Test thoroughly for proton-induced (from secondary particles) SEL due to the low threshold LETs shown
- Gain better statistics for SEL cross section
- Simulate/Understand room temperature latchup high LET
  - Account for spacing below design rule limits
  - Account for different resistance network seen by anode/cathode in SRAM layout
- Use experimental and simulation work to provide a predictive model to tag likely latching events in MRED
- **Graduate in August '08**