Materials stability, band alignment and defects in post-Si CMOS nanoelectronics

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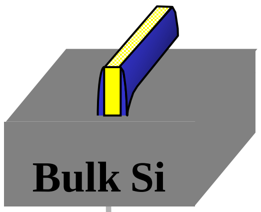
Collaborators: Vanderbilt, Sematech, NIST, NCSU, Stanford, IMEC, UT-A, UT-D, Penn State, UAlbany, UCSB, UCSD, IBM, Intel, AMAT, TI, Freescale…

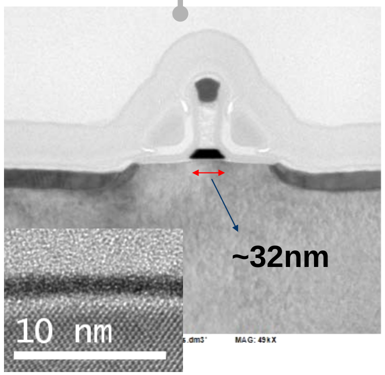
Support: Vanderbilt MURI (AFOSR) and SRC

One vision of the CMOS roadmap

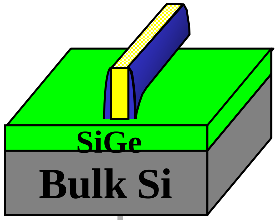
High-k/Metal Gate on Si



Today

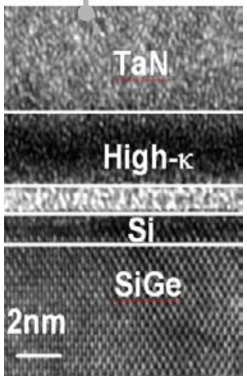


Higher Mobility SiGe or Ge Channel

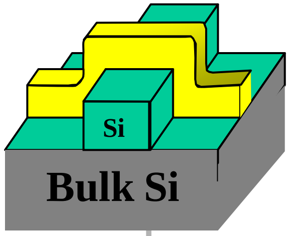


Characterization Issues:

- SiGe-HK Interface
- Damage at p-n in SiGe
- Strain in channel

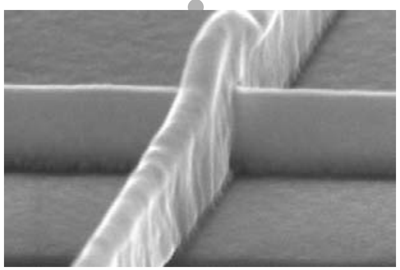


Tri-gate or FinFET

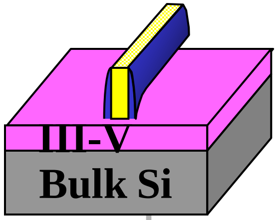


Characterization Issues:

- Sidewall S/D doping
- Sidewall silicidation
- Sidewall etch

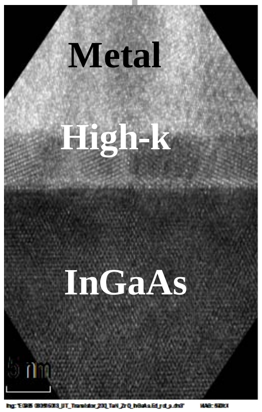


Higher Mobility III-VChannel

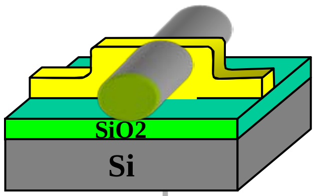


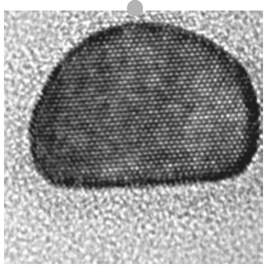
Characterization Issues:

- strain, E_g for III-V on Si
- III-V – HK interface
- Doping



Nanowire Transistor





Sematech

Motivation: Help develop a fundamental understanding and control of radiation induced defects in future CMOS materials.

High resolution experimental studies of high-k on Ge, III-V and other substrates:

- **Composition and depth profiling – XPS, MEIS, RBS, SPM…**
- **Electronic structure – PES, IPE, optical and electrical methods**
- **Surface/interface passivation chemistry and relation to defects**

Summary of work over grant period:

- **Interface passivation and oxide reduction on during high-K deposition**
- **Surface/film analysis of gate stacks exposed to high-energy radiation**
- **Studies of Fermi level pinning and unpinning at oxide-semicond. interfaces**
- **Metal gate – high-K stack interface chemistry and band alignment**

CMOS gate stack activities @ Rutgers

Tools:

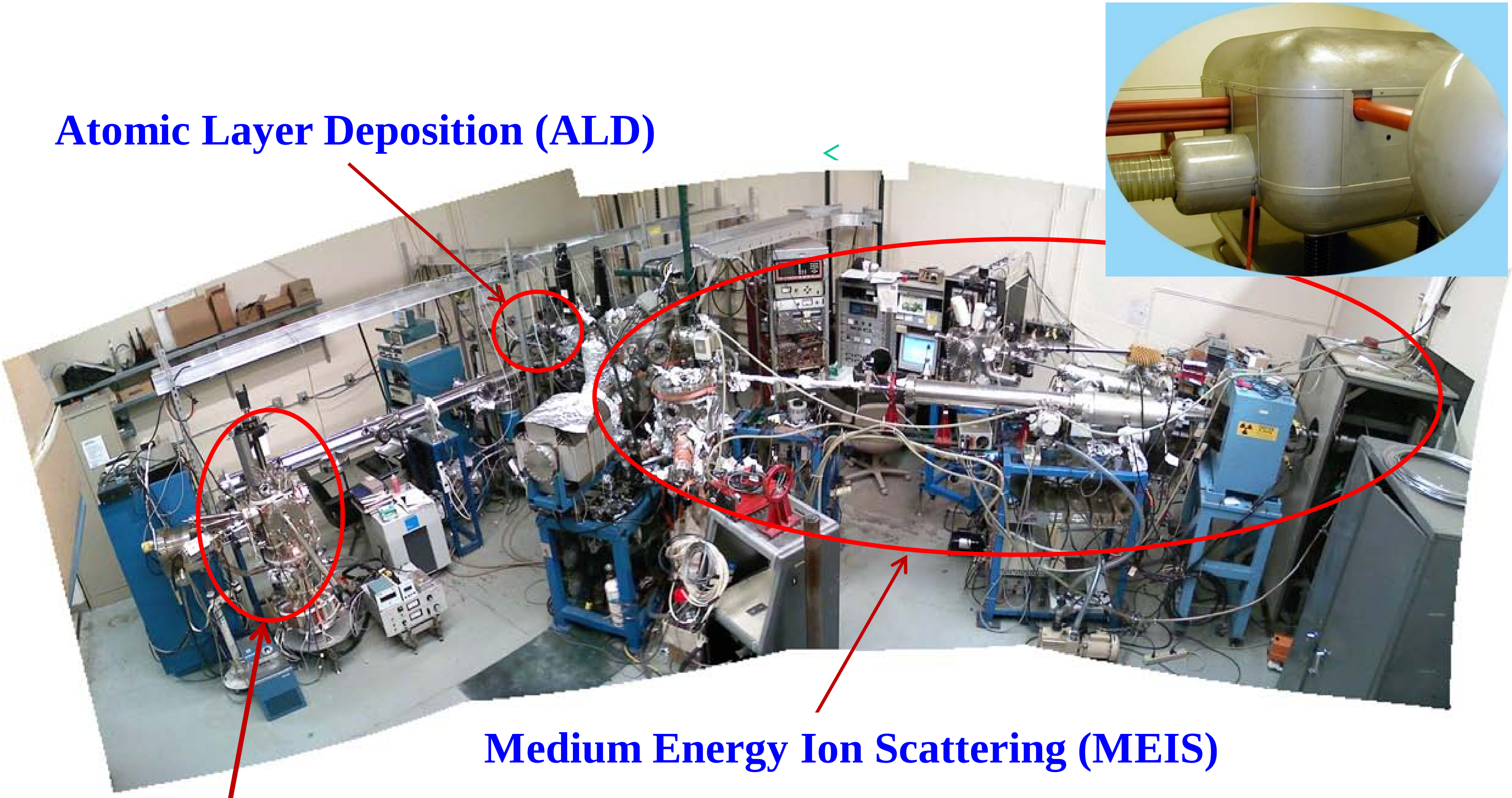
- Ion scattering - MEIS, RBS
- Electronic structure – XPS, UPS, Inverse PES, Internal PES
- Electrical – CV, IV (plus work with Sematech)
- Microscopy – TEM/STEM/EELS, SEM, STM, AFM….

Issues:

- Post-Si Substrates: Ge, GaAs, InGaAs
- Etching and passivation chemistry on alternative substrates
- Radiation induced defects (esp. in dielectric and at interfaces)
- Film initiation and growth (esp. for ALD growth)
- Influence of interface layers (work function engineering)
- Metal gate/high-κ dielectric film and interface stability
- Diffusion/atomic mobility (O, Si, N, metal, etc…)
- Epitaxial oxides and higher-K - e.g. STO/Si, La compounds

Integrated MEIS/ALD system

Atomic Layer Deposition (ALD)

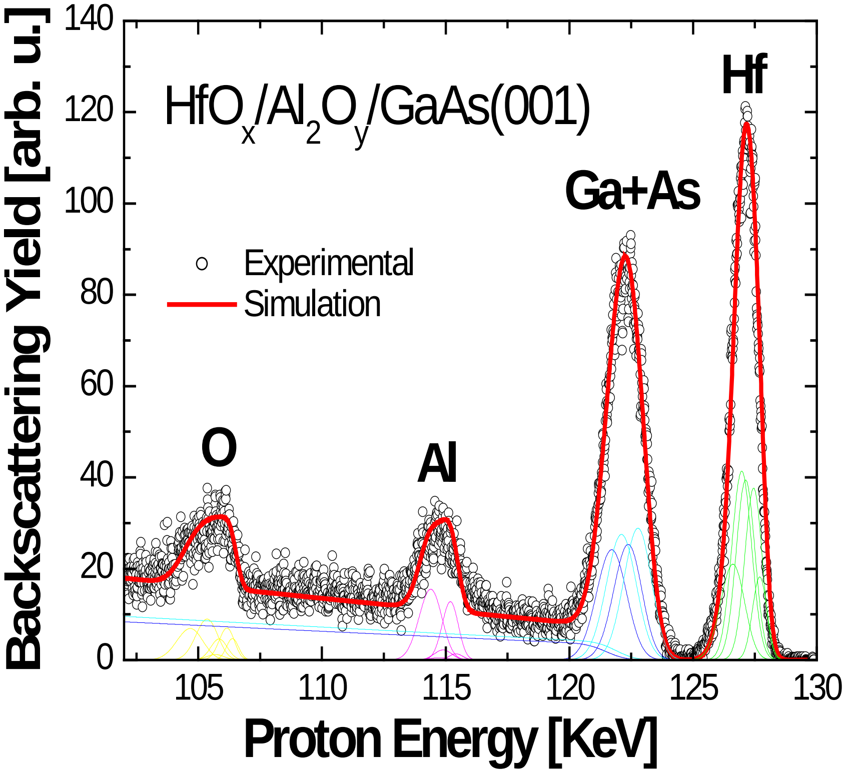


Medium Energy Ion Scattering (MEIS)

X-ray Photoemission (XPS)

Plus NRP, LEED, PLD, FTIR….

Medium Energy Ion Scattering (MEIS)



- Low energy, high resolution RBS
- Quantitative composition and structure down to ~200 Å
- High depth resolution:
  ~ 3 Å near surface
- Absolute elemental areal density

Purpose of this past year's work

- Explore processing and passivation chemistries for Ge devices (analogous to prior work on III-V substrates)
  - Control of interfacial oxide to minimize electrical defects between gate insulators and channel materials, and to maximize capacitance.
  - growth of an ideal dielectric layer

- What processing produces optimal films/interfaces?
- Solution (wet): etches, solution oxide growth
- Can we use gas-vacuum (dry) methods to clean and passivate: desorption anneals, ALD growth/cleaning, UV

Solution-based Ge cleaning and oxidation

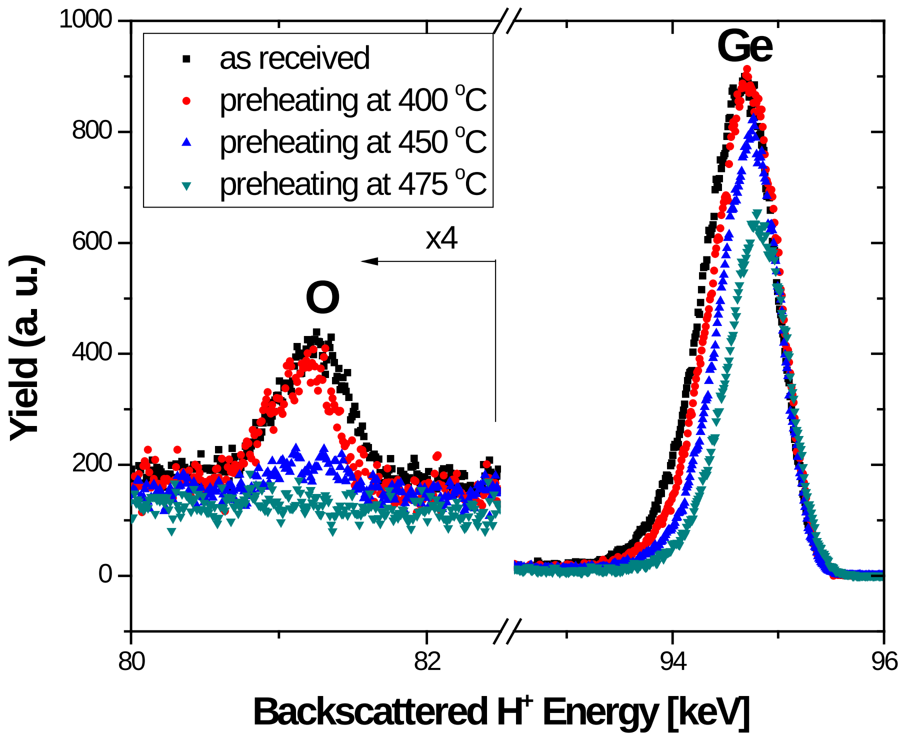
Some chemistries explored:

- **De-ionized water; HF; DIW/H_2O_2**
- **HF/DIW/H_2O_2**
- **NH_4OH/H_2O_2**
- **HCl/H_2O_2**
- **H_2SO_4**

Sulfur-passivation in hot $(NH_4)_2S$ on H_2SO_4/H_2O_2-treated Ge

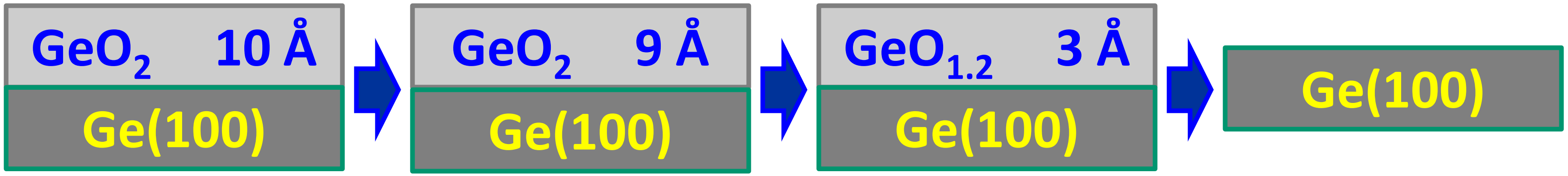
- **$(NH_4)_2S$ etches oxide**
- **Thin GeO_xS_y layer remains**
- **H_2SO_4/H_2O_2 and $(NH_4)_2S$ treatment results in low C**

Thermal desorption of the native oxide of Ge in high vacuum (≤10^{-7} torr)



- **~400 °C:**
  partial conversion of GeO_x
- **450 °C:**
  substantial desorption of O
- **475 °C:**
  no detectable oxygen
- **Decrease of Ge peak:**
  re-crystallization and/or loss of Ge

Drastic thermal desorption of O above 450 °C



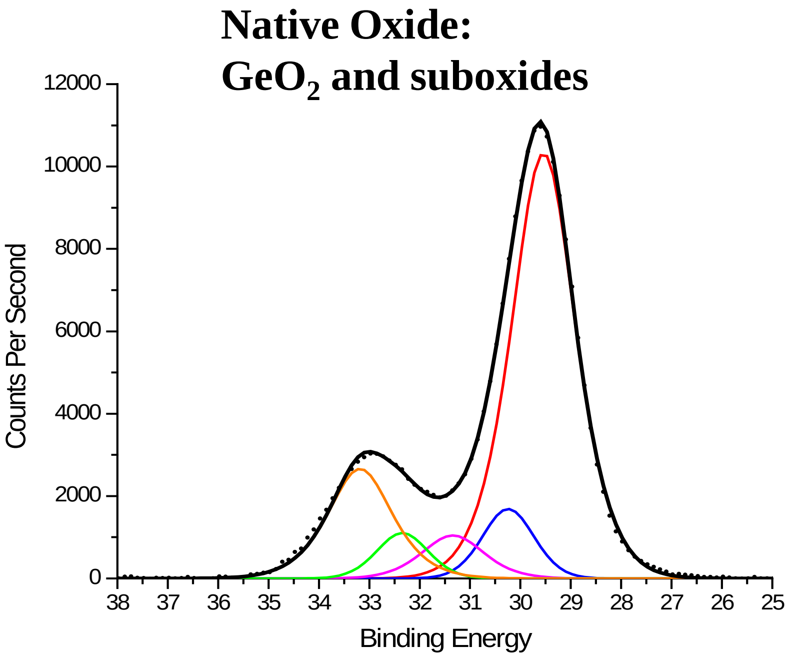
GeO_2 10 Å
Ge(100)

GeO_2 9 Å
Ge(100)

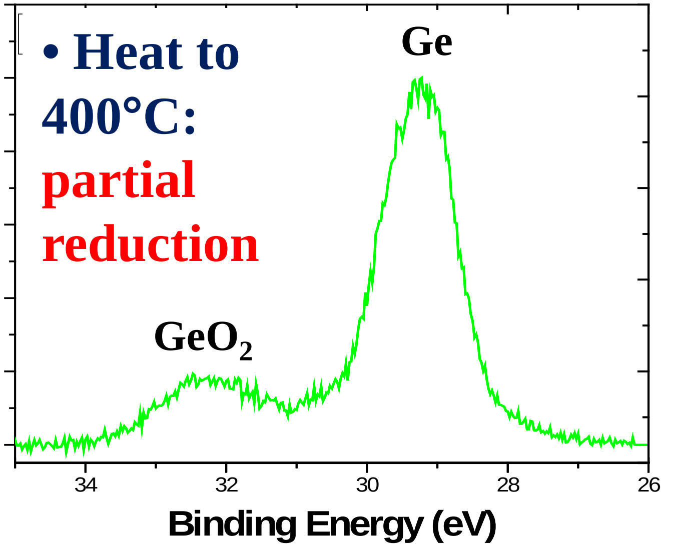
$GeO_{1.2}$ 3 Å
Ge(100)

Ge(100)

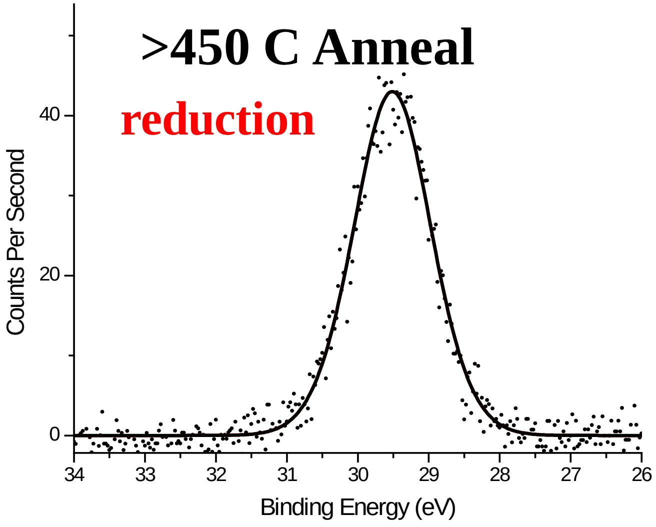
XPS of Ge oxide reduction during anneal



Native Oxide:
GeO_2 and suboxides



- **Heat to 400°C: partial reduction**

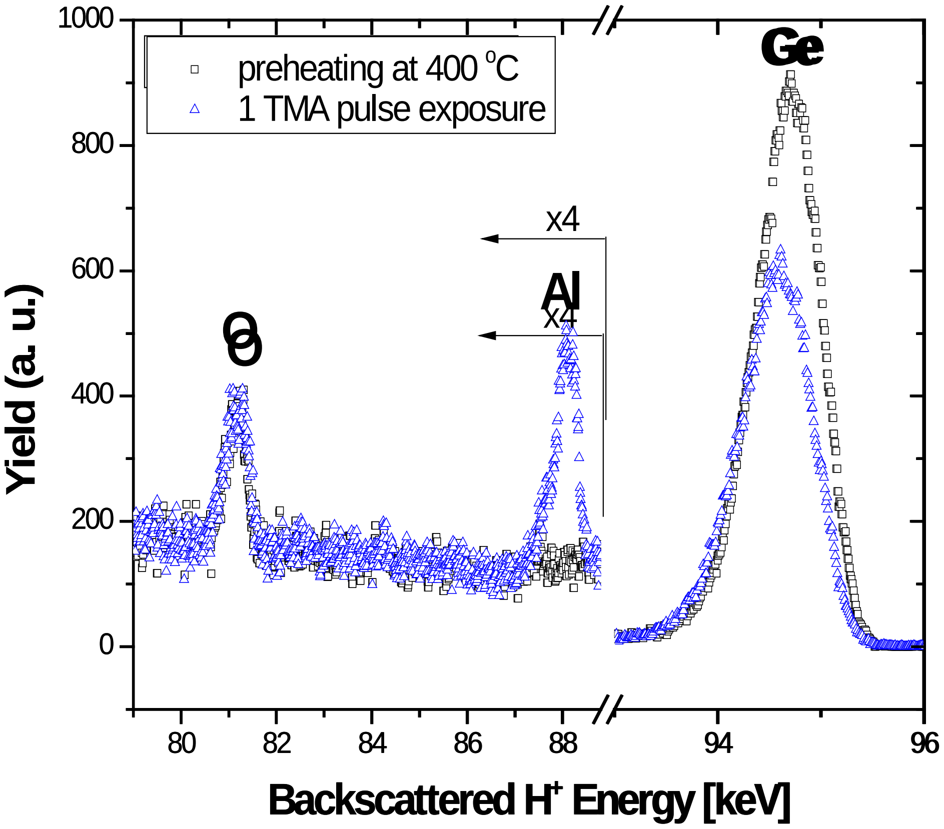


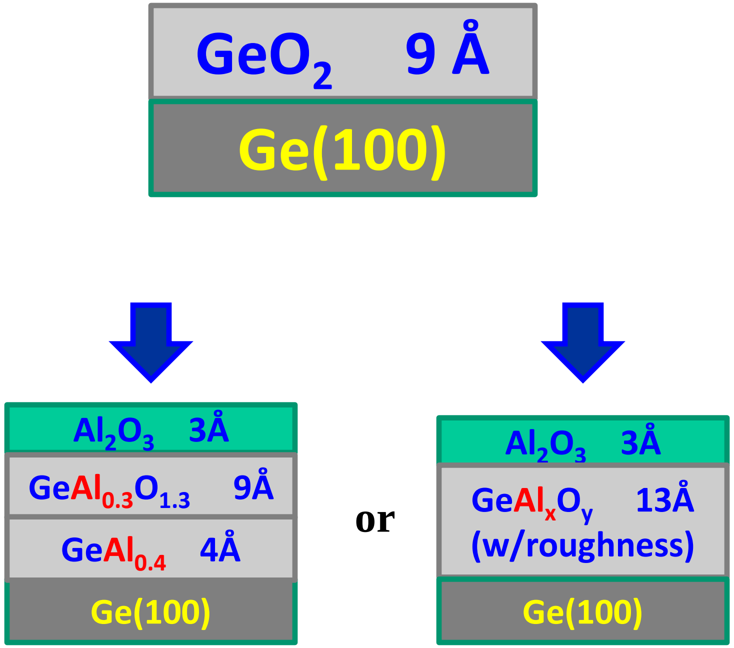
>450 C Anneal

reduction

- **Heat Ge in vacuum (or air) – oxide desorbs at much lower T than on Si.**

Reduction of Ge oxides by TMA exposure at 400C





GeO_2 9 Å

Ge(100)

Al_2O_3 3Å

$GeAl_{0.3}O_{1.3}$ 9Å

$GeAl_{0.4}$ 4Å

Ge(100)

or

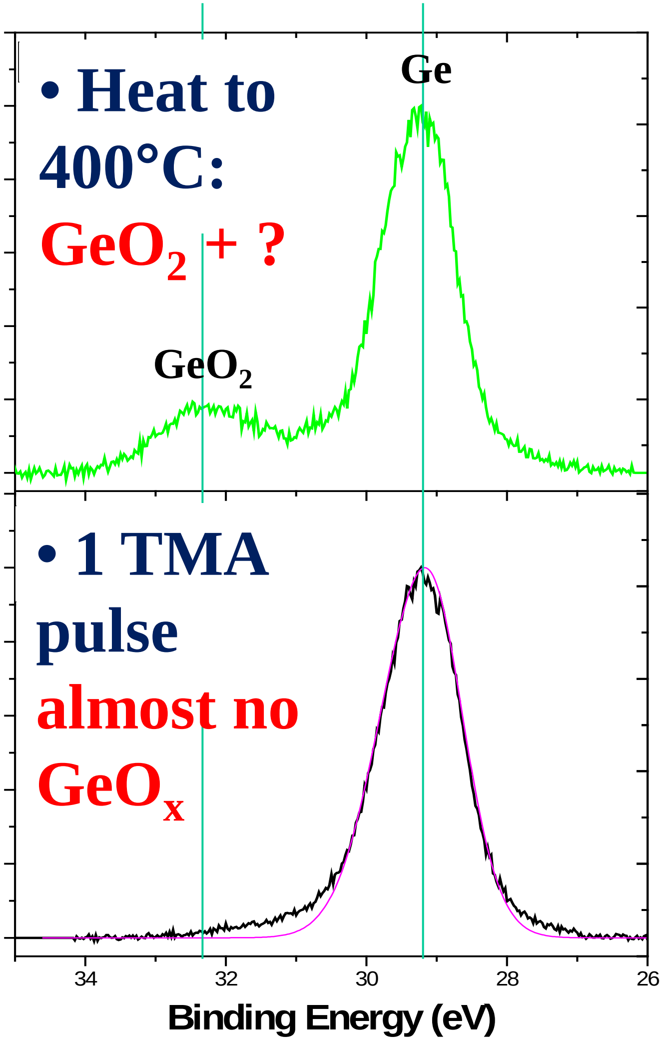
Al_2O_3 3Å

$GeAl_xO_y$ 13Å
(w/roughness)

Ge(100)

- No change of O content, $4.5\times10^{15}/cm^2$: Al_2O_3 formation occurs with O from the native oxide ➔ Ge native oxide reduction
- Decrease of Ge peak: re-crystallization and/or loss/desorption of Ge
- Al and Ge layers react and mix ➔ GeAlO and GeAl? layer

XPS of Ge oxide reduction during ALD growth



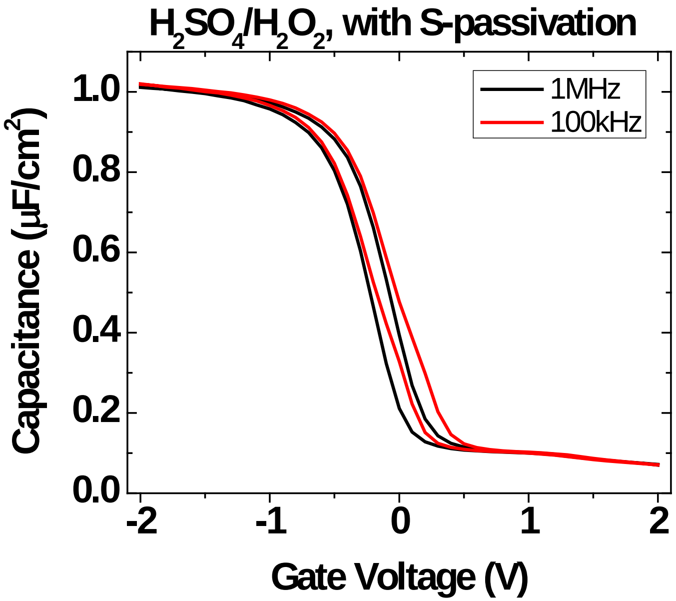
- Heat to 400°C:
  GeO$_2$ + ?

- 1 TMA pulse
  almost no GeO$_x$

Ge oxide reduction by TMA pulse!

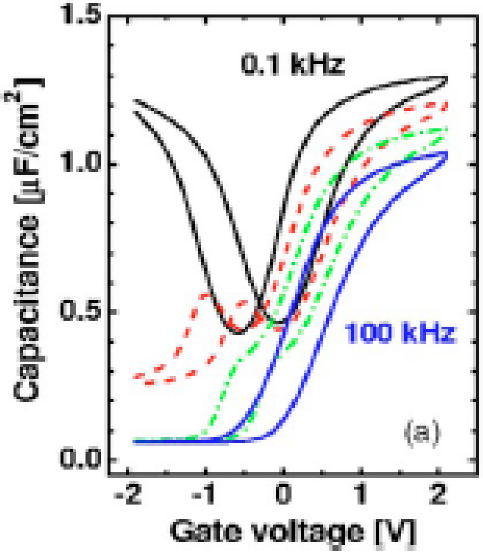
Ge surface chemistry and electrical defects

Cleaning	HF	HF/DIW/H_2O_2	H_2SO_4/H_2O_2 HF	H_2SO_4/H_2O_2
S-passivation	No	Yes	Yes	Yes
Q_i/e (cm^{-2})	4.00×10^{13}	4.17×10^{12}	3.56×10^{12}	3.19×10^{12}
ΔV_{FB_HS}(V)	0.31	0.29	0.22	0.15
D_{it} (eV^{-1} cm^{-2})	3.80×10^{12}	1.66×10^{11}	8.91×10^{10}	6.23×10^{10}



Prior work (lit.)

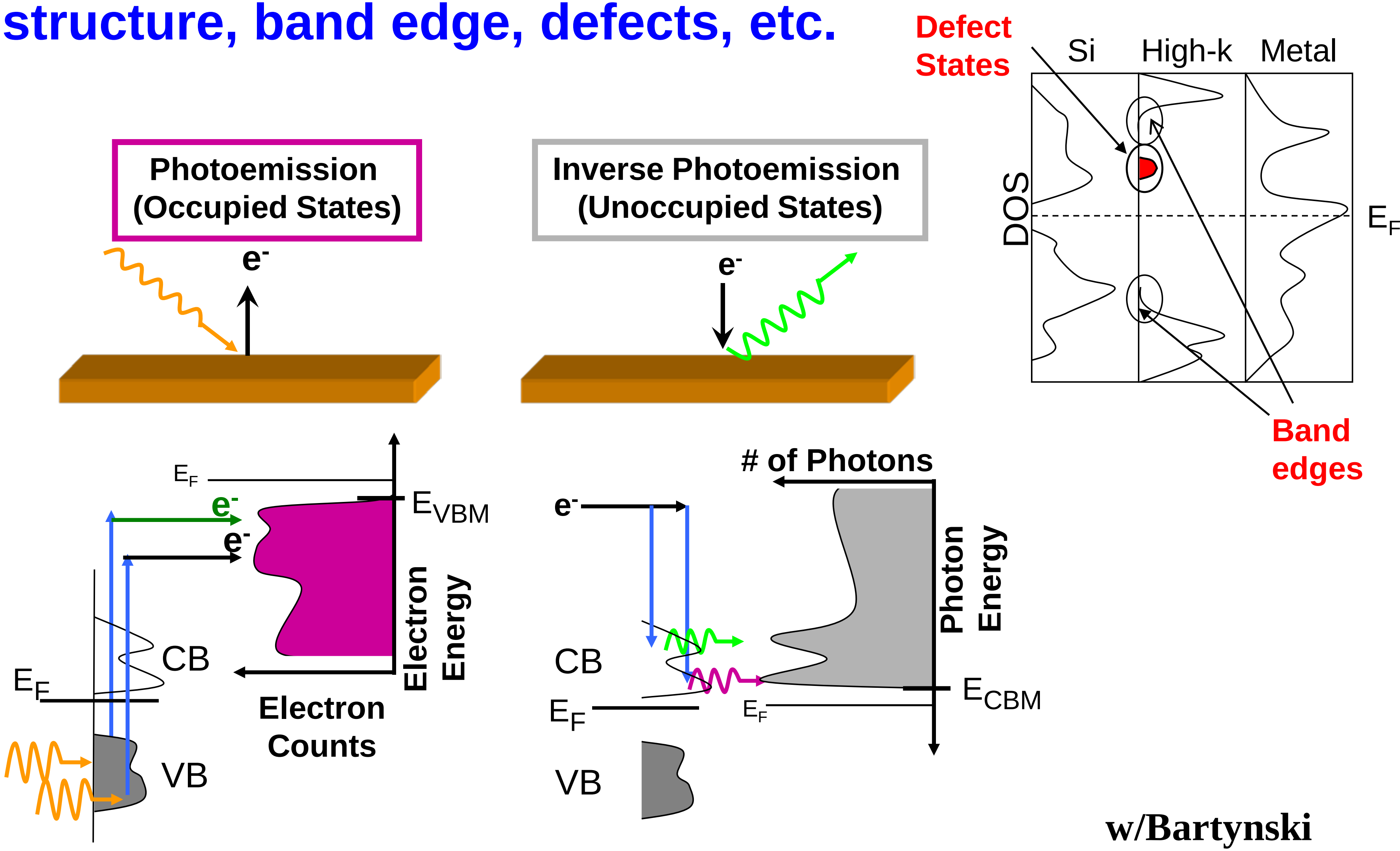
Current work



HfO_2 40A, hysteresis is ~0.15V.
Ge surface was first H_2SO_4/H_2O_2 treated.
No HF used before sulfidation in $(NH_4)_2S$.

77A HfO_2, hysteresis is ~0.5V.
10% HF etching for 10mins before sulfidation in $(NH_4)_2S$.
APL 89, 112905 (2006)

Experimental methods to determine electronic structure, band edge, defects, etc.



Photoemission (Occupied States)

Inverse Photoemission (Unoccupied States)

w/Bartynski

Post-silicon CMOS take home messages:

- **Radiation induced electrical defects (at low conc.) observable by C-AFM, but not most other surface methods.**
- **Although high-K films are defective, they appear not more sensitive to radiation degradation then SiO_2-based CMOS.**
- **High-K dielectrics and metal gates are in product….on Si!**
- **Very good devices can and have been grown on Ge and III-Vs.**
- **Electrical properties a strong function of surface passivation.**
- **Favorable band alignment found for some passivation and film growth conditions. Fermi level pinning (of interface defects?) can be controlled if film grown properly.**
- **Oxides of Ge and III-V's less stable thermally and electrically relative to SiO_2; can be consumed during high-K growth.**
- **Metallization materials and processes strongly affect interface chemistry and electrical properties.**

Recent MURI-related publications

- Sylvie Rangan, Eric Bersch, Robert Allen Bartynski, Eric Garfunkel and Elio Vescovo; *Band offsets of a ruthenium gate on ultrathin high-κ oxide films on silicon*, Physical Review B **79**, 075106 (2009).
- Hang Dong Lee, Tian Feng, Lei Yu, Daniel Mastrogiovanni, Alan Wan, Torgny Gustafsson, and Eric Garfunkel; *Reduction of native oxides on GaAs during atomic layer growth of* Al_2O_3, Applied Physics Letters **94**, 222108 (2009).
- M. Dalponte, M.C. Adam, H.I. Boudinov, L.V. Goncharova, T. Feng, E. Garfunkel and T. Gustafsson; *Effect of excess vacancy concentration on As and Sb doping in Si*, J. Phys. D: Appl. Phys. **42** (2009) 165106.
- S. Rangan, et al; Aluminum gate interaction with ultrathin high-k oxide films on Si, submitted.
- C.L. Hsueh, et al; Effect of surface oxidation and sulfur-passivation on Ge based MOS capacitors, submitted.
- E. Garfunkel, J. Gavartin and G. Bersuker, *Defects in CMOS Gate Dielectrics*, Defects in Microelectronic Materials and Devices: Edited by D. Fleetwood, S. Pantelides, and R.D. Schrimpf, CRC Press 2008 Chapter 11, pp 341-358.

These and other papers can be downloaded at: http://garf.rutgers.edu

Future directions

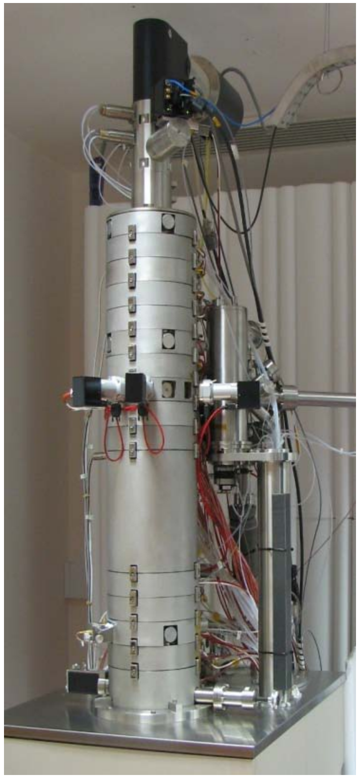
- Focus further on planar Ge, SiGe, III-V, GaN, SiC… substrates
  - **Correlate defect generation rate with E_{gap} and e-h pair generation probability of semiconductor and metal layers adjoining dielectric**
  - **Correlate physical and electrical measurements of “intrinsic” and “radiation induced/enhanced” defects**
  - **Explore E_f pinning and relation to radiation induced defects**
  - **Monitor H/D concentration/profiles in post-silicon materials**
- Si, Ge and III-V nanowire devices
- Radiation-induced defects in organic electronics, novel memory, graphene-based devices, MEMS

Our value to community: ultrathin film growth (ALD, etc), atomic scale resolution (ion scattering, spectroscopy), materials chemistry

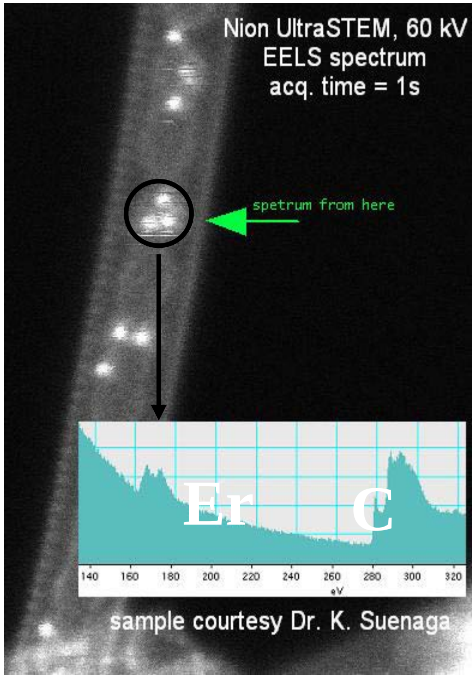
Nion–Rutgers (Krivanek-Batson) Collaboration: High Resolution EELS in an aberration-corrected STEM

- *~10 meV target EELS energy resolution*
- *20-50 pA into a 1-1.5 Å probe @50 kV*
- *~0.5 Å probe @10pA, 100kV (lower energy res.)*

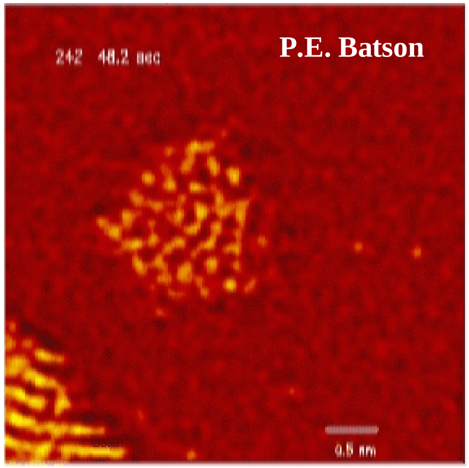
Nion aberration-corrected TEM column



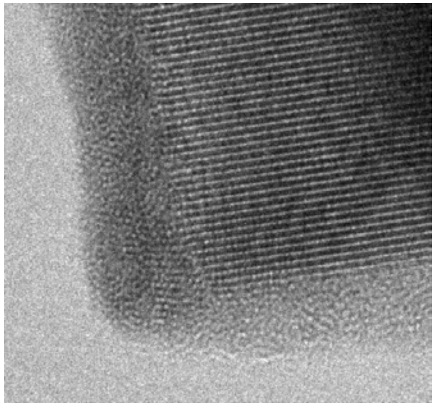
Atomic resolution spectroscopy: Er-doped buckyball filled nanotube



Optical Dielectric Forces: Au Coalescence



HfO_2-coated Ge nanowire



Additional slides

Including some work from past years

Post-Docs and Students (PDs available for employment)

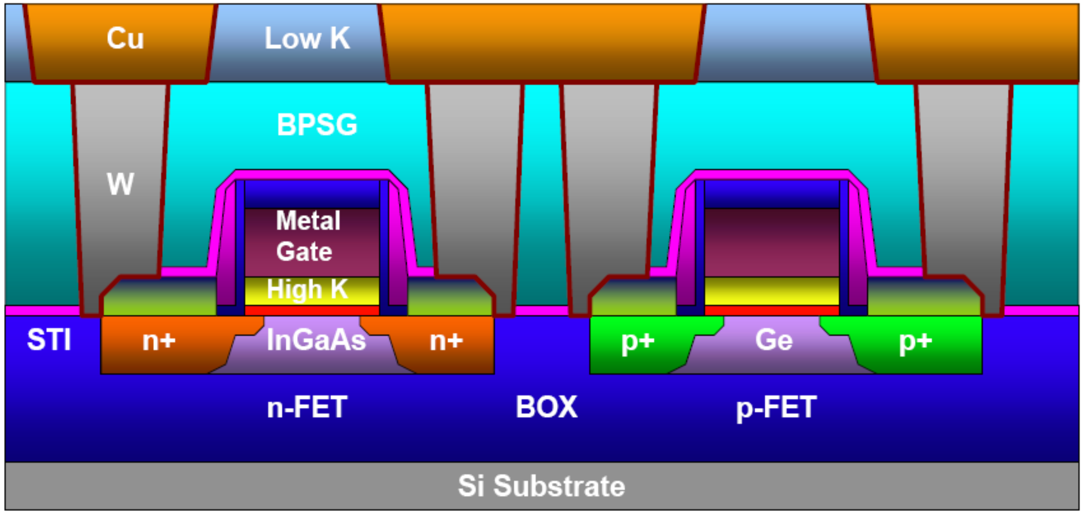
- Post-Docs
  - Lei Yu
  - Ozgur Celik
  - ChienLan Hsueh
  - Alan S. Wan
  - Hang Dong Lee

- Current Students and Anticipated Graduation Date
  - Tian Feng, Dec. 2010
  - Lauren Klein, January 2011
  - Dan Mastrogiovanni, June 2011

Alternative Channel Materials

- Mobility improves by straining Si, but CMOS scaling would benefit from yet higher mobility….try other semiconductors.
- A key challenge for alternative channel materials is passivation – need low interface and bulk defect concentration.

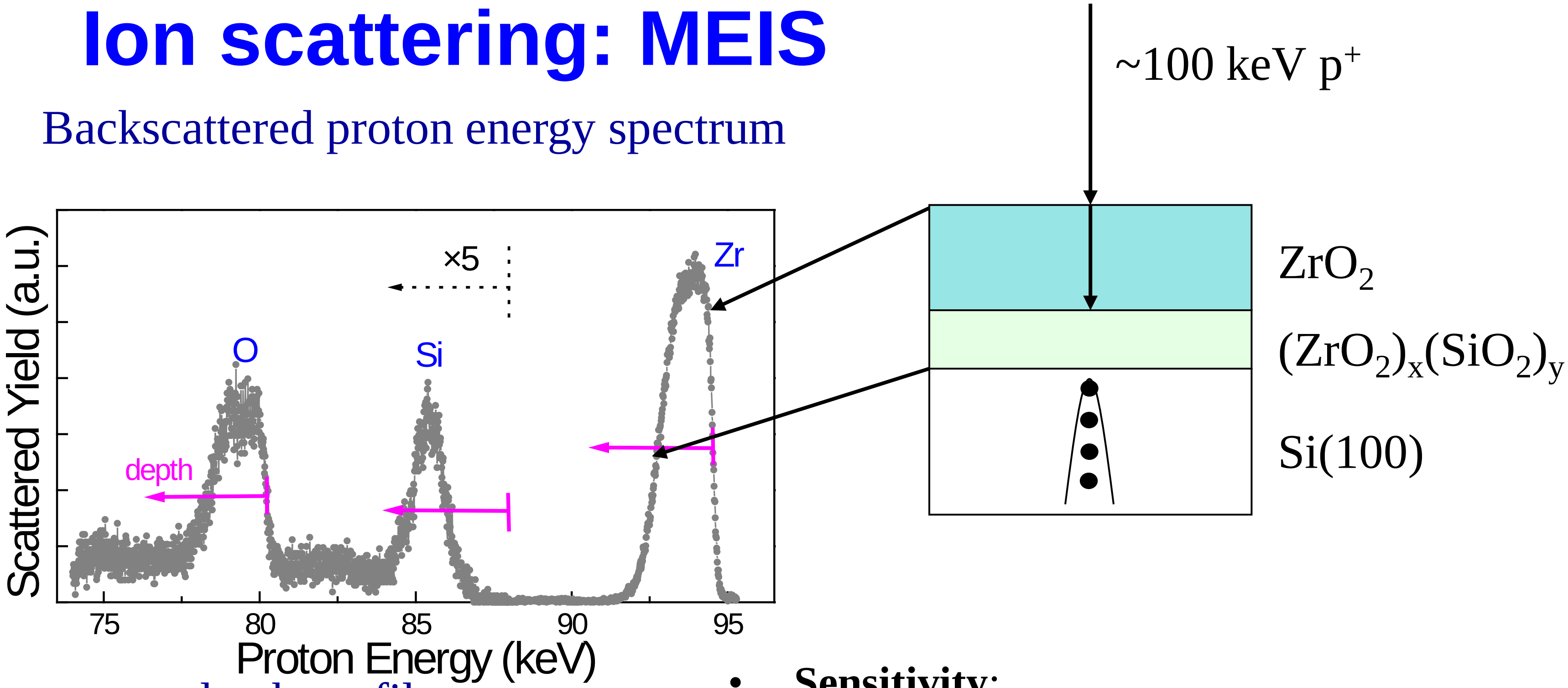
- InGaAs-on-insulator: NFET (surface channel)
- Ge-on-Insulator: PFET (surface channel)



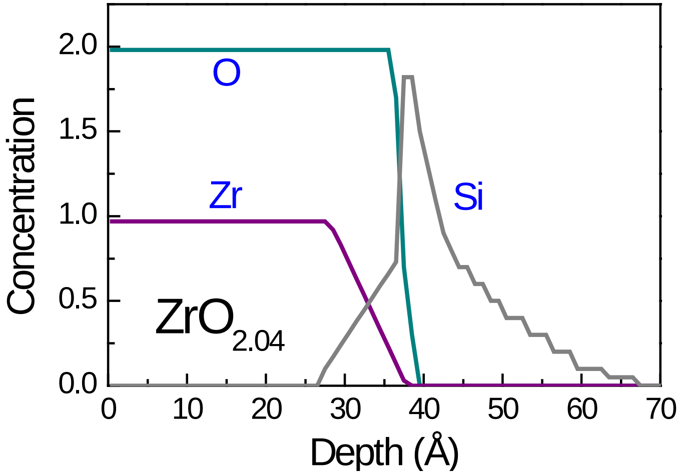
IBM

Ion scattering: MEIS

Backscattered proton energy spectrum

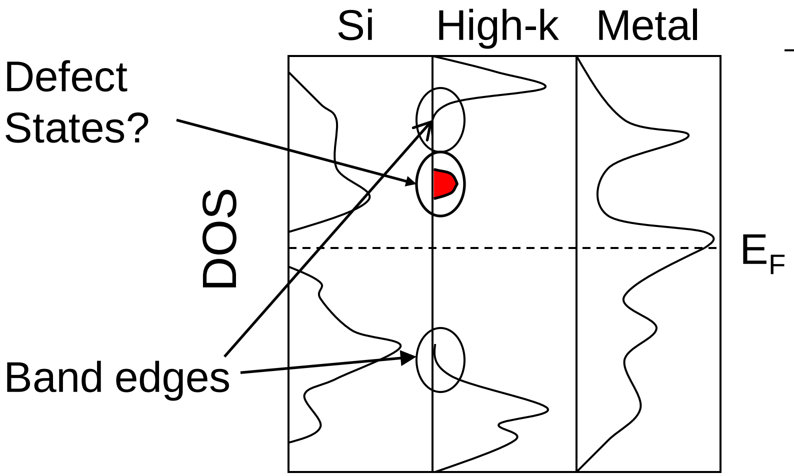


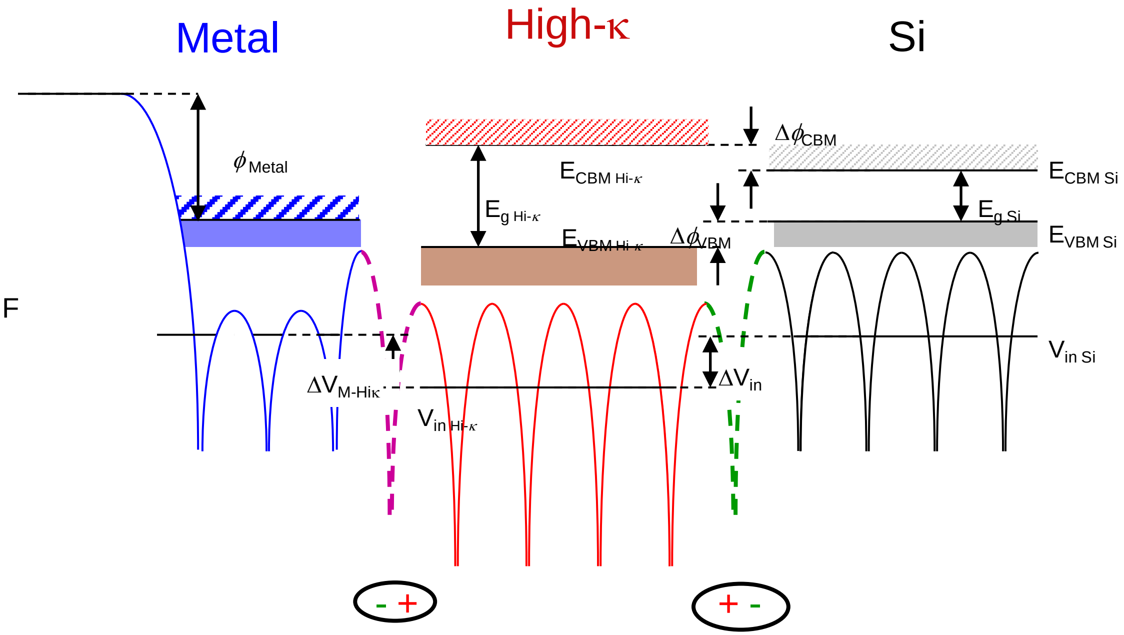
depth profile



- **Sensitivity**:
  ≈ 10^{+12} atoms/cm^2 (Hf, Zr)
  ≈ 10^{+14} atoms/cm^2 (C, N)
- **Accuracy** for determining total amounts:
  ≈ 5% absolute (Hf, Zr, O), ≈ 2% relative
  ≈ 10% absolute (C, N)
- **Depth resolution**: (need density)
  ≈ 3 Å near surface
  ≈ 8 Å at depth of 40 Å

Electronic structure across multilayer stacks





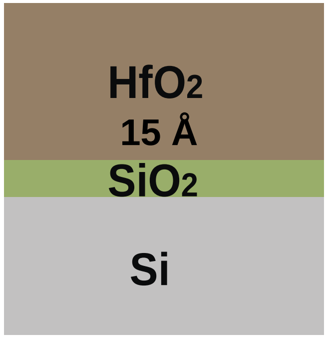
Band alignment, “effective” work function, energy gap…

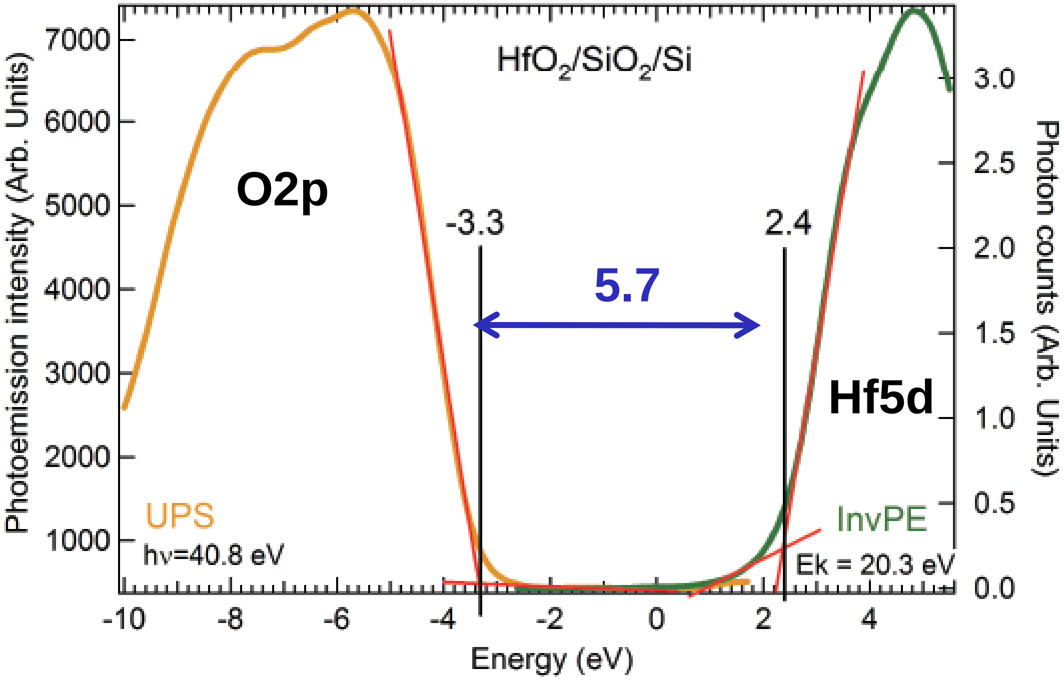
- Band edge energies determined in many ways – elec. and optical spec.
- Can we use spectroscopies to (i) measure energies and LDOS more precisely, (ii) determine interface dipoles and band alignment, and (iii) use interface engineering to control effective work function…

Photoemission and inverse photoemission of $HfO_2/SiO_2/Si$

Single chamber

UHV measurments





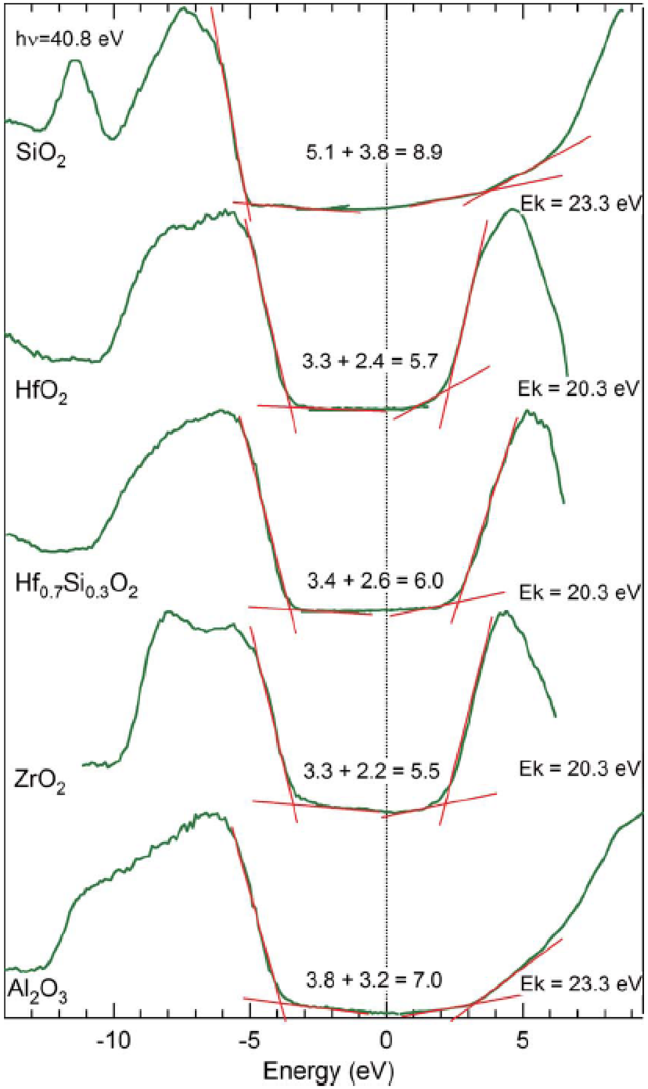
Gap determination

Substrate band edges determination

↓

Band offsets

Band alignment determination by photoemission and inverse photoemission



	Gap	VBO	CBO	χ
Si	1.1			4.1
SiO_2	8.9	4.5	3.3	1.3
HfO_2	5.7	2.7	1.9	2.5
$Hf_{0.7}Si_{0.3}O_2$	6.0	2.8	2.1	2.8
ZrO_2	5.5	2.7	1.7	2.7
Al_2O_3	7.0	3.2	2.7	2.5

Direct experimental determination of crucial parameters:

Gap, VBO, CBO and χ

Band offsets of ultrathin high-k oxide films with Si, Bersch et al., Phys. Rev. B 78 (2008) 085114

Fundamental understanding of band alignment (conduction band)

	Ru		Al		Ti	
Oxide	**Expt**	**MIGS**	**Expt**	**MIGS**	**Expt**	**MIGS**
HfO_2	2.4	2.5	1.5	1.9	1.8	1.9
$Hf_{0.7}Si_{0.3}O_2$	2.4	2.4	1.5	1.8	1.7	1.8
SiO_2	3.8	3.9	3.4	3.0	3.1	3.0
Al_2O_3	3.0	2.7	2.0	2.0	2.4	2.0

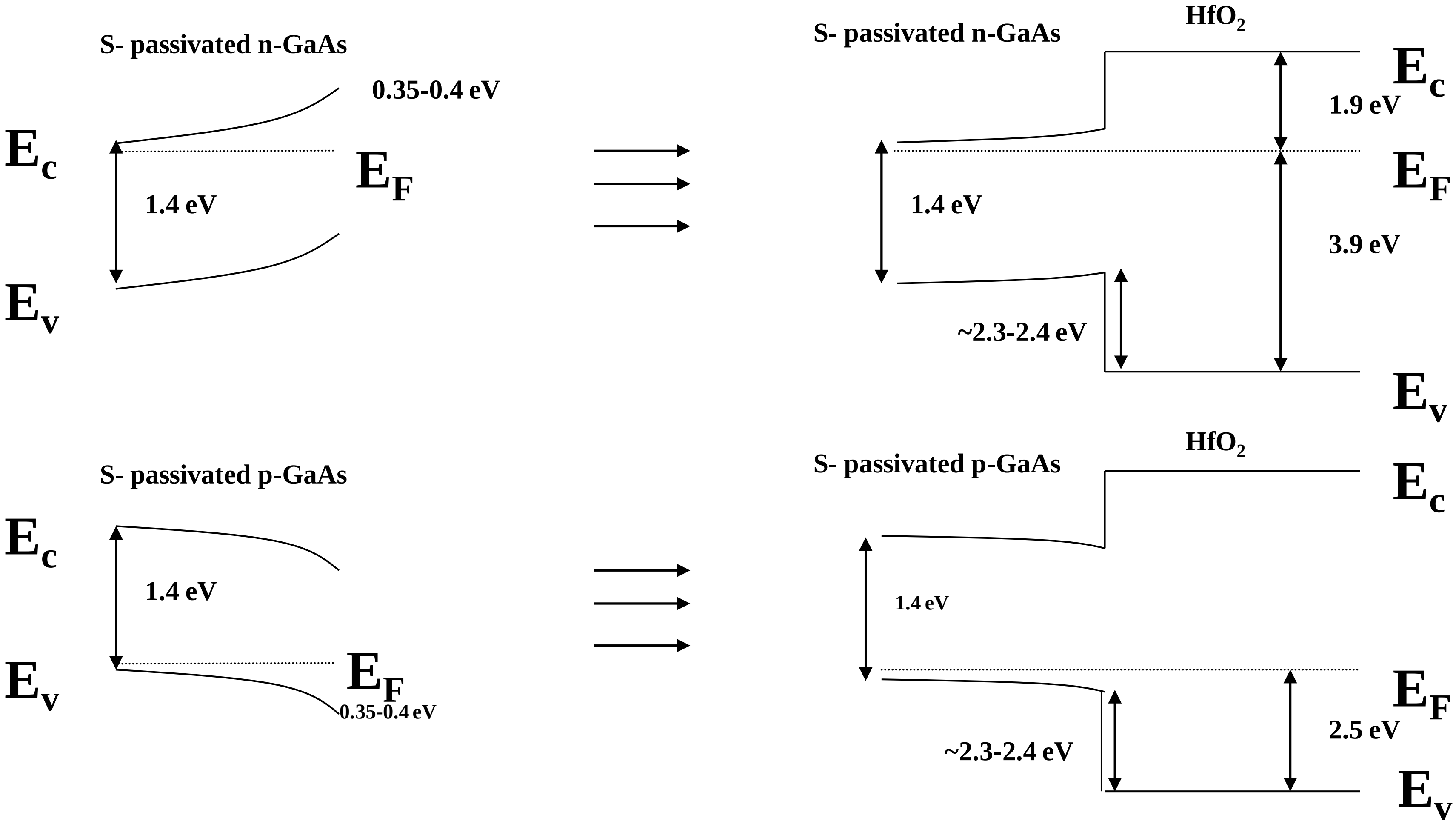
Agreement between experimental CBO and MIGS-predicted CBO when no metal-induced interface oxide is present.

Band offsets of a ruthenium gate on ultrathin high-k oxide films on Si, Rangan et al., Phys. Rev. B 79 (2009) 075106

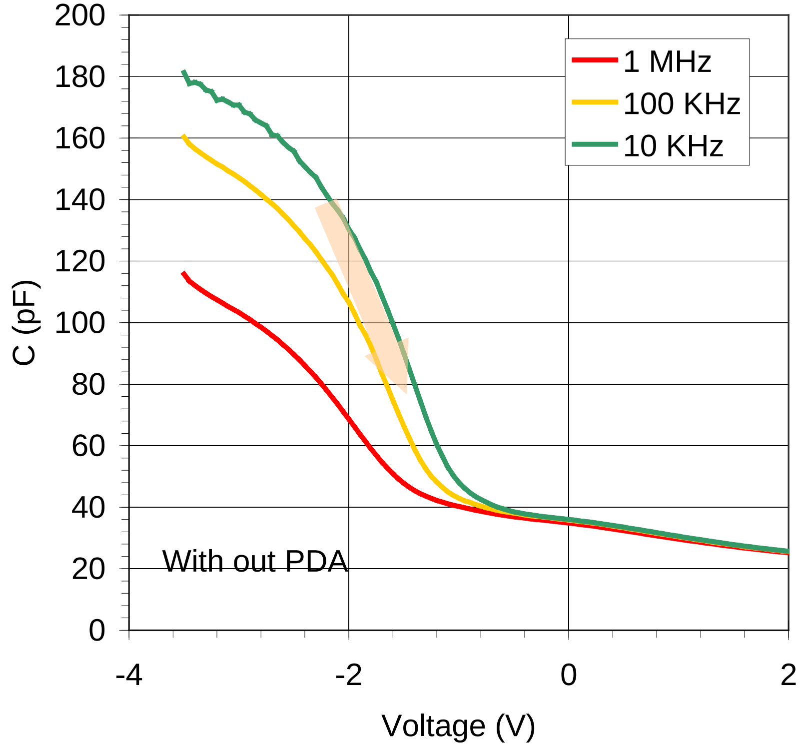
Aluminum gate interaction with ultrathin high-k oxide films on Si, Rangan et al., submitted APL

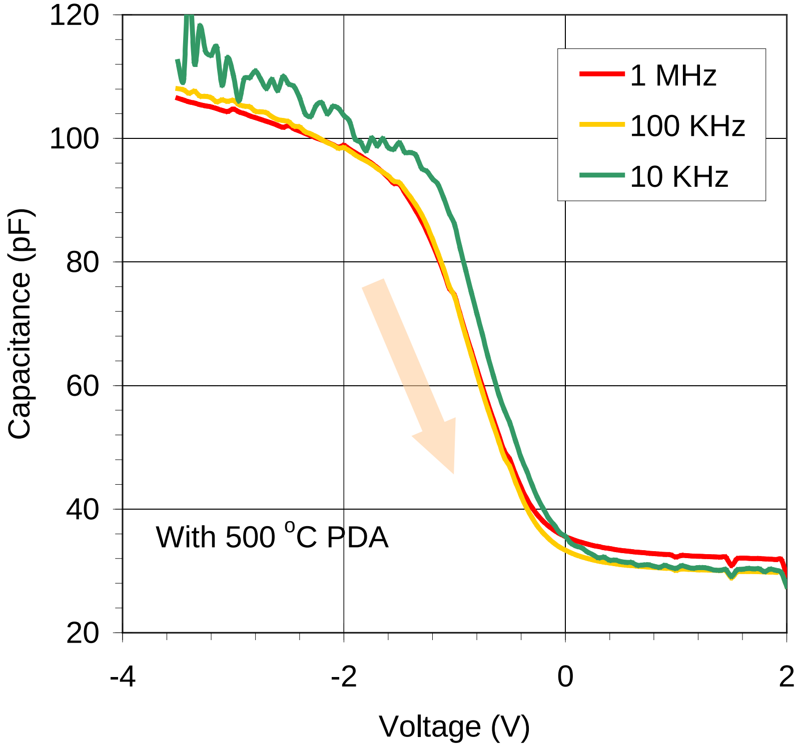
Band offsets of a Ti gate with ultrathin high-k oxide films on Si, Rangan et al., manuscript in preparation

- **On S-passivated III-V films E_f is partially pinned.**
- **After HfO_2 growth, much less pinning.**
- **Conduction and valance band offsets agree with literature.**



4.5 nm thick III-V MOSCAPs (effect of 500 ºC PDA)



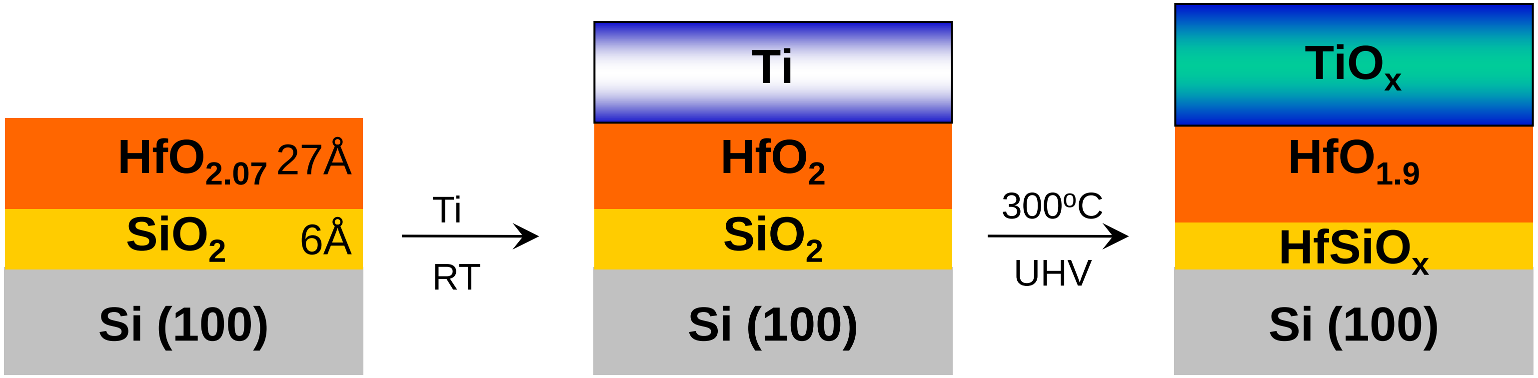


ALD growth at 320 ºC; Device area: 2.5×10^4 μm^2.

For thin oxide, PDA significantly improves freq. dispersion, assuming that the MOSCAP CV behavior is dominated by the interface quality

Gate metal effects on chemical stability of dielectrics

Metal as source or sink for oxygen and hydrogen



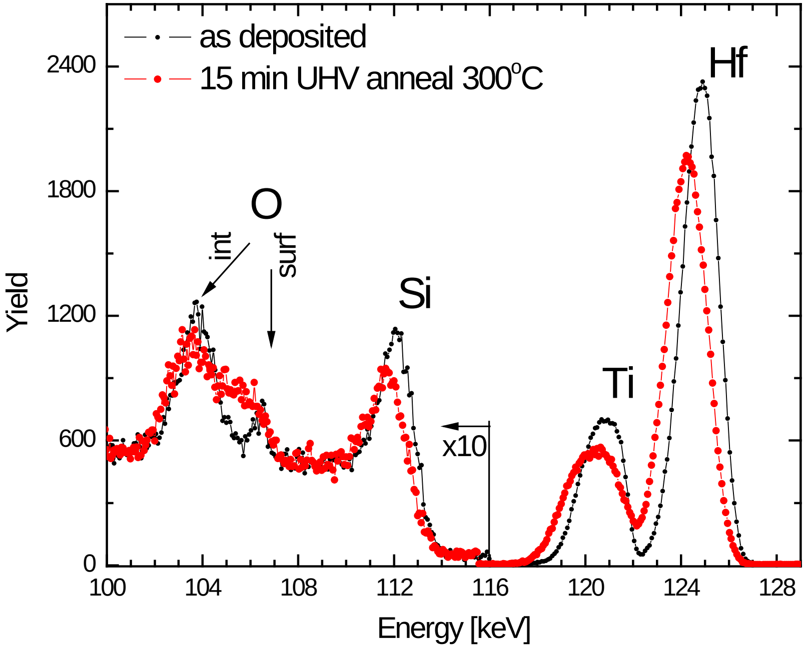
$HfO_{2.07}$ 27Å
SiO_2 6Å
Si (100)

$\xrightarrow[\text{RT}]{\text{Ti}}$

Ti
HfO_2
SiO_2
Si (100)

$\xrightarrow[\text{UHV}]{300^oC}$

TiO_x
$HfO_{1.9}$
$HfSiO_x$
Si (100)



- Initial HfO_2 film has small amount of interfacial SiO_2 (~6-7Å) and excess of oxygen (~$HfO_{2.07}$)
- Deposited Ti forms uniform layer, no strong intermixing with HfO_2;
- Oxygen concentration in Ti layer is small

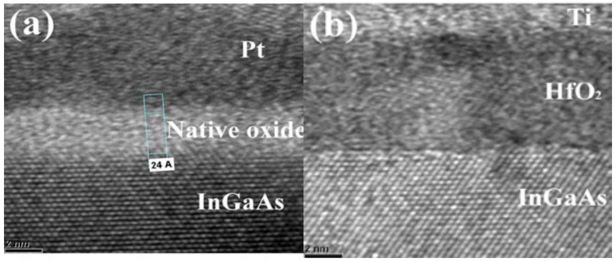
<u>After UHV anneal at 300°C for 15 min:</u>

- Lowering and broadening of Ti peak
- Hf and Si peak shift and O peak changes

⇒ Ti layer partially oxidized

Interface reduction (self-cleaning) during growth and processing

- “Self-cleaning” during ALD growth is a phrase that described the concomitant reduction and removal of surface oxides from a substrate during the ALD process. It has been observed by several groups (P.D. Ye et. al.,APL, 83, 180; M. Frank et. al., APL, 86, 152904; C. Hinkle et. al., APL, 92, 071901).



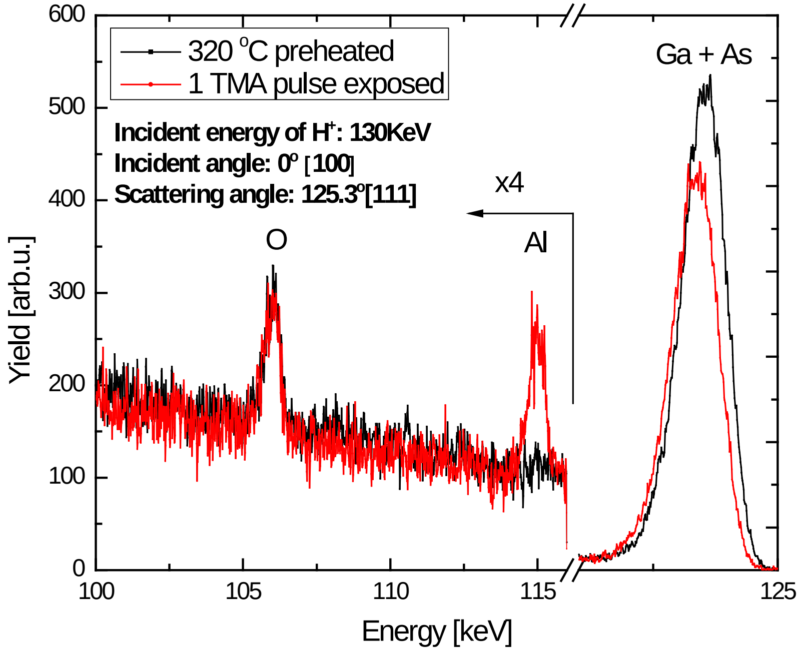
C.H. Chang et. al. (APL, 89, 242911)

- Some issues regarding “self-cleaning”:

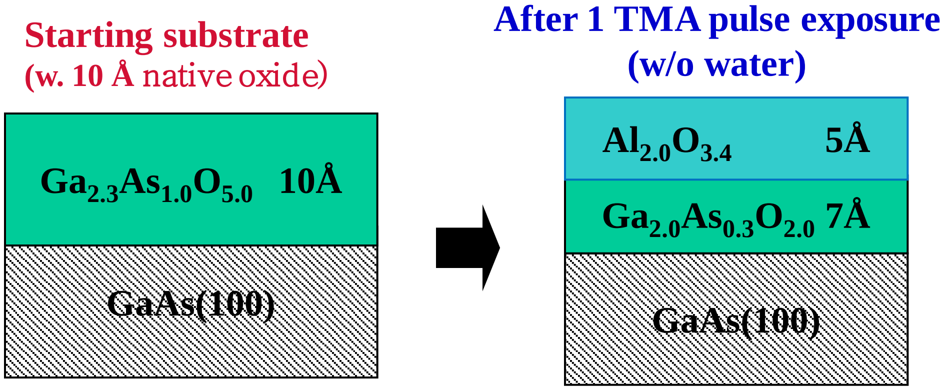
1. When does it occur? At the very first introduction of precursor or continuously through the growth?
2. Where do the surface chemical species go? Desorb or incorporate into the dielectric or substrate?
3. Can it help us prepare optimal gate stacks?
4. No detailed structural data reported regarding “self-cleaning”.

Native oxide reduction after 1 TMA pulse

In situ MEIS



- **The O content in the Al oxide layer is 3.5 ($\times 10^{15}$at./cm^2), similar to the O decrease in the native oxide layer, 3.0 (= 4.6-1.6) ➔ O atoms from the native oxide layer form the Al oxide (the *only* oxygen source).**
- **The (Ga+As) density in the native oxide layer is reduced from (2.0+0.9) to (1.6+0.24) ➔ desorption of Ga and As.**



Starting substrate
(w. 10 Å native oxide)

$Ga_{2.3}As_{1.0}O_{5.0}$ 10Å

GaAs(100)

After 1 TMA pulse exposure
(w/o water)

$Al_{2.0}O_{3.4}$ 5Å

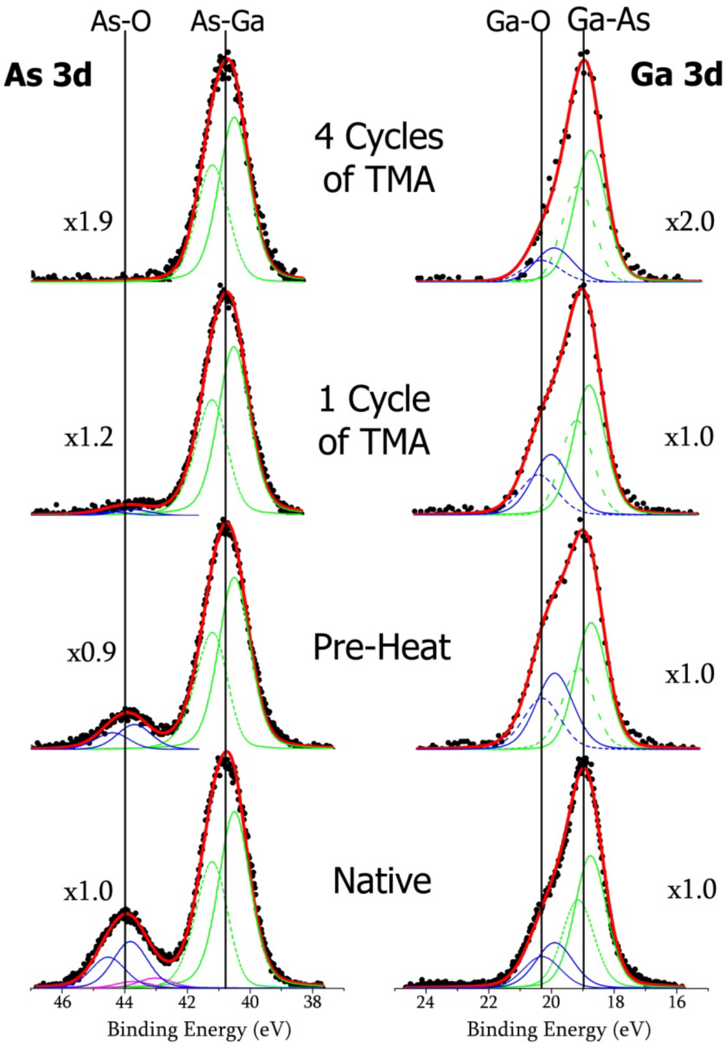
$Ga_{2.0}As_{0.3}O_{2.0}$ 7Å

GaAs(100)

Areal density ($\times 10^{15}$ at./cm^2)

		Preheated	1 TMA
Native oxide	Ga	2.0	1.6
	As	0.9	0.24
	O	4.6	1.6
Al oxide	O	n/a	3.5
	Al	n/a	2.0

Photoemission (XPS) during growth



After preheating: Conversion of As_2O_3 (46% decrease) to Ga_2O_3 (47% increase) (relative to as-received wafer).

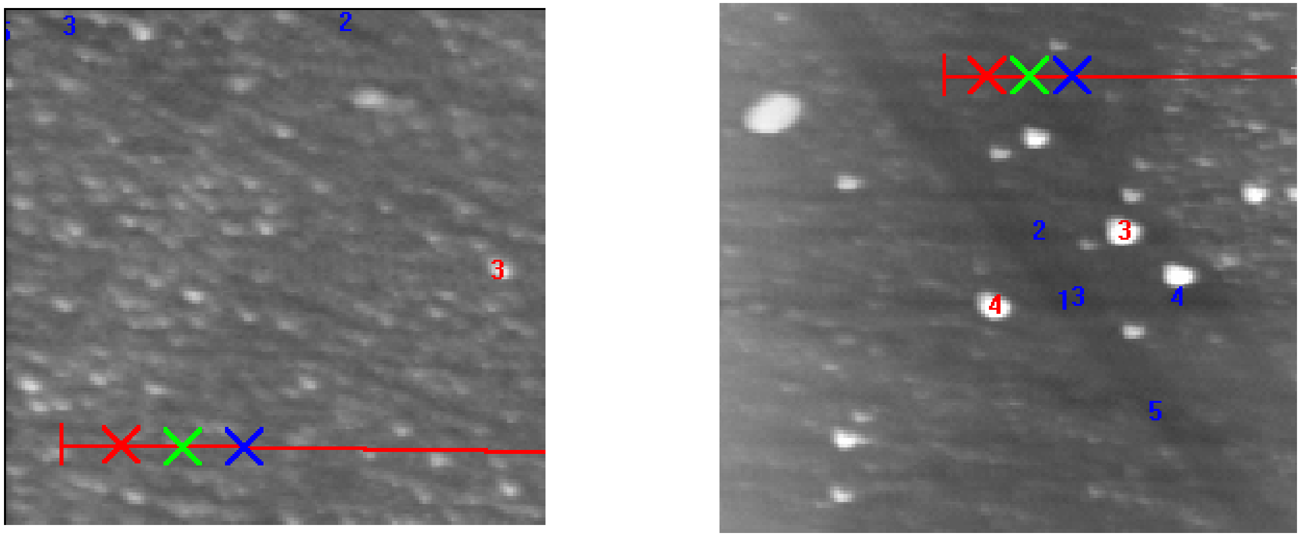
The native oxides in the preheated samples consist of a mixture of As_2O_3, As_2O_5 and Ga_2O_3. The Ga:As ratio (~2:1) is close to the one from MEIS (2.3:1).

After 1 TMA pulse: Decrease of the As-O (~75%) and Ga-O (~16%) peak areas, consistent with MEIS.

After 4 TMA pulses: Further decrease of As-O below the XPS detection level (to a lesser extent also Ga-O) - confirms the MEIS result.

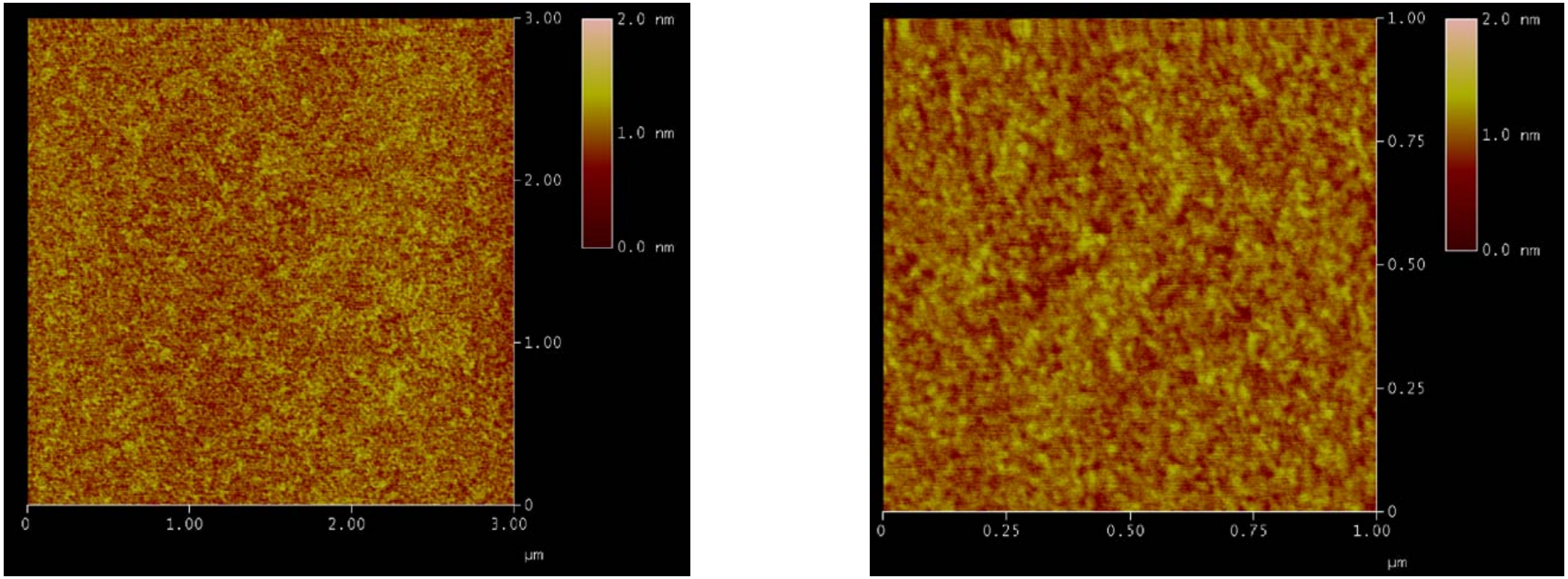
AFM images of HfO_2/SiON/Si

Before (a) and after (b) radiation exposure ~10^{15} ~ 200keV He^{2+}



(a) (b)

AFM images of Al-HfO_2-InGaAs stack before (a) and after (b) 100 keV H^+ (~10^{15} ion/cm^2) Intel/Stanford



(a) **(b)**

Conductive Tip AFM Image and I-V Behavior of a Ru/HfO_2/Si Stack

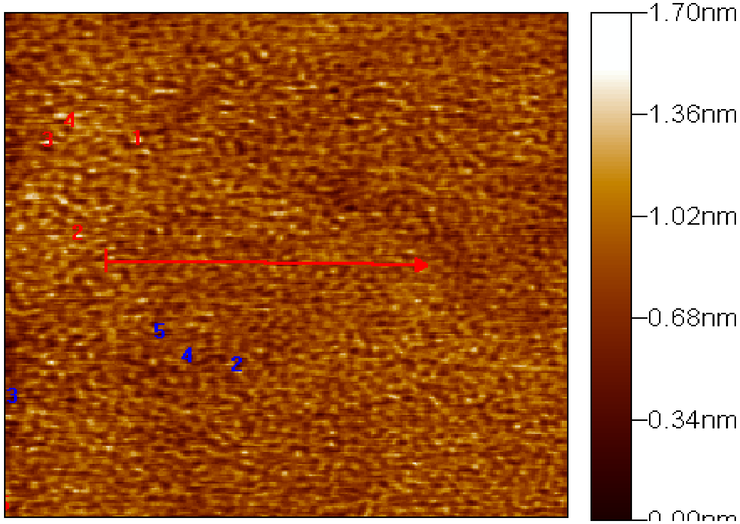


Image physical and spectroscopic behavior of radiation induced defects

For simple F-N tunneling with an electron effective mass of 0.18, the HfO_2/Si conduction band barrier height is 1.4eV