Materials stability, band alignment and defects in post-Si CMOS nanoelectronics

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Collaborators:

Vanderbilt team; Sematech team - Bersuker, et al.

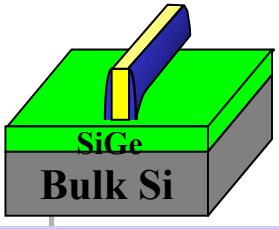
plus researchers at NIST, NCSU, Stanford, IMEC, UT-A, UT-D, Penn State, UAlbany, UCSB, UCSD, IBM, Intel, AMAT, TI, Freescale…

Support: Vanderbilt MURI (AFOSR) and SRC

One vision of the CMOS roadmap (from Sematech)

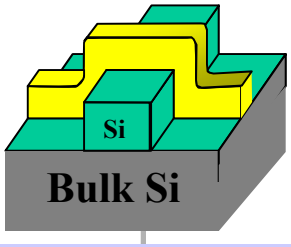
High-k / Metal Gate

Hi Mobility Channel



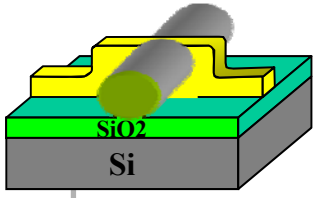
Characterization Issues:
- SiGe-HK Interface
- Damage at p-n in SiGe
- Strain in channel

FinFET

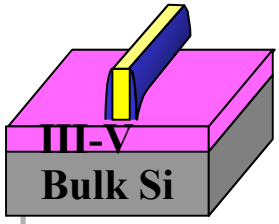


Characterization Issues:
- Sidewall S/D doping
- Sidewall silicidation
- Sidewall etch

Nanowires



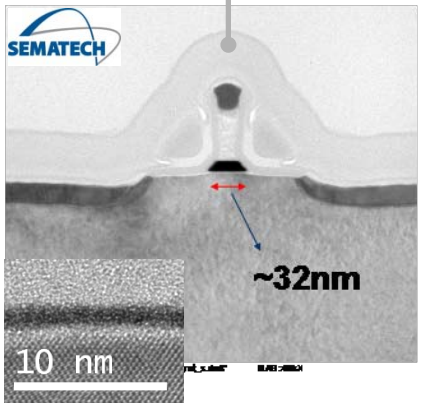
III-V

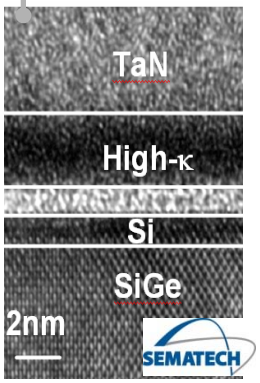


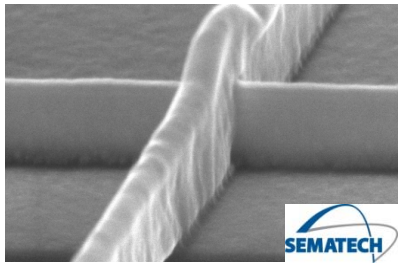
Characterization Issues:
- strain, E_g for III-V on Si
- III-V – HK interface
- Doping

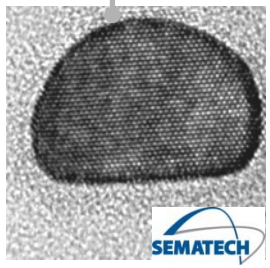
Many options!

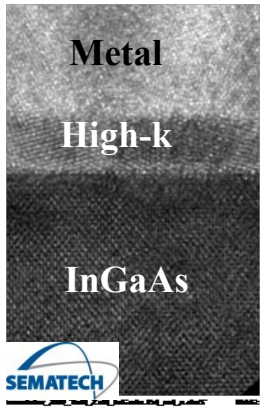
2009 2011 2013 2015 2017 2019







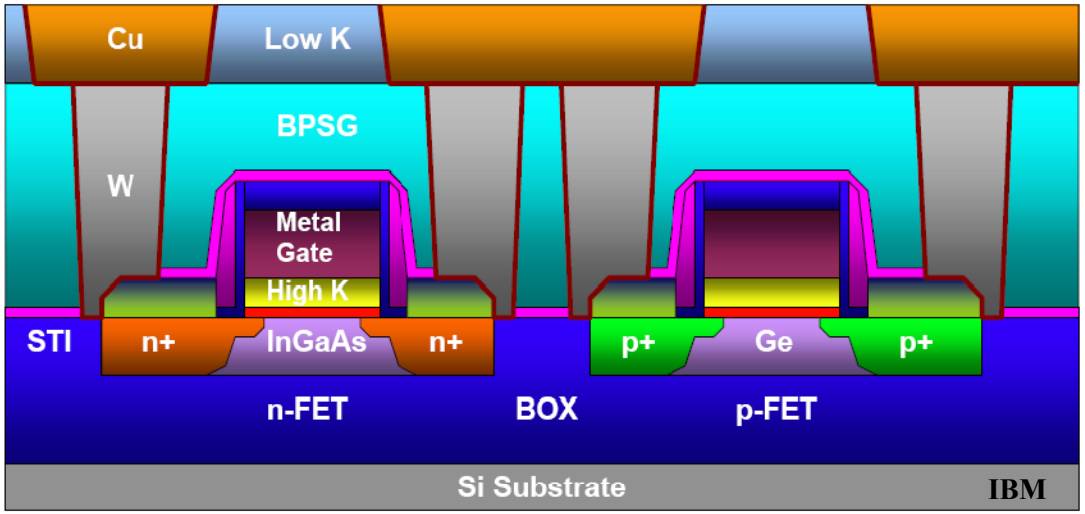




Alternative Channel Materials

- Mobility improves by straining Si, but CMOS scaling would benefit from yet higher mobility….try other semiconductors.
- A key challenge for alternative channel materials is passivation – need low interface and bulk defect concentration.
- Need high I_{on}/I_{off} ratio, appropriate integration, high thermal stability, appropriate band alignment with no E_f pinning, etc.
- Ge and SiGe studied for years for CMOS; now III-Vs as well.

  - InGaAs-on-insulator: NFET (surface channel)
  - Ge-on-Insulator: PFET (surface channel)



Motivation: Help develop a fundamental understanding and control of radiation induced defects in future CMOS materials.

Rutgers team uses high resolution characterization tools to:

- **Determine composition, structure and electronic properties of gate stacks that use new (post-Si) materials**
- **Help determine physical and chemical nature of pre-existing and radiation induced defects**

Experimental studies of high-k on III-V and other substrates:

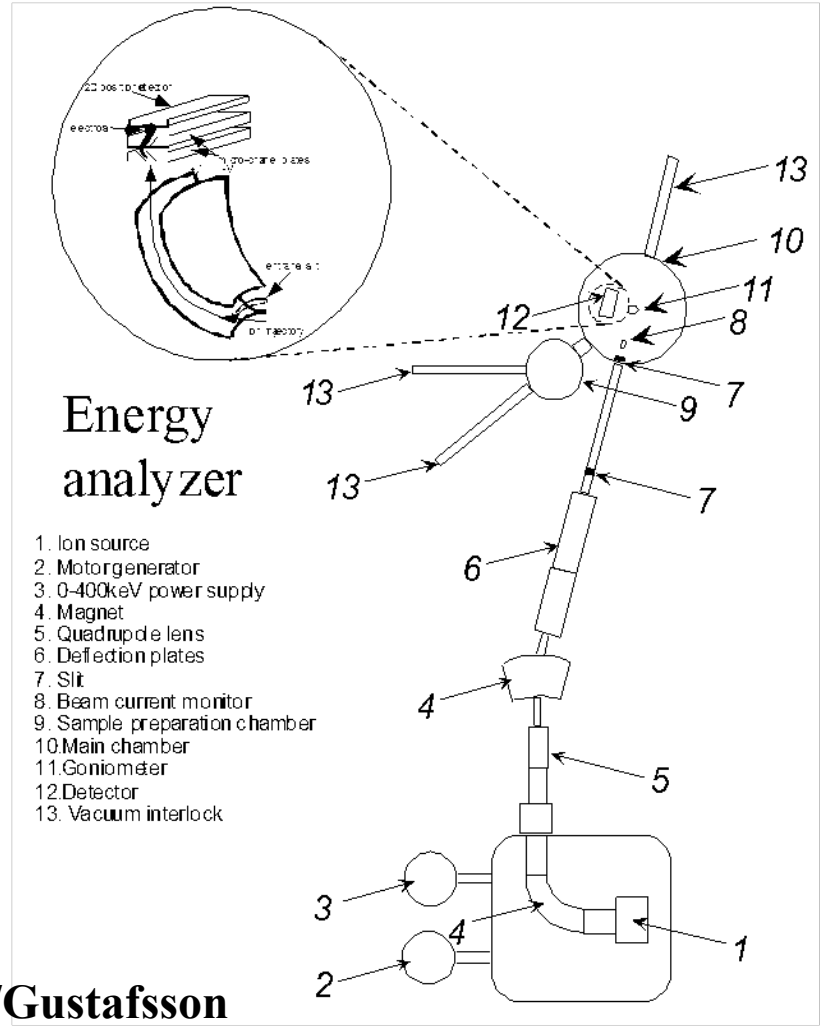
- **Composition and depth profiling – XPS, MEIS, RBS, SPM…**
- **Electronic structure – PES, IPE, optical and electrical methods**
- **Surface/interface passivation chemistry and relation to defects**

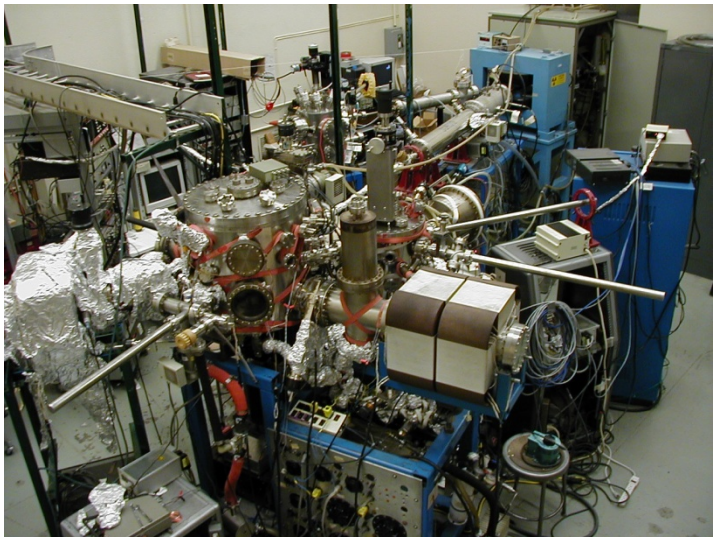
CMOS gate stack activities

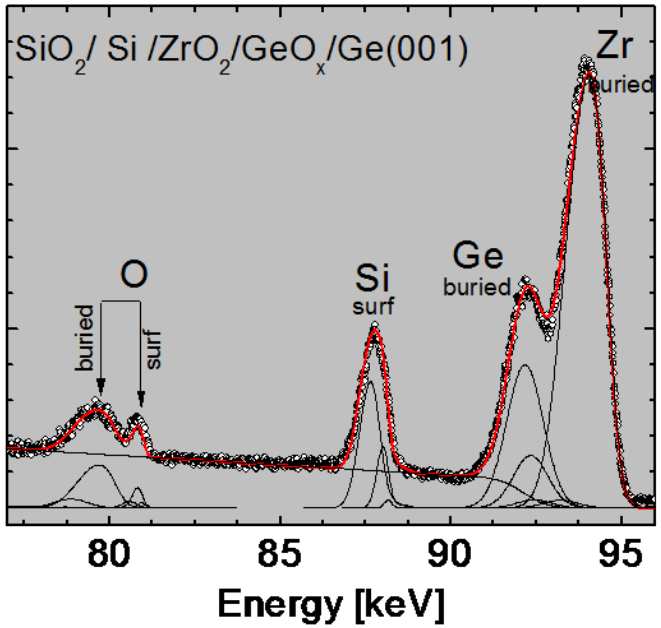
- Ion scattering - MEIS, RBS
- Electronic structure – XPS, UPS, Inverse PES, Internal PES
- Substrates: Si, SiGe, Ge, GaAs, InGaAs
- Etching chemistry and roughness
- Defects – intrinsic, process induced, radiation induced
- Electrical – CV, IV
- Film initiation and growth (esp. for ALD growth)
- Film stoichiometry and thickness for multilayer structures
- Microscopy - TEM, SEM, AFM….
- Influence of interface layers (diffusion barrier, growth initiator, work function engineering)
- Metal gate/high-κ dielectric film and interface stability
- Diffusion/atomic mobility (O, Si, N, metal, etc…)
- Epitaxial oxides and higher-K - e.g. STO/Si, La compounds

MEIS (Medium Energy Ion Scattering)

Low-energy version of RBS with high depth resolution (~ 3 Å vs. ~100 Å)



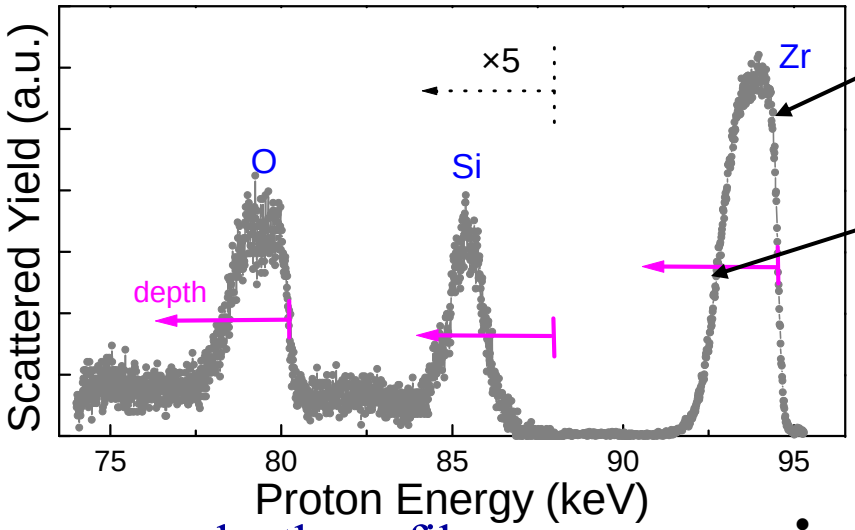


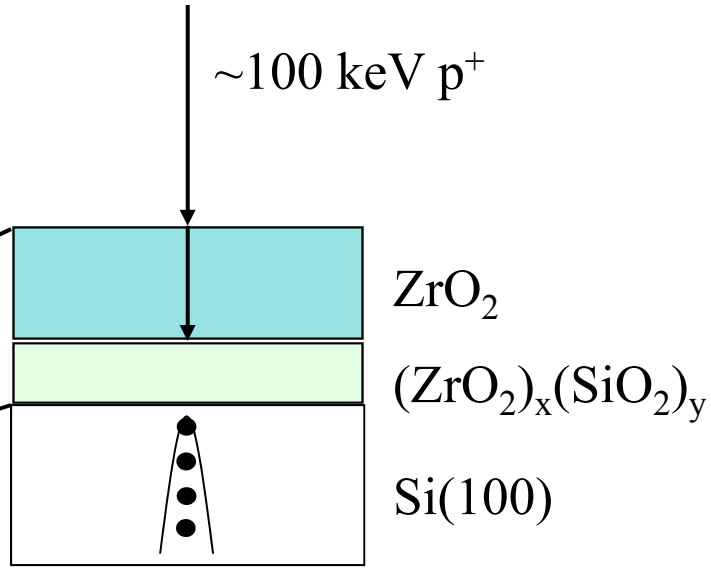


w/Gustafsson

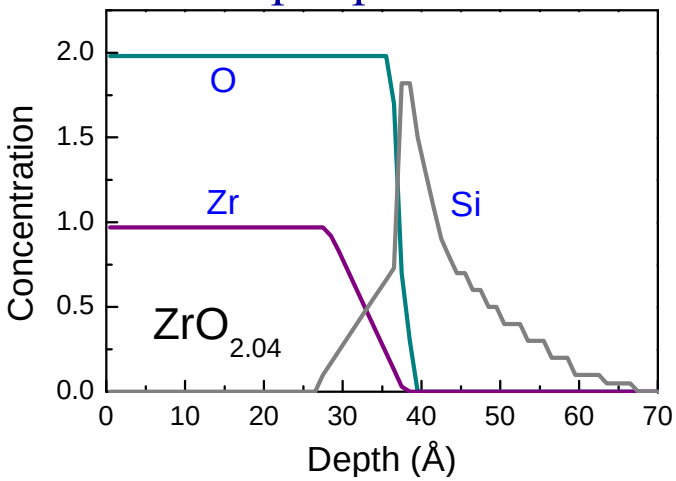
Ion scattering: MEIS

Backscattered proton energy spectrum





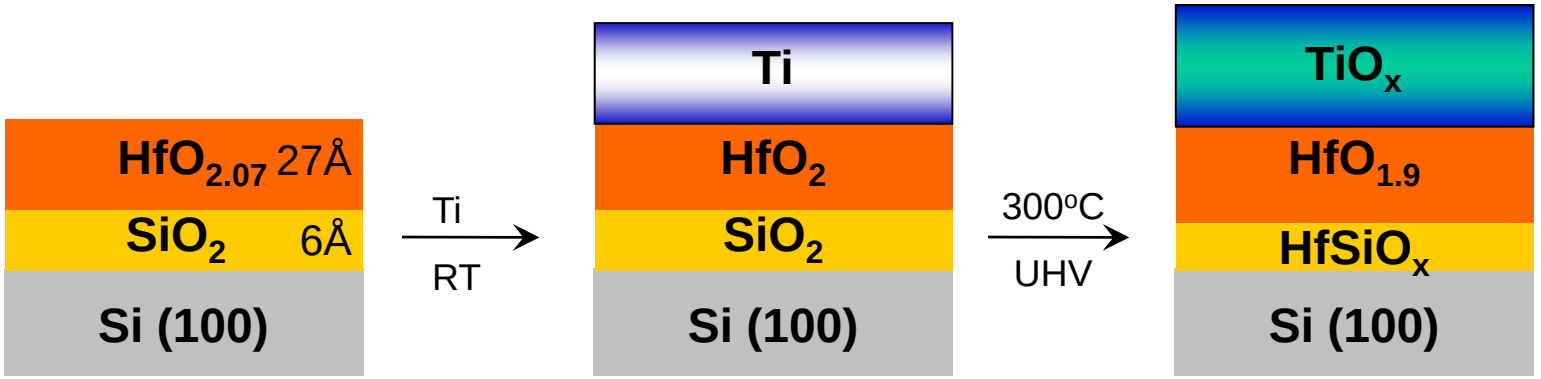
depth profile

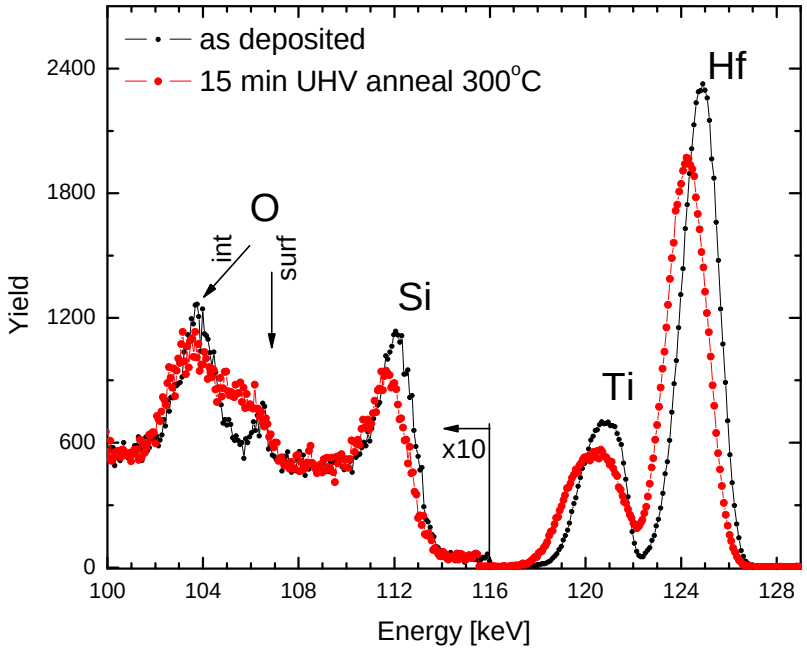


- **Sensitivity**:
  ≈ 10^{+12} atoms/cm^2 (Hf, Zr)
  ≈ 10^{+14} atoms/cm^2 (C, N)
- **Accuracy** for determining total amounts:
  ≈ 5% absolute (Hf, Zr, O), ≈ 2% relative
  ≈ 10% absolute (C, N)
- **Depth resolution**: (need density)
  ≈ 3 Å near surface
  ≈ 8 Å at depth of 40 Å

Gate metal effects on chemical stability of dielectrics

Metal as source or sink for oxygen and hydrogen





- Initial HfO_2 film has small amount of interfacial SiO_2 (~6-7Å) and excess of oxygen (~$HfO_{2.07}$)
- Deposited Ti forms uniform layer, no strong intermixing with HfO_2;
- Oxygen concentration in Ti layer is small

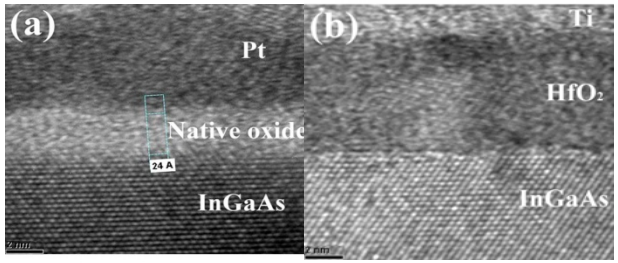
<u>After UHV anneal at 300°C for 15 min:</u>

- Lowering and broadening of Ti peak
- Hf and Si peak shift and O peak changes

⇒ Ti layer partially oxidized

Interface reduction (self-cleaning) during growth and processing

- "Self-cleaning" during ALD growth is a phrase that described the concomitant reduction and removal of surface oxides from a substrate during the ALD process. It has been observed by several groups (P.D. Ye et. al.,APL, 83, 180; M. Frank et. al., APL, 86, 152904; C. Hinkle et. al., APL, 92, 071901).



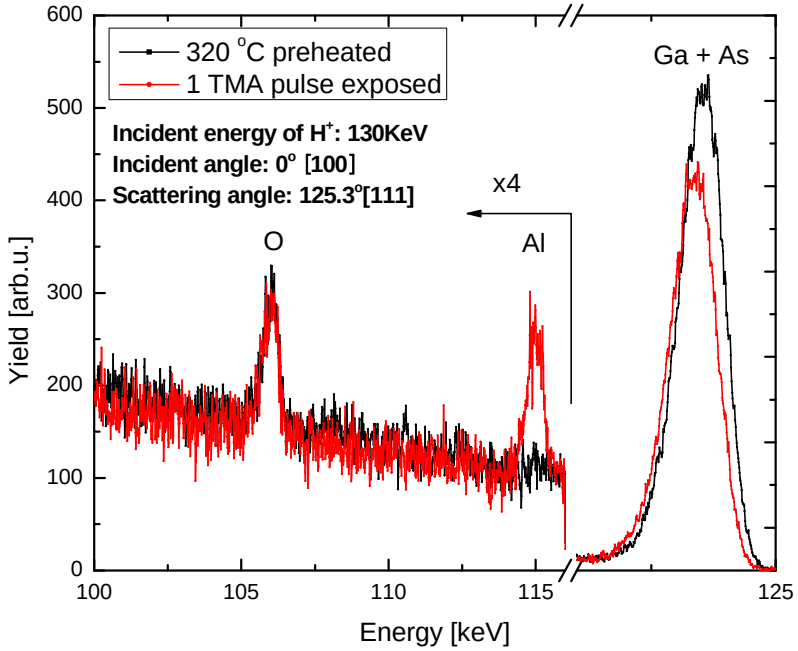
C.H. Chang et. al. (APL, 89, 242911)

- Some issues regarding "self-cleaning":

1. When does it occur? At the very first introduction of precursor or continuously through the growth?
2. Where do the surface chemical species go? Desorb or incorporate into the dielectric or substrate?
3. Can it help us prepare optimal gate stacks?
4. No detailed structural data reported regarding "self-cleaning".

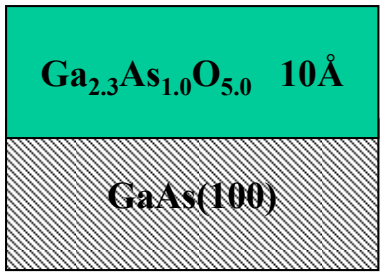
Native oxide reduction after 1 TMA pulse

In situ MEIS

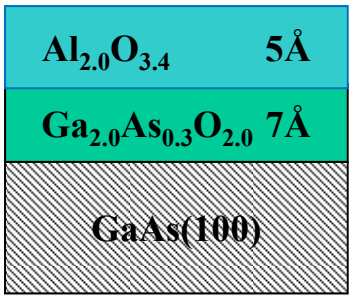


- **The O content in the Al oxide layer is 3.5 (×10^{15}at./cm^2), similar to the O decrease in the native oxide layer, 3.0 (= 4.6-1.6) ➔ O atoms from the native oxide layer form the Al oxide (the *only* oxygen source).**
- **The (Ga+As) density in the native oxide layer is reduced from (2.0+0.9) to (1.6+0.24) ➔ desorption of Ga and As.**

Starting substrate
(w. 10 Å native oxide)



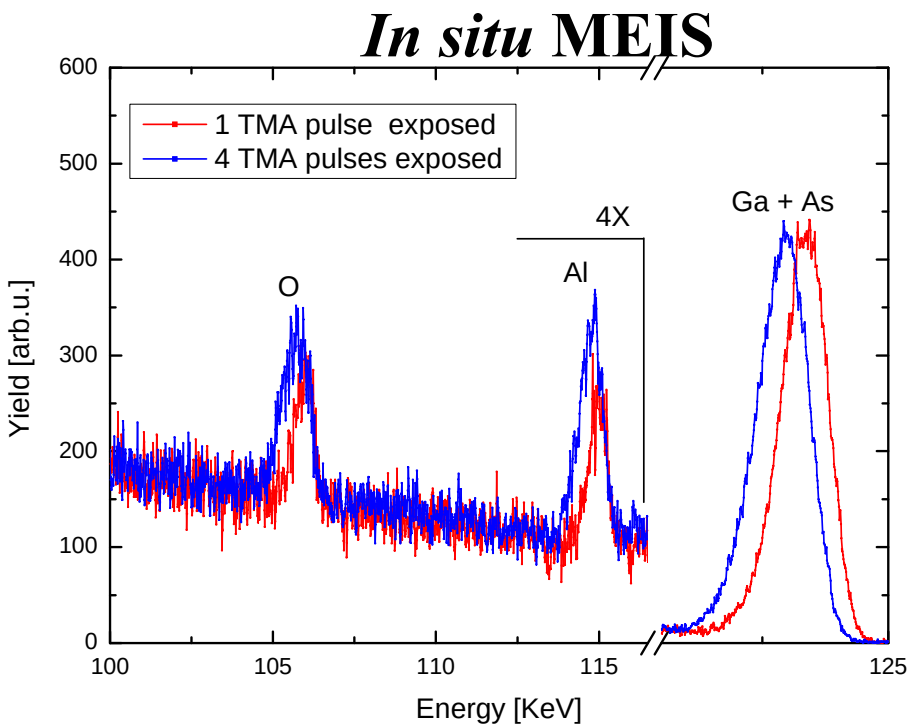
After 1 TMA pulse exposure
(w/o water)



Areal density (× 10^{15} at./cm^2)

		Preheated	1 TMA
Native oxide	Ga	2.0	1.6
	As	0.9	0.24
	O	4.6	1.6
Al oxide	O	n/a	3.5
	Al	n/a	2.0

Further native oxide reduction after 4 TMA pulses

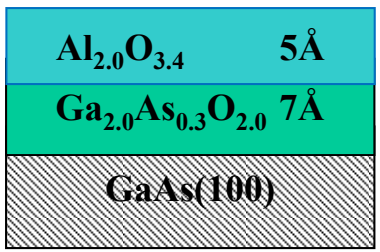


- **The O content in the native oxide layer decreases further, 1.6 to 1.1 ➔ further reduction of native oxides.**

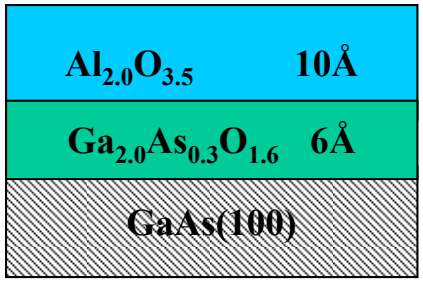
Areal density (× 10^{15} at./cm^2)

		Preheated	1 TMA	4 TMA
Native oxide	Ga	2.0	1.6	1.4
	As	0.9	0.24	0.21
	O	4.6	1.6	1.1
Al oxide	O	n/a	3.5	7.1
	Al	n/a	2.0	4.1

1 TMA pulse exposure w/o water

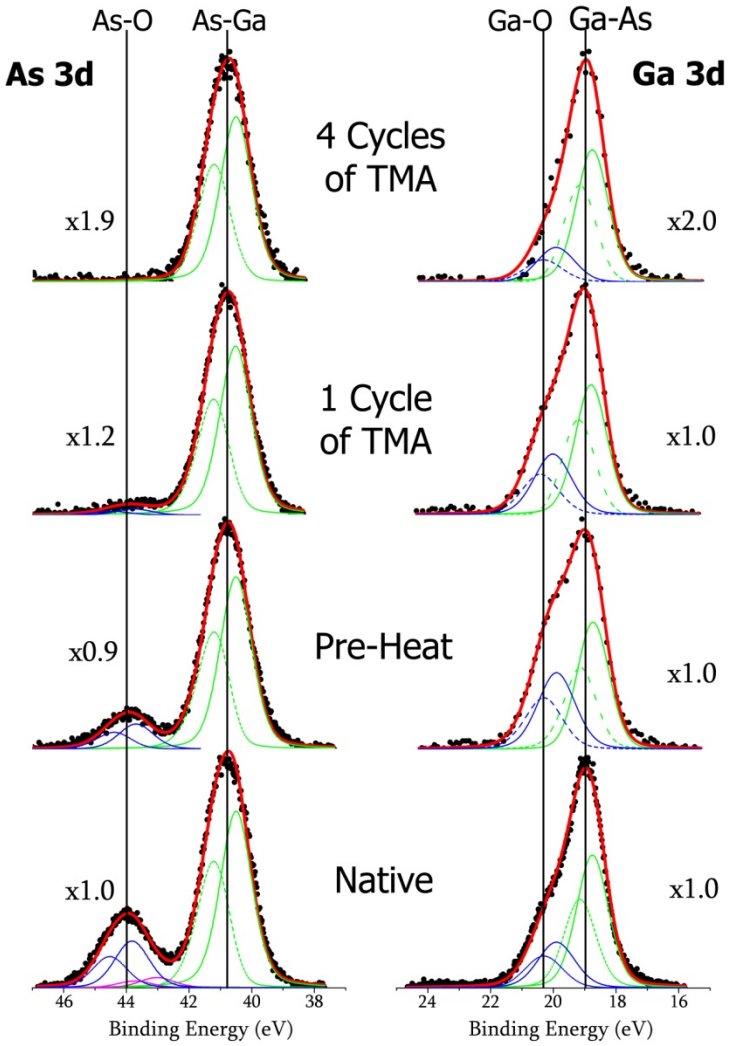


4 TMA pulse exposure w/o water



RUTGERS

Photoemission (XPS) during growth



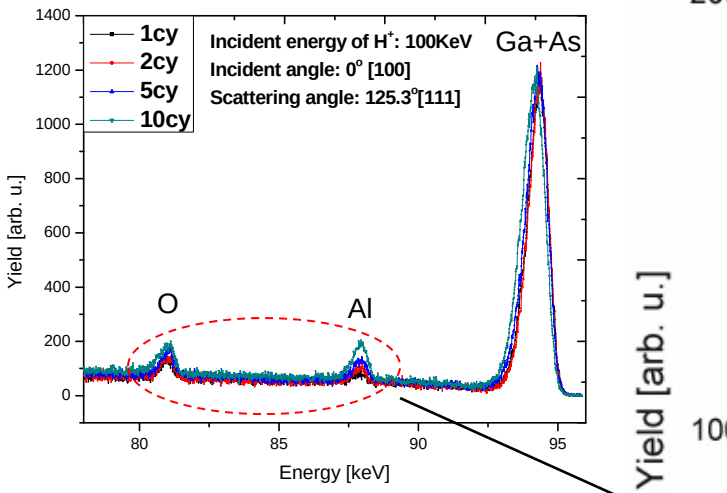
After preheating: Conversion of As_2O_3 (46% decrease) to Ga_2O_3 (47% increase) (relative to as-received wafer).

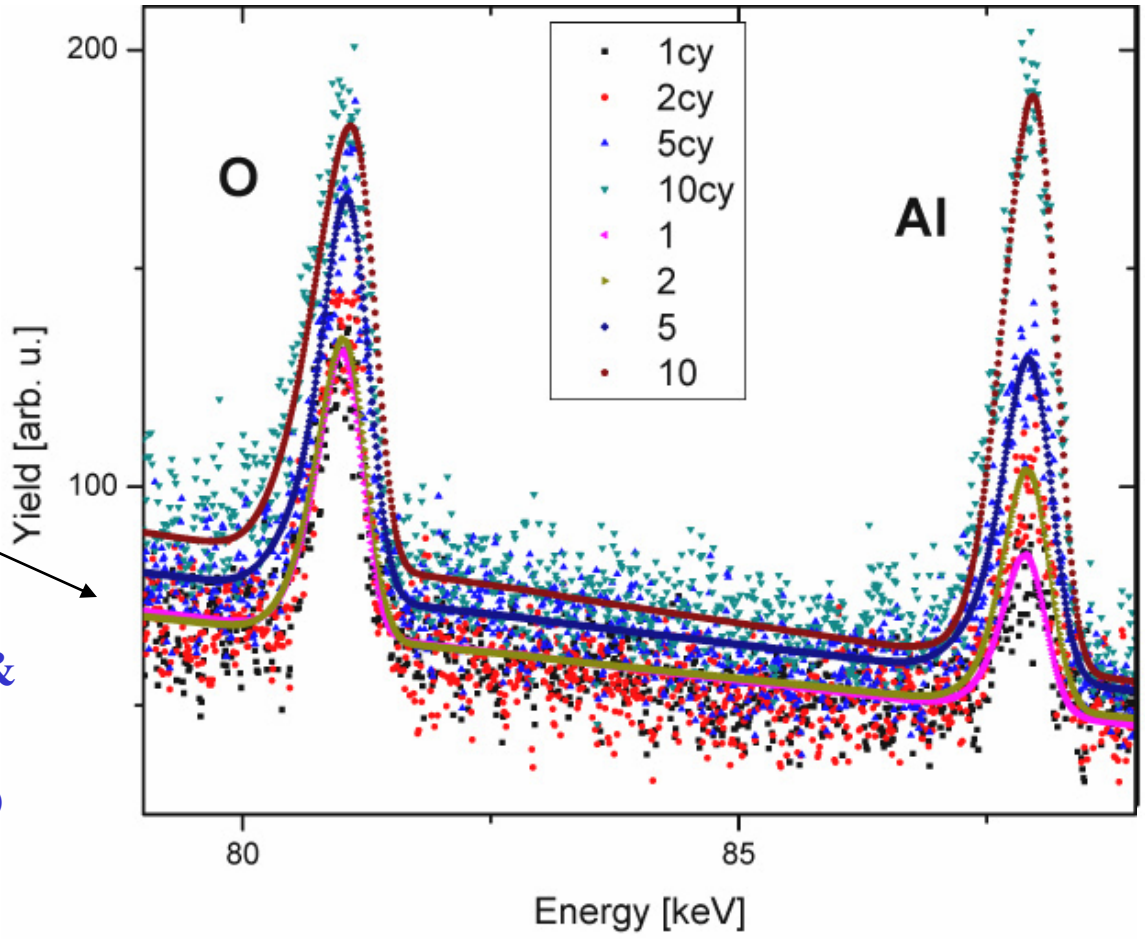
The native oxides in the preheated samples consist of a mixture of As_2O_3, As_2O_5 and Ga_2O_3. The Ga:As ratio (~2:1) is close to the one from MEIS (2.3:1).

After 1 TMA pulse: Decrease of the As-O (~75%) and Ga-O (~16%) peak areas, consistent with MEIS.

After 4 TMA pulses: Further decrease of As-O below the XPS detection level (to a lesser extent also Ga-O) - confirms the MEIS result.

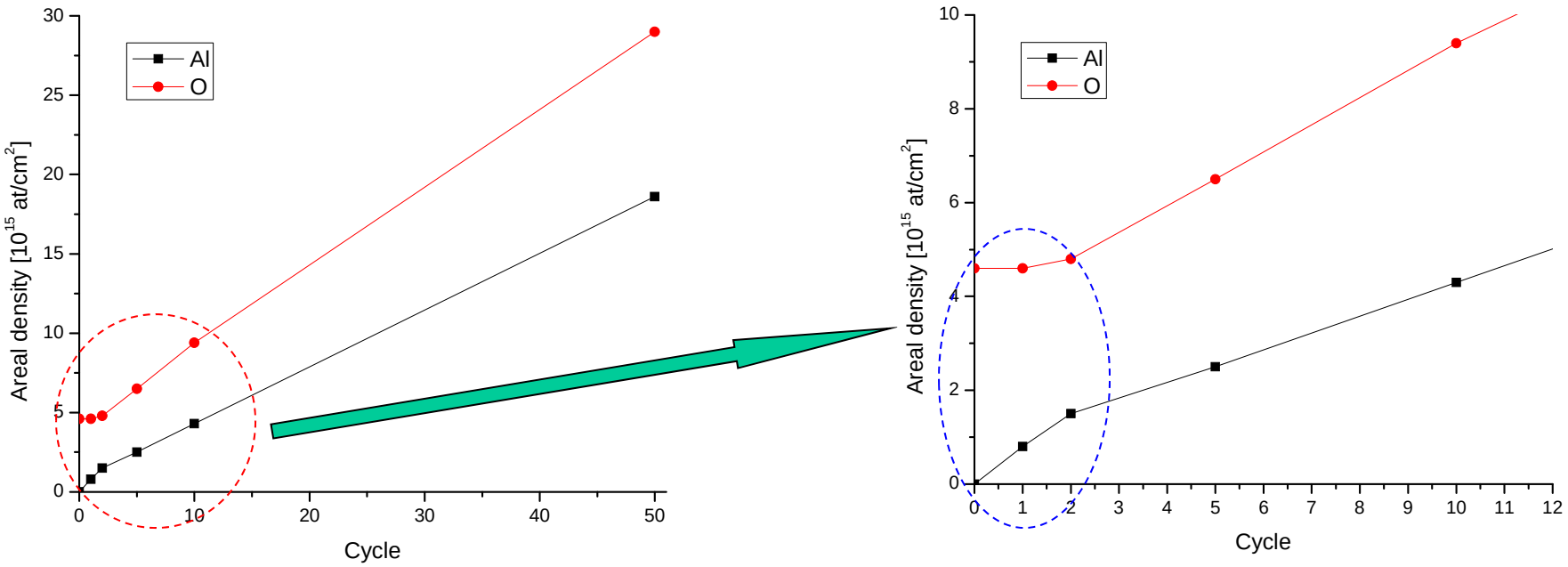
MEIS study of the growth rate of Al oxide





- Little O increase between 1 & 2 cycles while Al increases
  - ➔ Al oxide formation with O from the native oxides
  - ➔ Self cleaning continued

Linear Al oxide ALD growth after the 2nd cycle

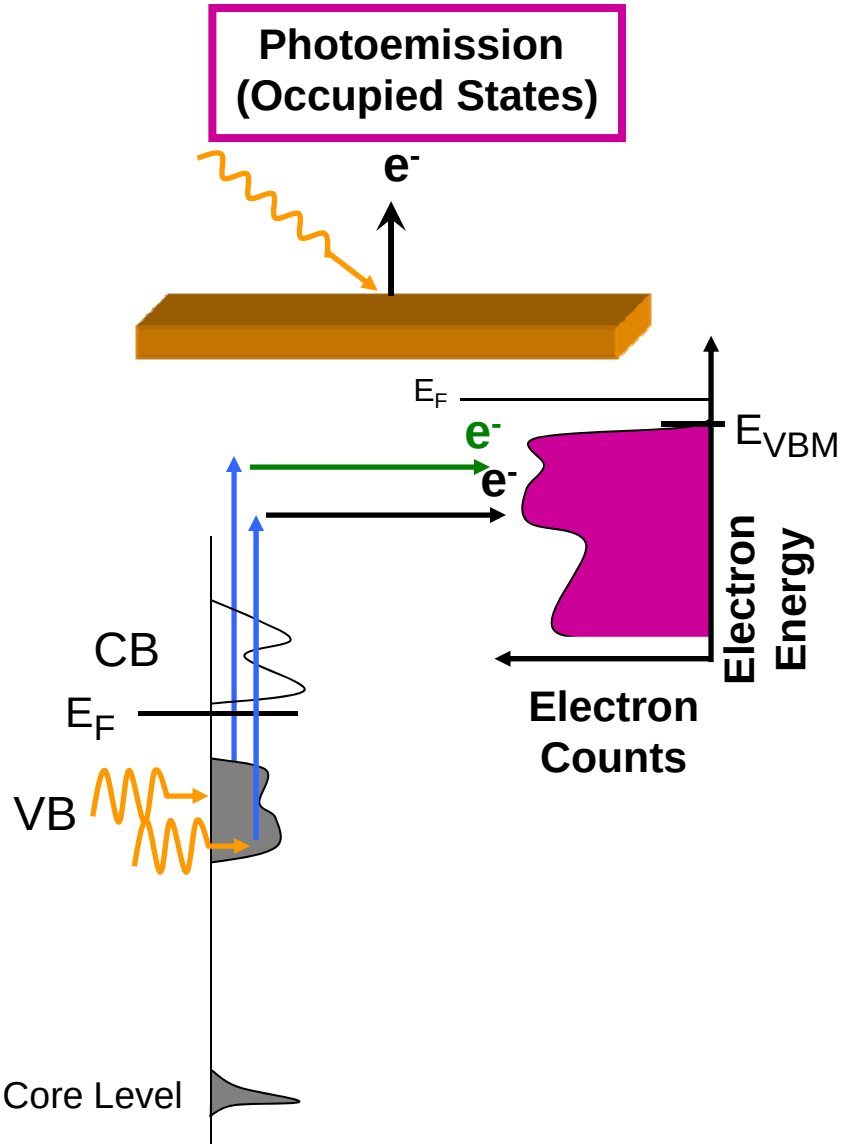


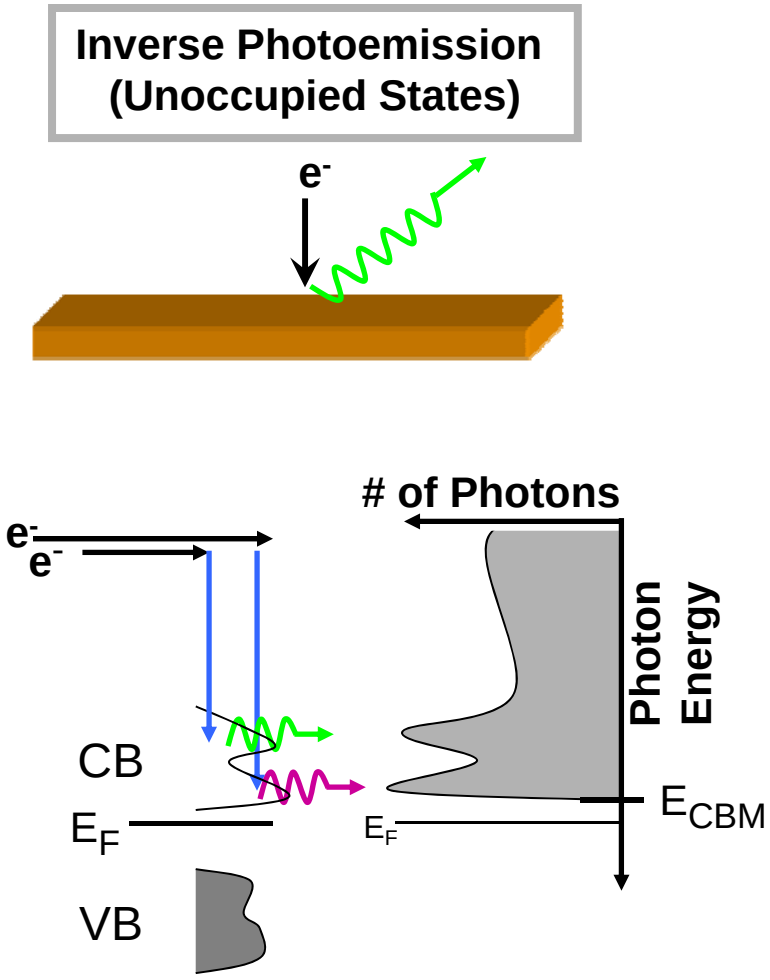
Areal Density (10^{15} at/cm^2)

Cycle	0 (pre-heated)	1	2	5	10	50
Al	0	0.8	1.5	2.5	4.3	18.6
O	4.6	4.6	4.8	6.5	9.4	29.0

- **After self cleaning (2nd cycle) the Al oxide growth rate becomes slower.**

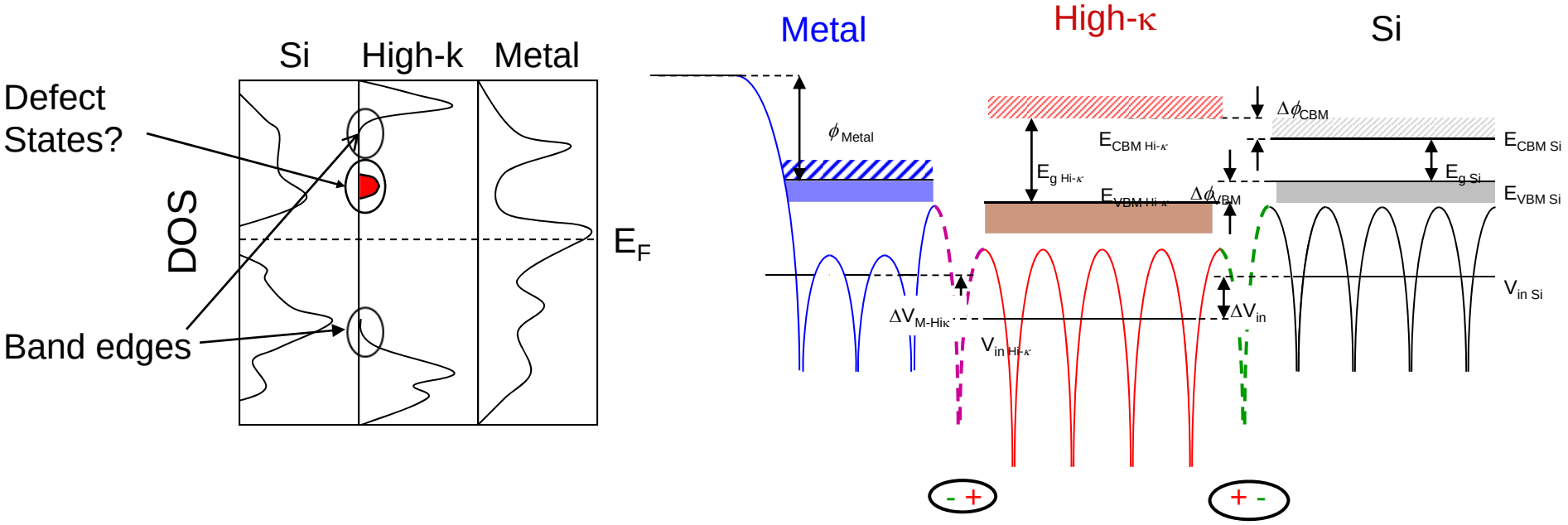
Experimental methods to determine electronic structure





w/Bartynski

Electronic structure across multilayer stacks



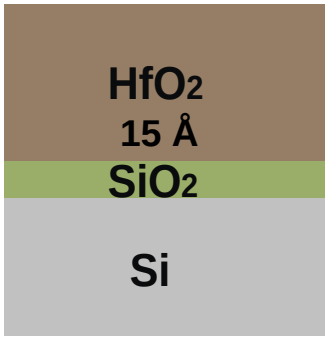
Band alignment, "effective" work function, energy gap…

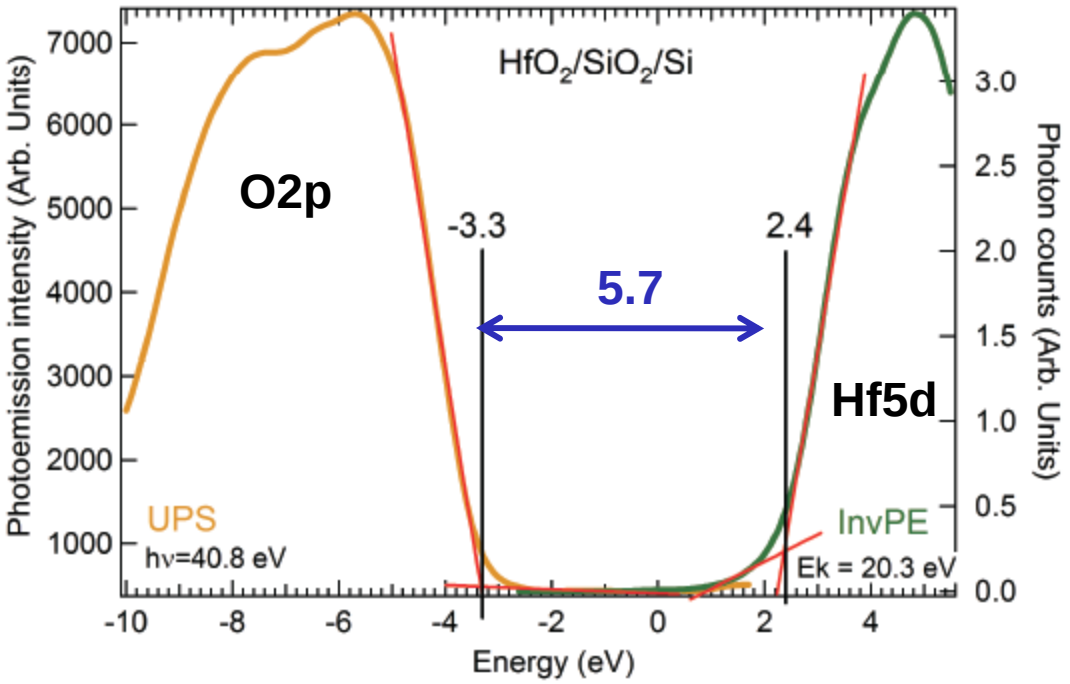
- Band edge energies determined in many ways – elec. and optical spec.
- Can we use spectroscopies to (i) measure energies and LDOS more precisely, (ii) determine interface dipoles and band alignment, and (iii) use interface engineering to control effective work function…

Photoemission and inverse photoemission of $HfO_2/SiO_2/Si$

Single chamber

UHV measurments





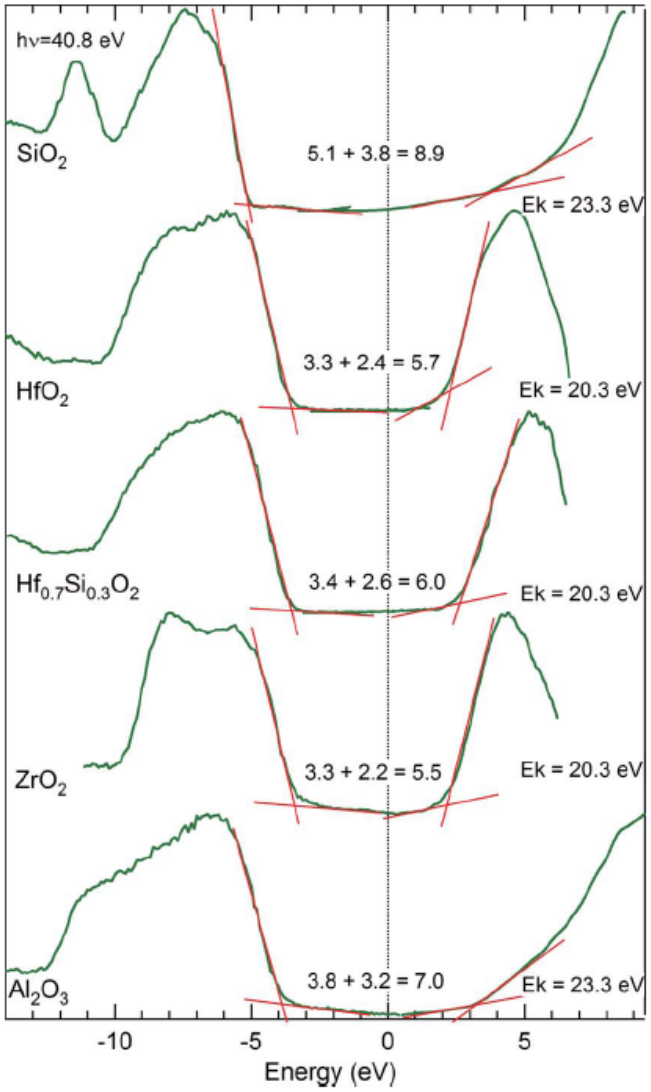
Gap determination

Substrate band edges determination

↓

Band offsets

Band alignment determination by photoemission and inverse photoemission



	Gap	VBO	CBO	χ
Si	1.1			4.1
SiO_2	8.9	4.5	3.3	1.3
HfO_2	5.7	2.7	1.9	2.5
$Hf_{0.7}Si_{0.3}O_2$	6.0	2.8	2.1	2.8
ZrO_2	5.5	2.7	1.7	2.7
Al_2O_3	7.0	3.2	2.7	2.5

Direct experimental determination of crucial parameters:

Gap, VBO, CBO and χ

Band offsets of ultrathin high-k oxide films with Si, Bersch et al., Phys. Rev. B 78 (2008) 085114

Fundamental understanding of band alignment (conduction band)

	Ru		Al		Ti	
Oxide	**Expt**	**MIGS**	**Expt**	**MIGS**	**Expt**	**MIGS**
HfO_2	2.4	2.5	1.5	1.9	1.8	1.9
$Hf_{0.7}Si_{0.3}O_2$	2.4	2.4	1.5	1.8	1.7	1.8
SiO_2	3.8	3.9	3.4	3.0	3.1	3.0
Al_2O_3	3.0	2.7	2.0	2.0	2.4	2.0

Agreement between experimental CBO and MIGS-predicted CBO when no metal-induced interface oxide is present.

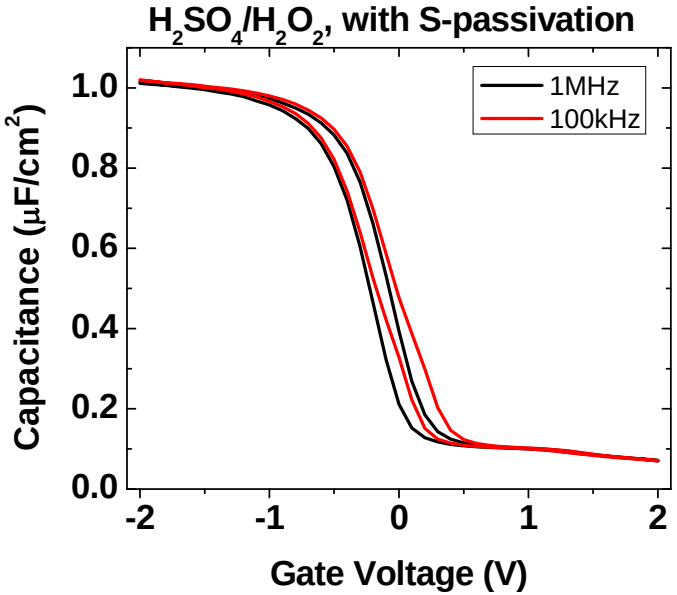
Band offsets of a ruthenium gate on ultrathin high-k oxide films on Si, Rangan et al., Phys. Rev. B 79 (2009) 075106

Aluminum gate interaction with ultrathin high-k oxide films on Si, Rangan et al., submitted APL

Band offsets of a Ti gate with ultrathin high-k oxide films on Si, Rangan et al., manuscript in preparation

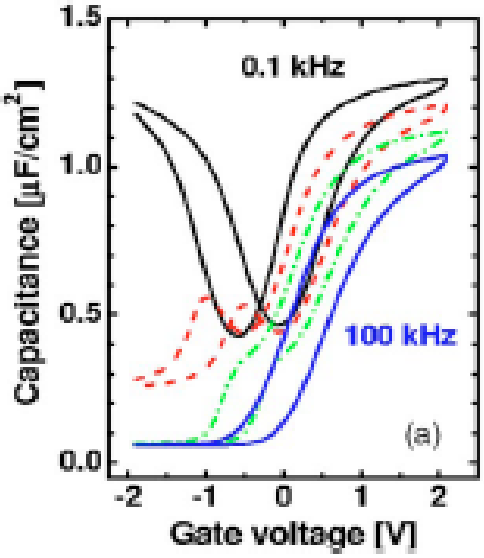
Ge surface chemistry and electrical defects

Cleaning	HF	HF/DIW/H_2O_2	H_2SO_4/H_2O_2 HF	H_2SO_4/H_2O_2
S-passivation	No	Yes	Yes	Yes
Q_i/e (cm^{-2})	$4.00x10^{13}$	$4.17x10^{12}$	$3.56x10^{12}$	$3.19x10^{12}$
ΔV_{FB_HS}(V)	0.31	0.29	0.22	0.15
D_{it} (eV^{-1} cm^{-2})	$3.80x10^{12}$	$1.66x10^{11}$	$8.91x10^{10}$	$6.23x10^{10}$



Prior work (lit.)

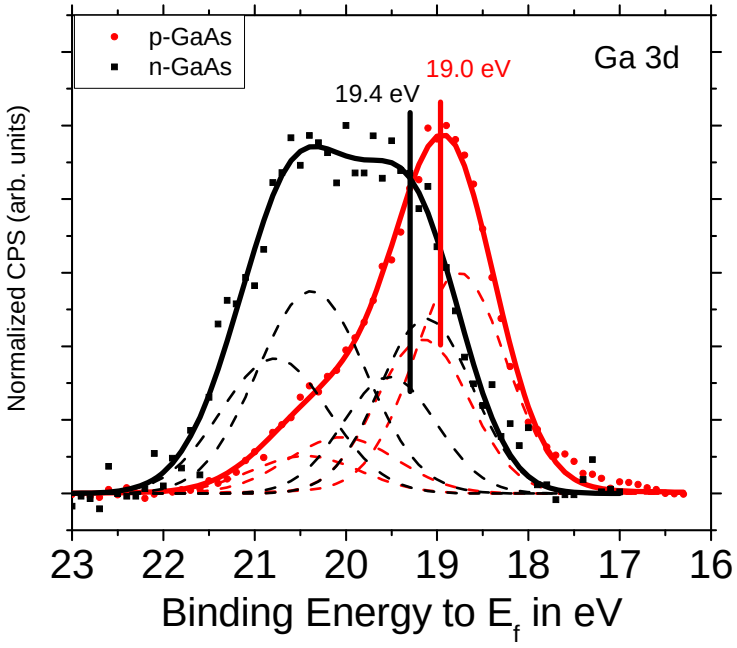
Current work

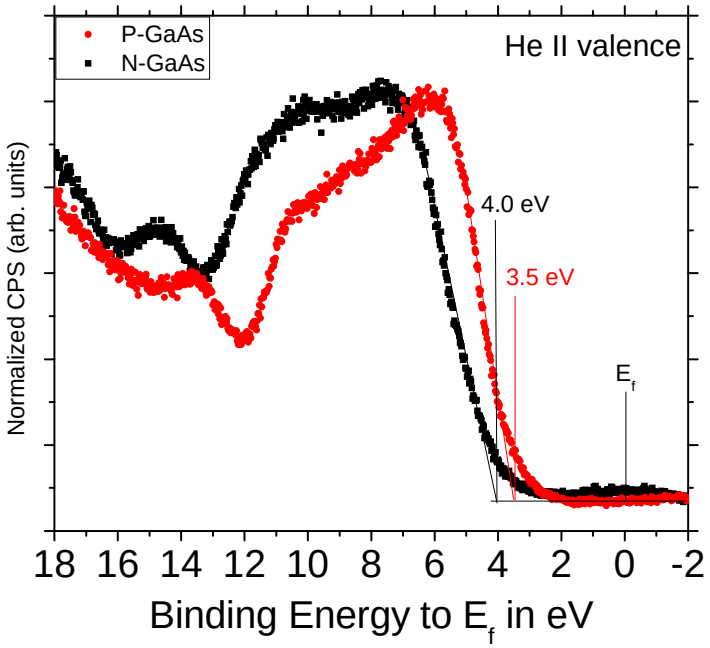


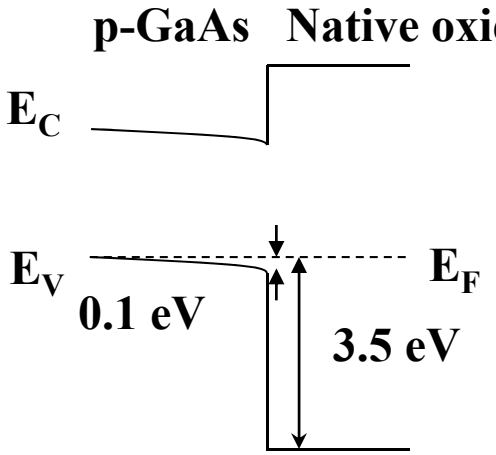
HfO_2 40A, hysteresis is ~0.15V.
Ge surface was first H_2SO_4/H_2O_2 treated.
No HF used before sulfidation in $(NH_4)_2S$.

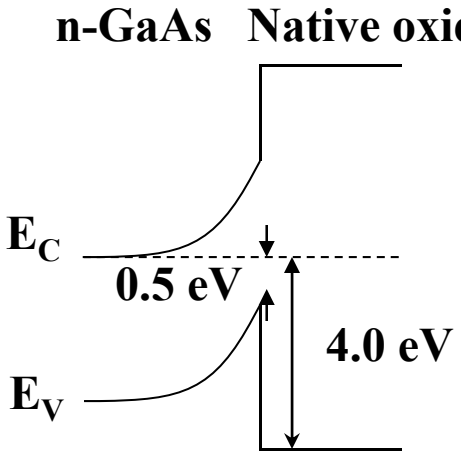
77A HfO_2, hysteresis is ~0.5V.
10% HF etching for 10mins before sulfidation in $(NH_4)_2S$.
APL 89, 112905 (2006)

Band alignment of GaAs native oxide



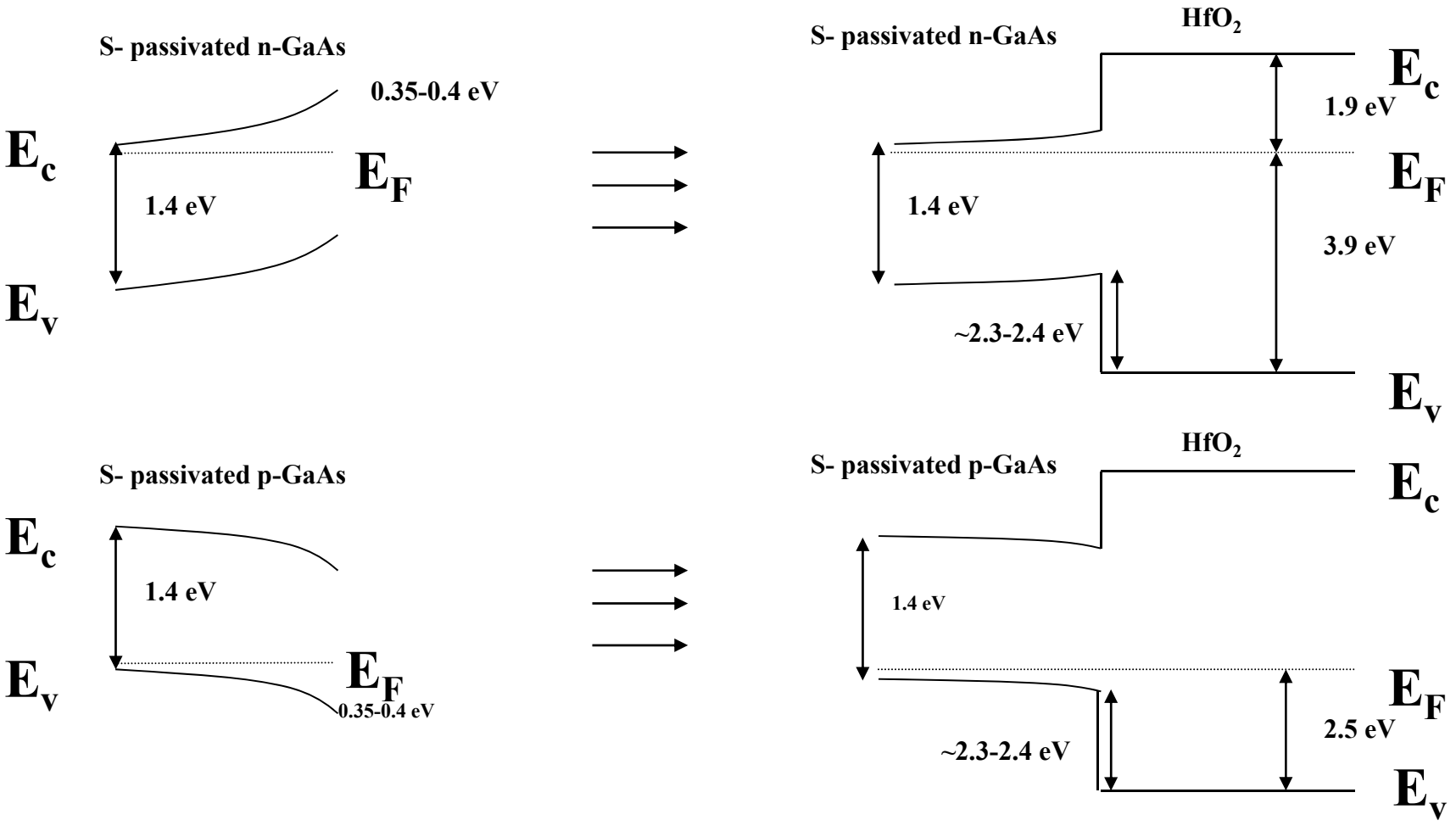






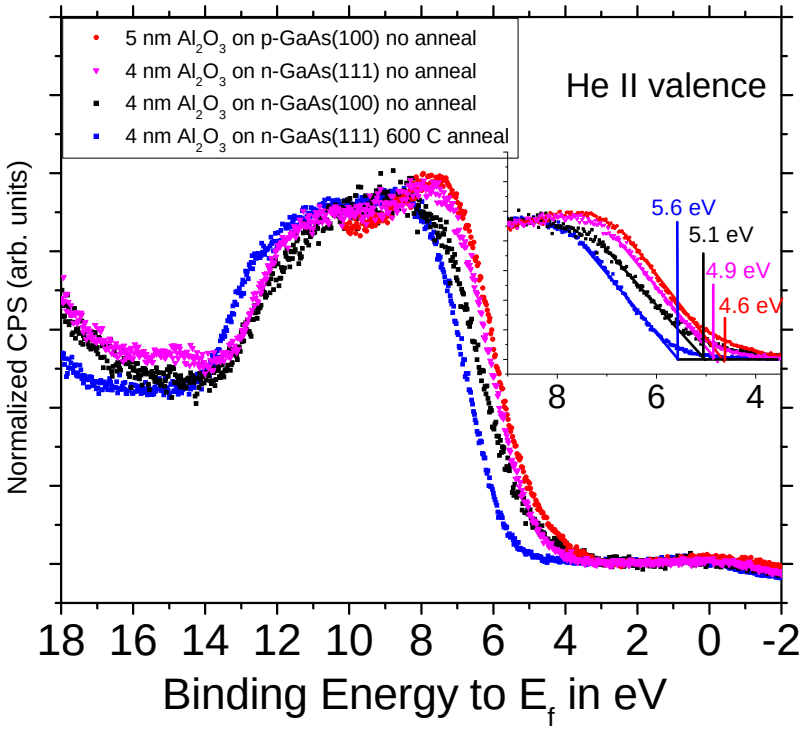
Pinning effects much stronger on n-GaAs than p-GaAs on native oxide surface

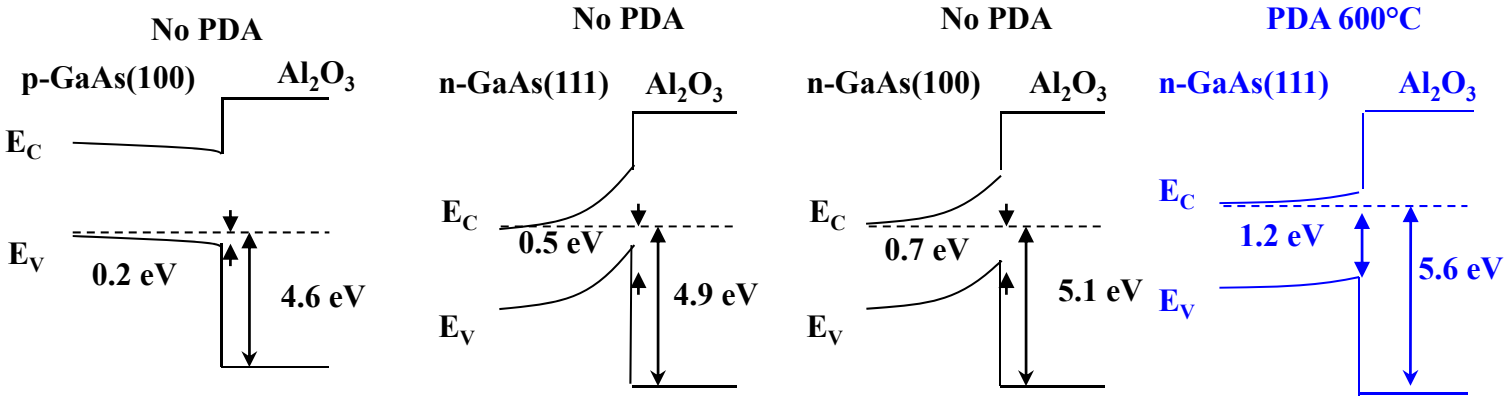
- On S-passivated III-V films E_f is partially pinned.
- After HfO_2 growth, much less pinning.
- Conduction and valance band offsets agree with literature.



Improvement of band alignment with post-processing on Al_2O_3/GaAs

- Post deposition anneal (PDA) @ 600°C in forming gas for ~ 15 sec yields improved energy level alignment for both n-GaAs and p-GaAs
- Valence band offset = 4.4 eV





Estimating the interface state density from band alignment

- Change in barrier height $\Delta\varphi$ vs change in work function $\Delta\Phi$
- Work function difference between n-GaAs and p-GaAs ≈ 1.4 eV
- Pinning parameter $S = \Delta\varphi/\Delta\Phi$ has been proposed to be related to the interface state density at $D(E_F)$ by:[2-3]

$$S = \frac{1}{[1 + (4\pi e^2/\varepsilon_i)\, D(E_F)\, \delta/A]}$$

- For no PDA 4nm Al_2O_3/GaAs, measured S = 0.3 eV/1.4 eV = **0.21**

  $D(E_F) = 5.2 \times 10^{11}$ cm^{-2} eV^{-1}
- For PDA 600°C 4nm Al_2O_3/GaAs, measured S = 1.0/1.4 = **0.71**

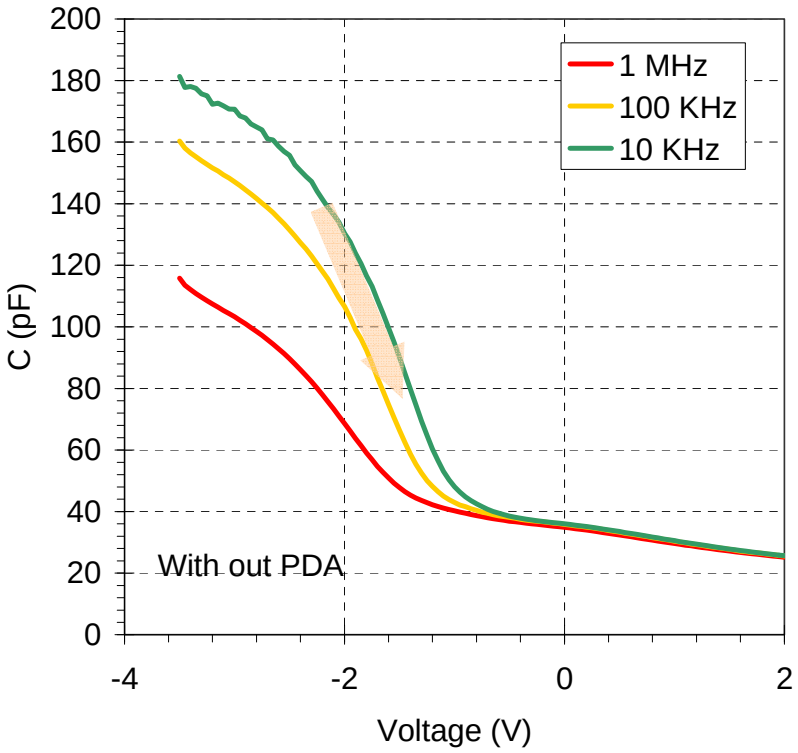
  $D(E_F) = 5.6 \times 10^{10}$ cm^{-2}eV^{-1}
- Maximum S value given by empirical formula determined by the *optical* dielectric constant:[4]

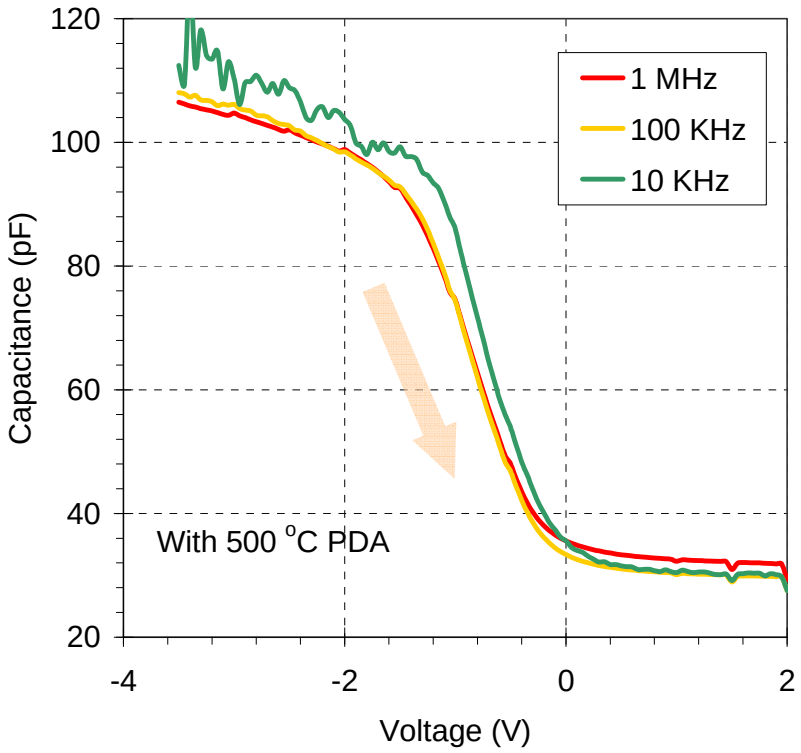
- For Al_2O_3, $\varepsilon_\infty = 3.1$, S = **0.69**

$$S = \frac{1}{1 + 0.1\,(\varepsilon_\infty - 1)^2}$$

2. C. Tejedor, E. Louis, F. Flores, *J. Phys. C* 10, 2163 (1977).
3. W. Mönch, "Semiconductor surfaces and interfaces" 3rd edition, Springer, New York (2001)
4. J. Robertson and J. Falabretti, *Mat. Sci. Eng. B* 136, 267 (2006)

4.5 nm thick III-V MOSCAPs (effect of 500 °C PDA)

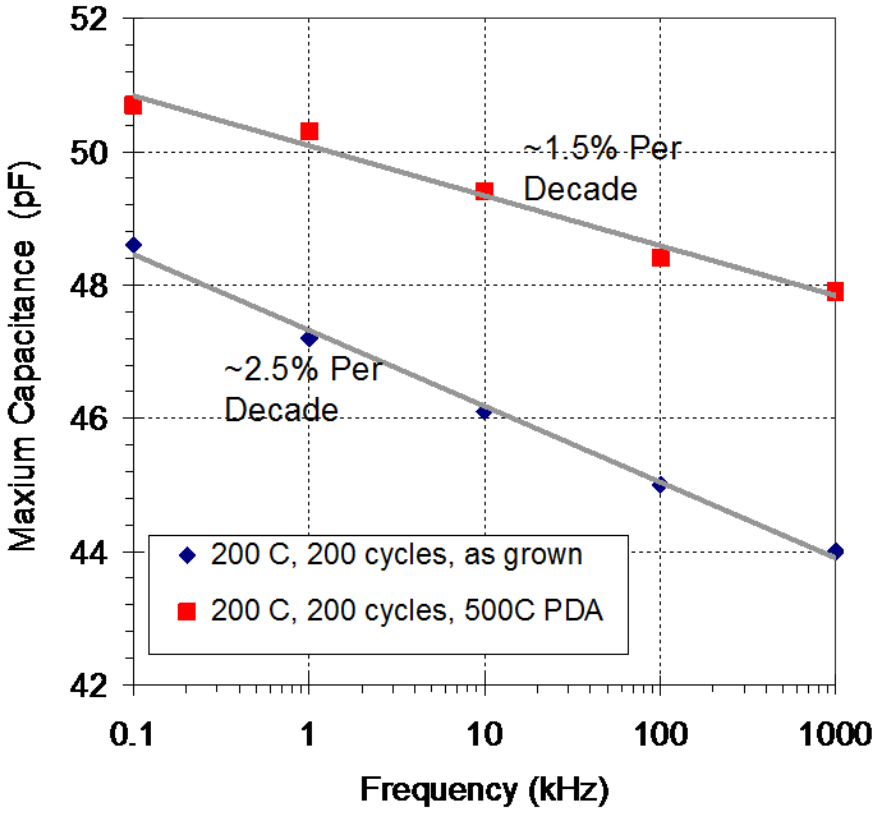




ALD growth at 320 °C; Device area: 2.5×10^4 μm².

For thin oxide, PDA significantly improves freq. dispersion, assuming that the MOSCAP CV behavior is dominated by the interface quality

Comments on MOSCAP frequency dispersion



Observation from experiments

1. Dispersion in accumulation capacitance
2. Rise in inversion capacitance of individual CV curves
3. Lateral shift in the CV curves; almost linear dispersion variation with respect to log(f)
4. Very slow "turn-on" or "stretch out" of CV
5. Almost linear dispersion variation with respect to log(f)

With improved annealing techniques, one should be able to minimize the bulk traps

1 and 2 above can be attributed to interface states.

3, 4, 5 may be explained by the presence of bulk/border traps

Post-silicon CMOS take home messages:

- High-K dielectrics and metal gates are in product!
- Very good devices can and have been grown on Ge and III-Vs.
- Electrical properties a strong function of surface passivation.
- Favorable band alignment found for some passivation and film growth conditions. Fermi level pinning (of interface defects?) appears not critical if film grown properly.
- Oxides of Ge and III-V's less stable thermally and electrically relative to SiO_2; can be consumed during high-K growth.
- Tendency of high-K to be partially reduced by Si substrate or gate not present for Ge and III-V's.
- Metallization materials and processes strongly affect interface chemistry and electrical properties.
- Sulfur passivation of semicond. surface helps in some systems.
- Si monolayers at interface appear helpful in minimizing defects.

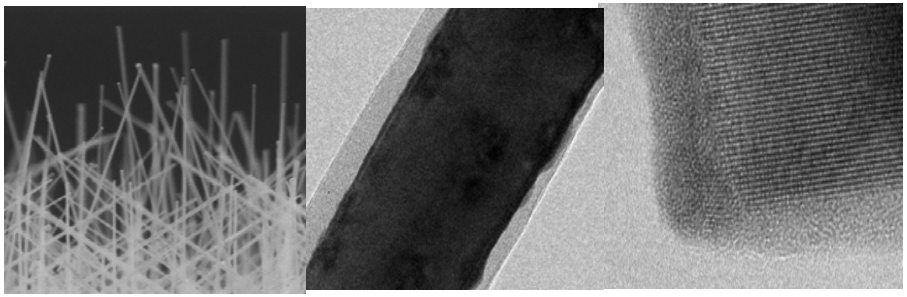
Recent MURI-related publications

- S. Rangan, et al; Aluminum gate interaction with ultrathin high-k oxide films on Si, accepted.
- H.D. Lee, et al; Reduction of native oxides on GaAs during atomic layer growth of Al_2O_3, accepted.
- S. Rangan, et al; *Band offsets of a ruthenium gate on ultrathin high-κ oxide films on silicon*, Physical Review B **79**, 075106 (2009).
- E. Garfunkel, et al; *Defects in CMOS Gate Dielectrics*, Defects in Microelectronic Materials and Devices: Edited by D. Fleetwood, S. Pantelides, and R.D. Schrimpf, CRC Press 2008 Chapter 11, pp 341-358.
- E. Bersch, et al; *Band offsets of ultrathin high-κ oxide films with Si*, Physical Review B **78**, 085114 (2008).
- S. Rangan, et al, *GeO_x interface layer reduction upon Al-gate deposition on a HfO_2 /GeO_x/Ge stack,* Appl. Phys. Lett. 92, 172 (2008).
- C.L. Hsueh, et al; Effect of surface oxidation and sulfur-passivation on Ge based MOS capacitors.

These and other papers can be downloaded at: http://garf.rutgers.edu

Future directions

- Focus further on III-V and Ge CMOS materials
  - **Correlate defect generation rate with E_{gap} and e-h pair generation probability of semiconductor and metal layers adjoining dielectric**
  - **Correlate physical and electrical measurements of "intrinsic" and "radiation induced/enhanced" defects**
  - **Explore E_f pinning and relation to radiation induced defects**
  - **Monitor H/D concentration/profiles in post-silicon materials**
- Si, Ge and III-V nanowire devices



- Radiation-induced defects in organic electronics, MEMS, graphene-based devices