

Materials stability, band alignment and defects in CMOS nanoelectronics

Team members: L. Yu, T. Feng, H.D. Lee, C.L. Hsueh, A. Wan, Q. Jiang, L. Goncharova, S. Rangan, D. Mastrogiovanni, E. Bersch, O. Celik, R. Bartynski, L. Feldman, T. Gustafsson and E. Garfunkel
Departments of Physics and Chemistry
Rutgers University, Piscataway, NJ

Collaborators:

Vanderbilt team; Sematech team - Bersuker, et al.

plus researchers at NIST, NCSU, Stanford, IMEC, UT-A, UT-D, Penn State, UCSB, IBM, Intel, AMAT, TI, Freescale, Taiwan

Support: Vanderbilt MURI (AFOSR) and SRC

Motivation: Help develop a fundamental understanding and control of radiation induced defects in future CMOS materials.

Rutgers team uses high resolution characterization tools to:

- **Determine composition, structure and electronic properties of gate stacks that use new (post-Si) materials**
- **Help determine physical and chemical nature of pre-existing and radiation induced defects**

Experimental studies of High-k on Ge and III-V substrates:

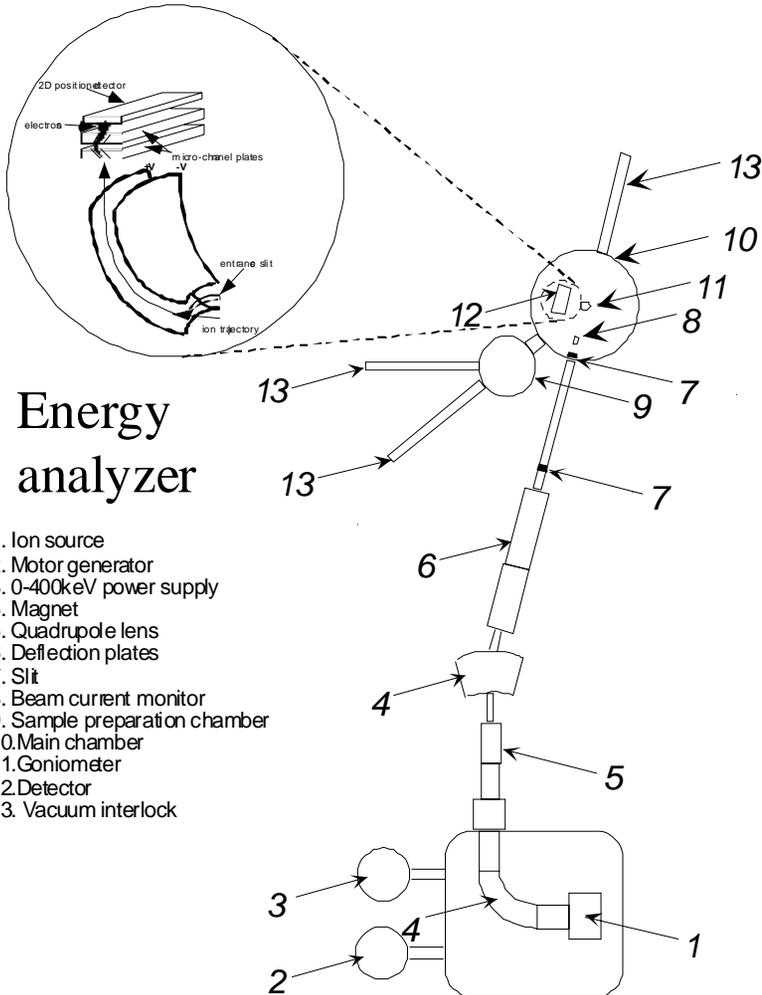
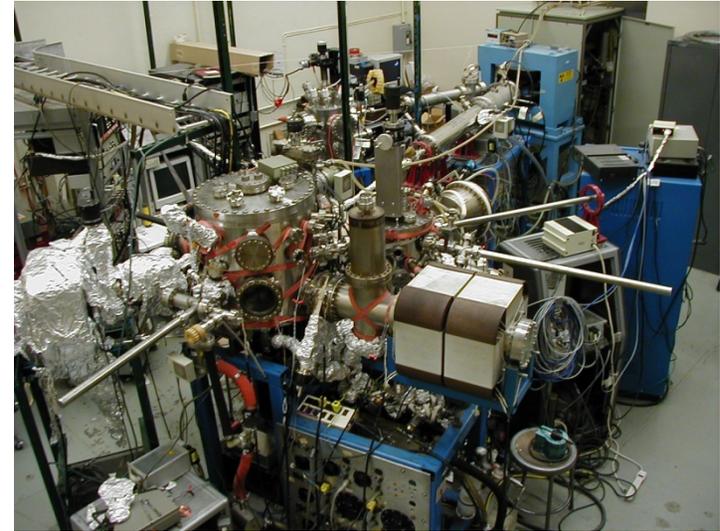
- **Composition and depth profiling –XPS, MEIS, RBS, SPM...**
- **Electronic structure – PES, IPE, optical and electrical methods**
- **Surface/interface passivation chemistry and relation to defects**

Current Rutgers work on CMOS gate stacks

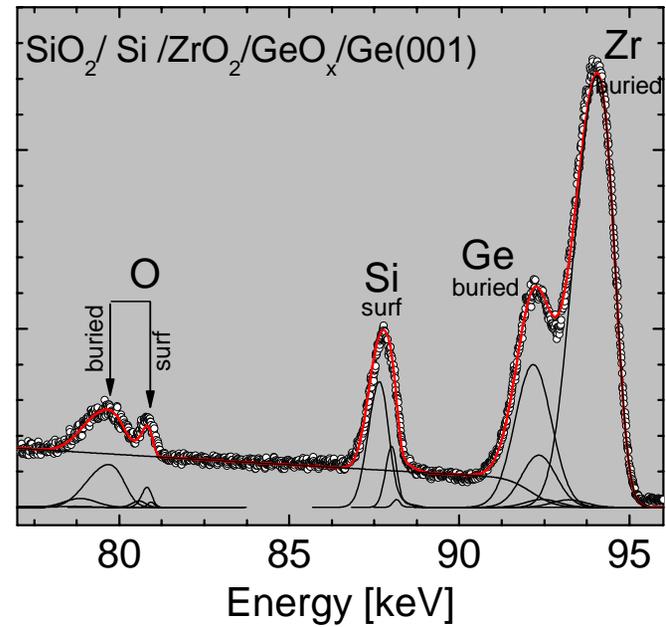
- Ion scattering - MEIS, RBS, LEIS
- Electronic structure – XPS, UPS, InvPES, IntPES
- Microscopy - TEM, SEM, AFM....
- Alternative substrates: Ge, GaAs, InGaAs
- Defect – radiation induced, processing induced, etc.
- Etching chemistry and roughness
- Film stoichiometry and thickness for multilayer structures
- Diffusion/atomic mobility (O, Si, N, metal, etc...)
- Dopant profiling and diffusivity – As, Sb, Bi, In, Ga
- Film initiation and growth (esp. for ALD growth)
- Influence of interface layers (diffusion barrier, growth initiator, work function engineering)
- Metal gate/high- κ dielectric film and interface stability
- Impurity concentration/profile – C, H, ...
- Epitaxial oxides - e.g. STO/Si, La compounds

MEIS (Medium Energy Ion Scattering)

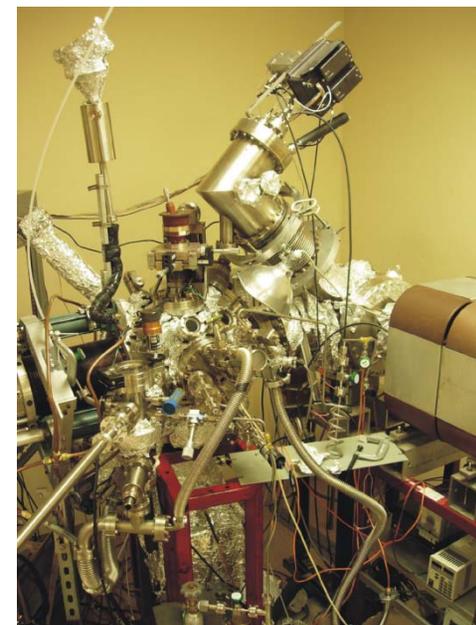
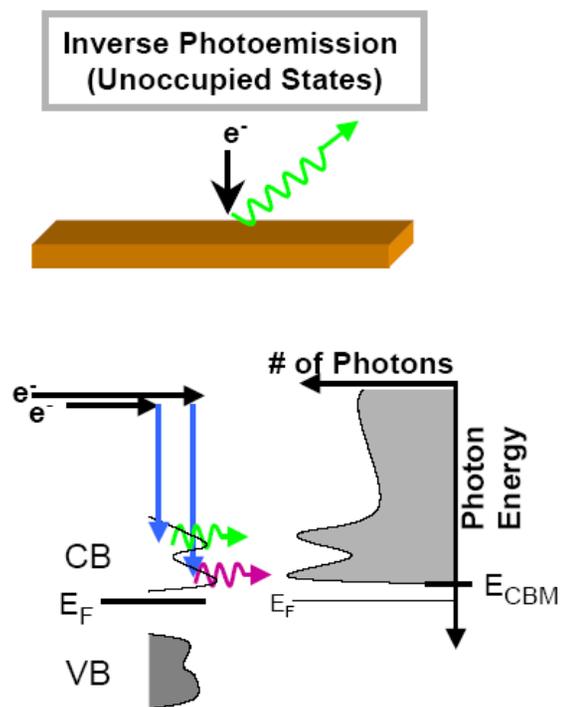
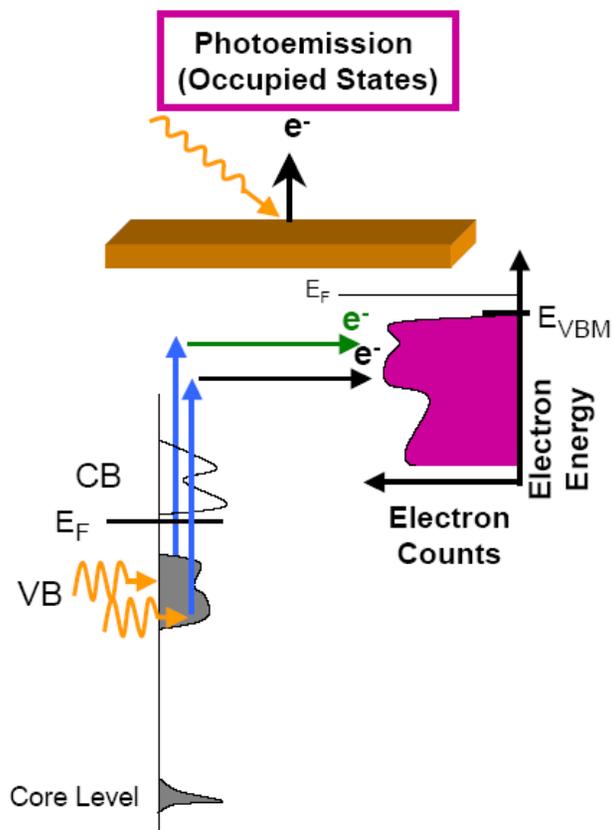
Low-energy version of RBS with high depth resolution ($\sim 3 \text{ \AA}$ vs. $\sim 100 \text{ \AA}$)



1. Ion source
2. Motor generator
3. 0-400keV power supply
4. Magnet
5. Quadrupole lens
6. Deflection plates
7. Slit
8. Beam current monitor
9. Sample preparation chamber
10. Main chamber
11. Goniometer
12. Detector
13. Vacuum interlock

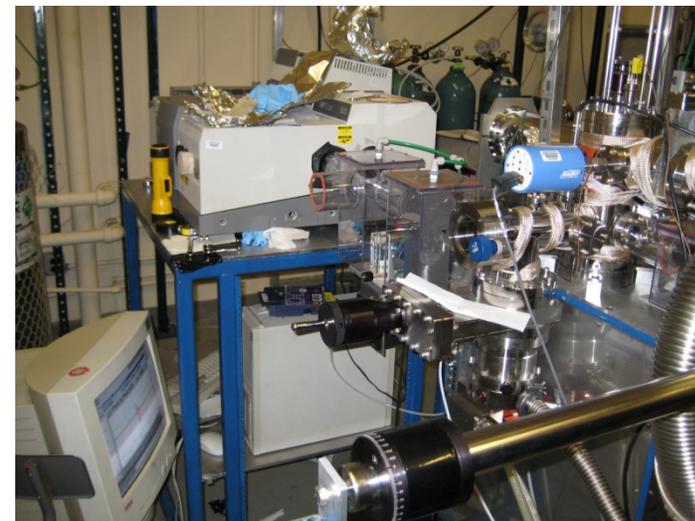
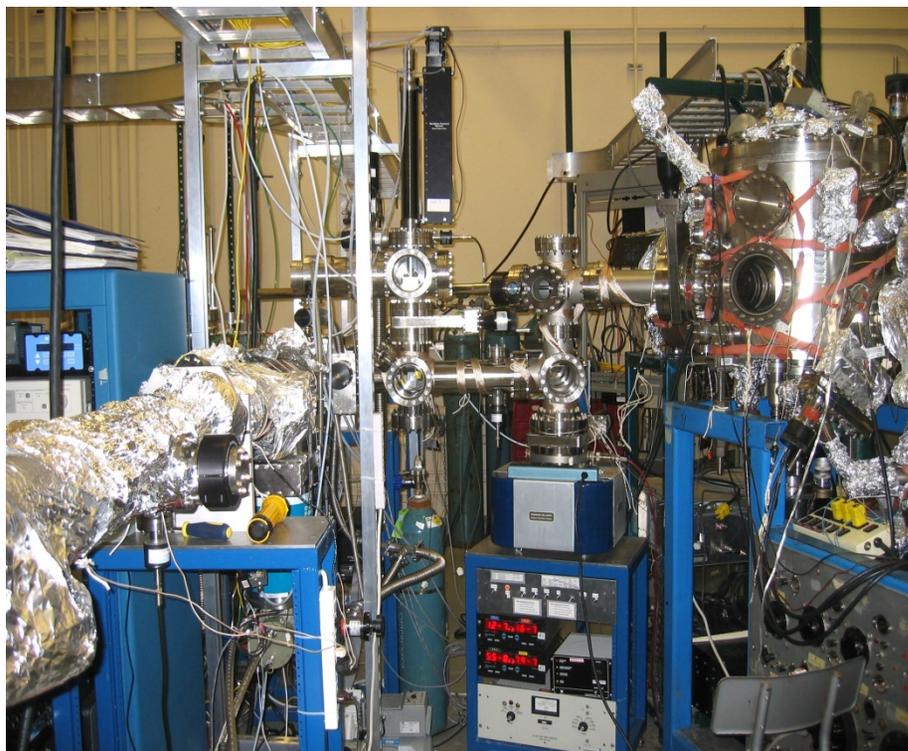


Electronic structure and band alignment

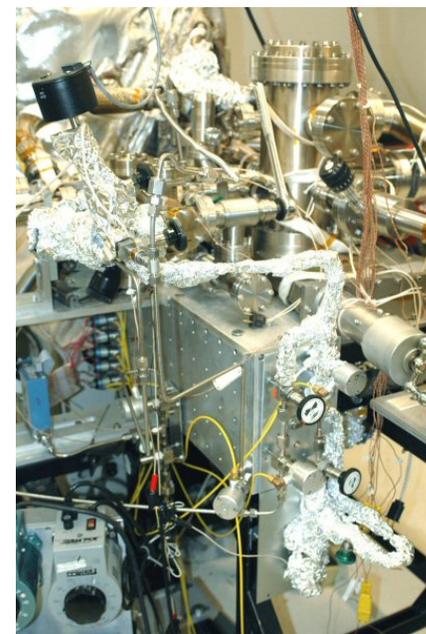


Other newly installed/commissioned equipment

UHV transfer system for growth and film analysis



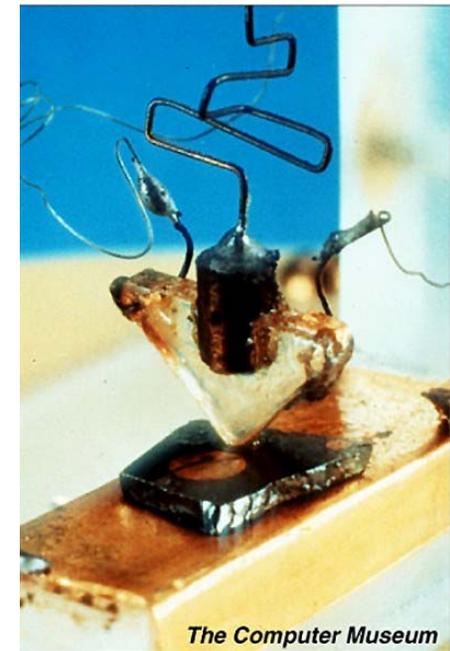
Several ALD growth systems



**Not shown: New photoemission system (XPS and UPS);
new electrical testing system (Keithley 4200)**

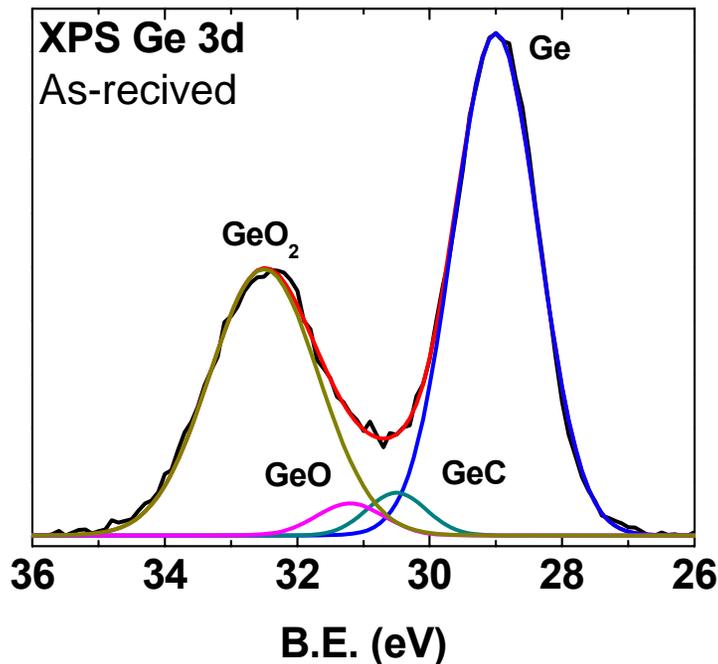
Several Ge MOSFET issues

- Unlike SiO_2 , GeO_2 is relatively **unstable** and dissolves in water. GeO is less water soluble, but more defective.
- Film defects, interfacial GeO_x , and impurities such as CH_x and GeC increase defect density and degrade device performance. **How to create an optimal interface?**
- Can a high-K dielectric be integrated on a Ge channel?
- Ge good for PMOS **and** NMOS?



Native oxides and carbon on Ge

None of the reported wet-chemical cleaning methods leads to an impurity-free Ge surface. Alternative approach: Convert hard-to-remove species into other chemical species which are easier to remove.



Some chemistries explored:

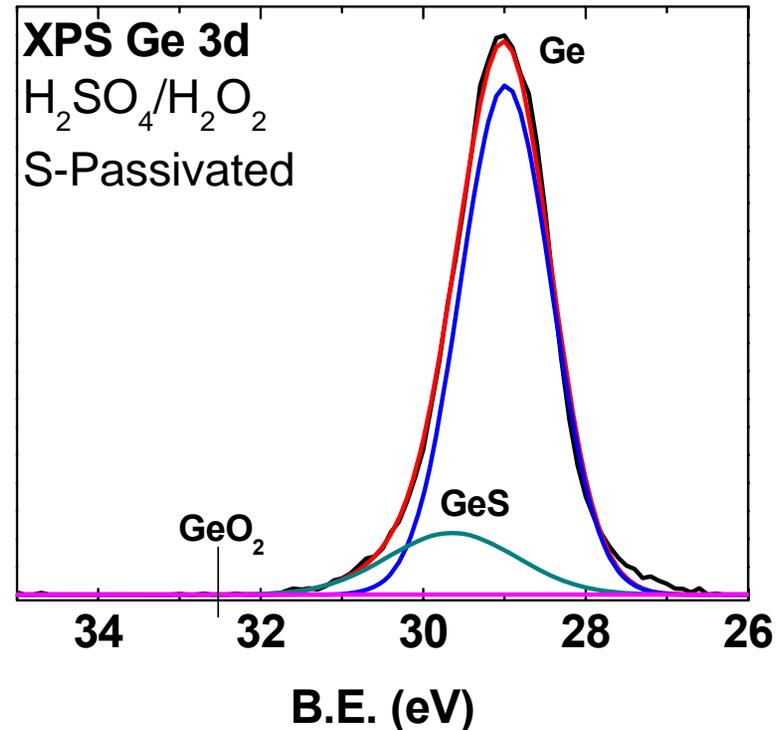
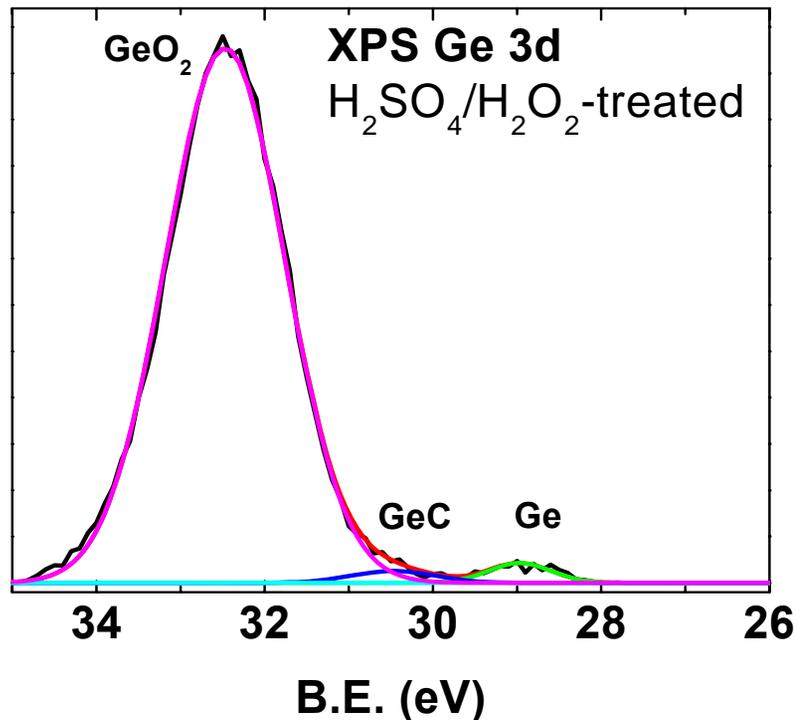
- De-ionized water; HF; DIW/H₂O₂
- HF/DIW/H₂O₂
- NH₄OH/H₂O₂
- HCl/H₂O₂
- H₂SO₄

Sulfur-passivation in hot (NH₄)₂S on H₂SO₄/H₂O₂-treated Ge

- (NH₄)₂S etches oxide
- Thin GeO_xS_y layer remains
- H₂SO₄/H₂O₂ and (NH₄)₂S treatment results in low C

- Starting surface has GeO, GeO₂, hydrocarbon, carbon....
- Some chemistries leave a thick oxide or sulfide.

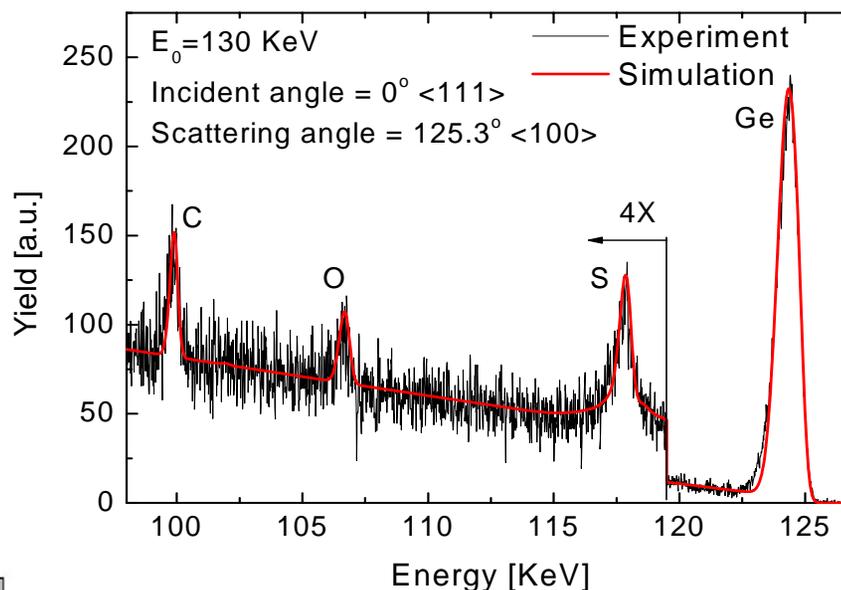
Ge cleaning / oxidation



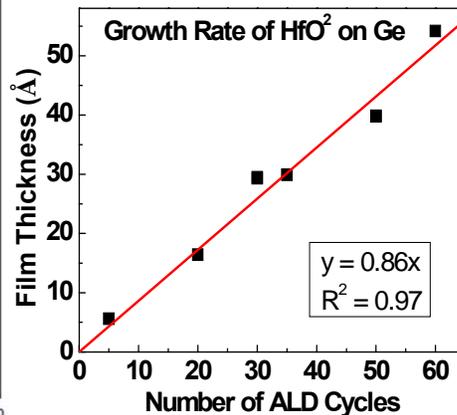
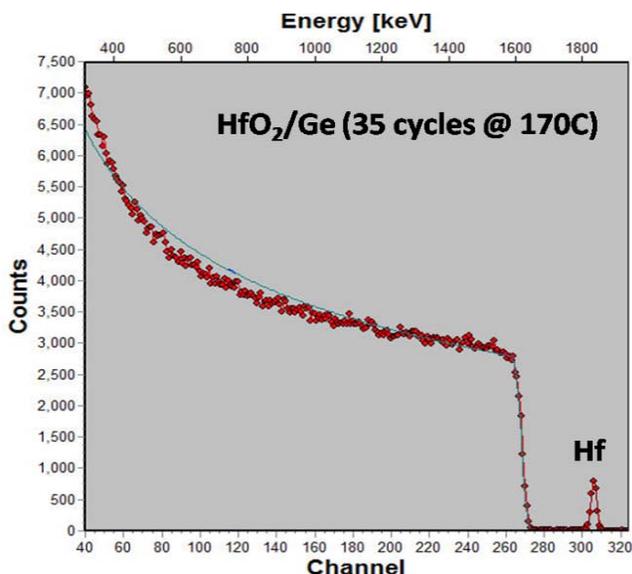
- XPS of Ge3d and C1s spectra of oxidized and S-passivated samples.
- No chemistry resulted in a C-free surface, but optimal ones lower the carbon and other impurities significantly.

Ion Scattering (MEIS and RBS)

MEIS for composition and depth profile of the S-passivated layer.



$\text{GeO}_{0.68}\text{S}_{0.32}$	7.5 Å
$\text{GeS}_{0.05}$	16 Å
Ge (111)	

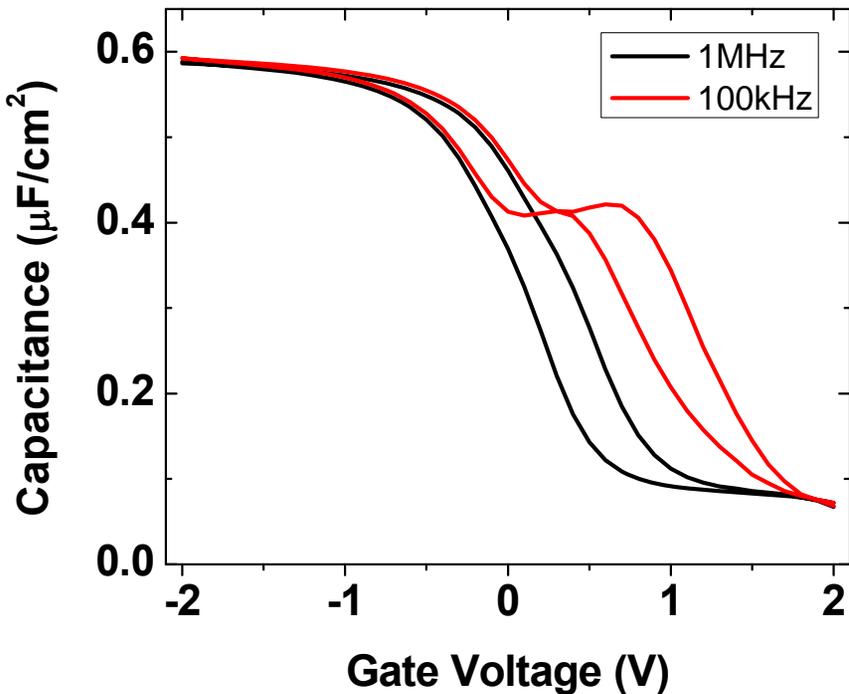


HfO₂ Growth conditions:

- Substrate temperature: $\sim 150^\circ\text{C}$
- Hf Precursor ($\text{Hf}(\text{N}(\text{CH}_3)(\text{C}_2\text{H}_5))_4$)
- Growth Rate: $\sim 0.86 \text{ \AA/cycle}$

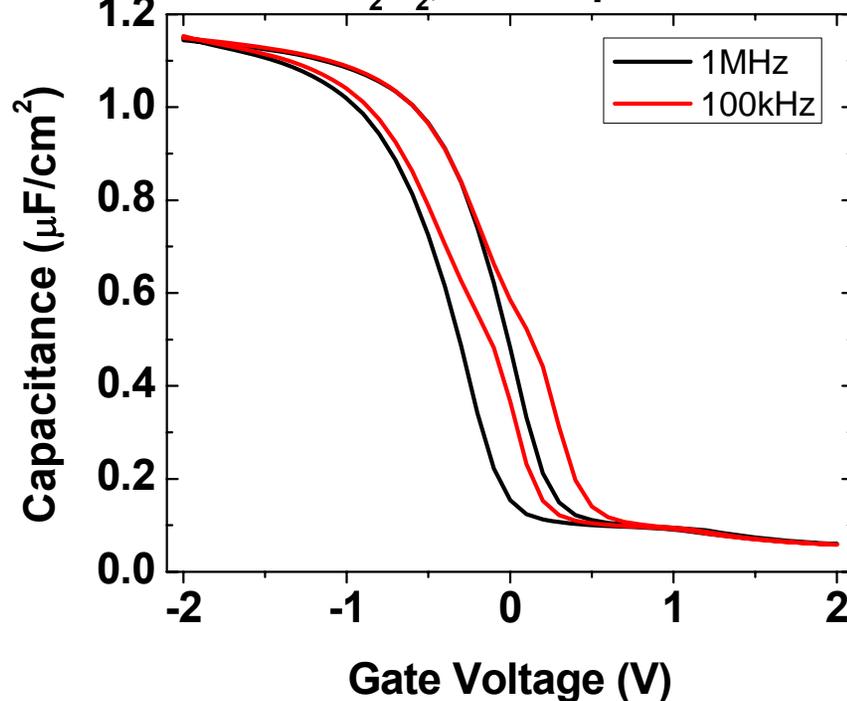
S-Passivation Improves the Interface

HF-last, without S-passivation



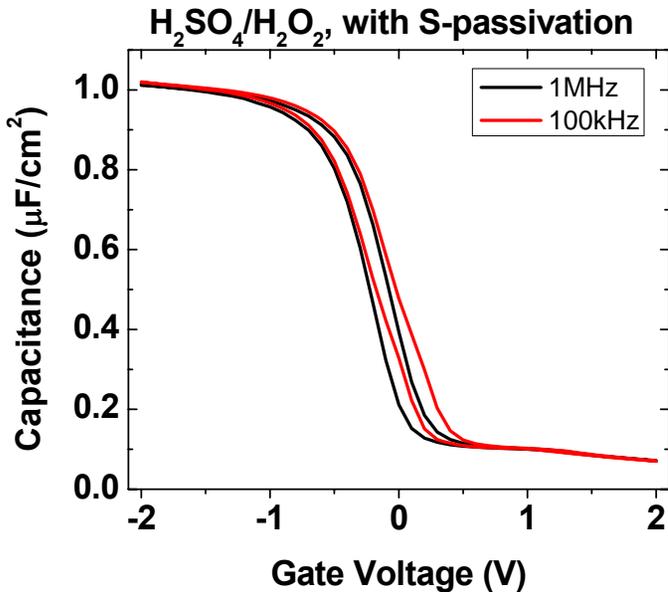
Q_i/e (cm ⁻²)	4.00×10^{13}
Q_{HS}/e (cm ⁻²)	1.15×10^{13}
ΔV_{FB_HS} (V)	0.31
D_{it} (eV ⁻¹ cm ⁻²)	3.80×10^{12}

HF/DIW/H₂O₂, with S-passivation

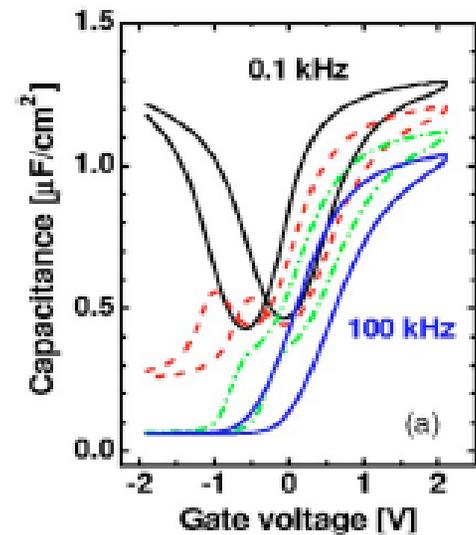
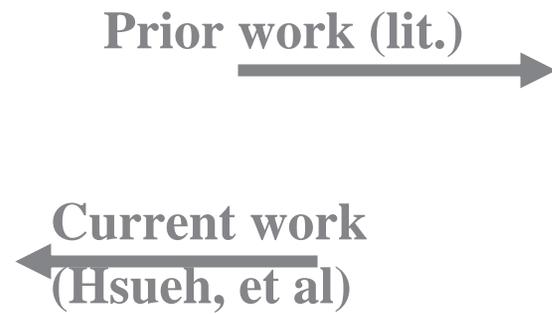


Q_i/e (cm ⁻²)	4.17×10^{12}
Q_{HS}/e (cm ⁻²)	2.09×10^{12}
ΔV_{FB_HS} (V)	0.29
D_{it} (eV ⁻¹ cm ⁻²)	1.66×10^{11}

Cleaning	HF	HF/DIW/H ₂ O ₂	H ₂ SO ₄ /H ₂ O ₂ HF	H ₂ SO ₄ /H ₂ O ₂
S-passivation	No	Yes	Yes	Yes
Q _i /e (cm ⁻²)	4.00x10 ¹³	4.17x10 ¹²	3.56x10 ¹²	3.19x10 ¹²
Q _{HS} /e (cm ⁻²)	1.15x10 ¹³	2.09x10 ¹²	1.5x10 ¹²	9.72x10 ¹¹
ΔV _{FB_HS} (V)	0.31	0.29	0.22	0.15
D _{it} (eV ⁻¹ cm ⁻²)	3.80x10 ¹²	1.66x10 ¹¹	8.91x10 ¹⁰	6.23x10 ¹⁰



HfO₂ 40Å, hysteresis is ~0.15V.
Ge surface was first H₂SO₄/H₂O₂ treated.
No HF used before sulfiding in (NH₄)₂S.



77Å HfO₂, hysteresis is ~0.5V.
10% HF etching for 10mins before sulfiding in (NH₄)₂S.
APL 89, 112905 (2006)

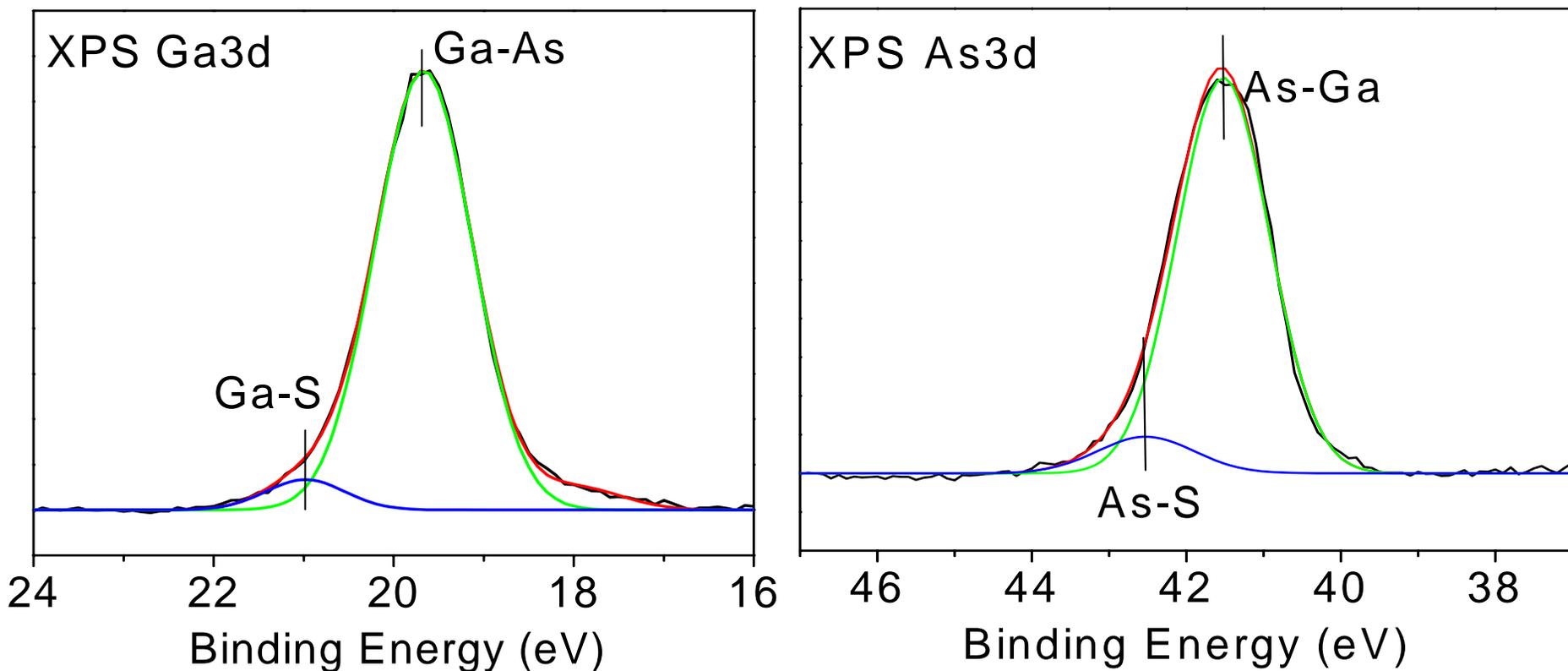
Summary Ge results

- Ge based high-k dielectric MOSCAPs have been grown and show very good electrical properties.
- MOSCAP properties are a strong function of surface cleaning and passivation. Wet chemistry is critical, and must be controlled with reproducible conditions (purity, temperature, concentration, pH, time etc.).
- Variations in surface treatment and ALD growth show up clearly in physical characterization (XPS, MEIS, etc.) and can be correlated with defects such as interface state density.

GaAs – based stacks

- How best to grow a high-K/metal electrode gate stack on GaAs-based channels with high quality interface?
- Can we use cleaning and passivation chemistries on GaAs that were found to produce optimal Ge/high-K gate stacks?
- Do ALD high-K growth chemistries and conditions that work on Si and Ge also work on III-V films?
- Do we need SiO_2 , nitride, Al_2O_3 or other interlayer materials and structures to minimize defect density and produce viable gate stacks?

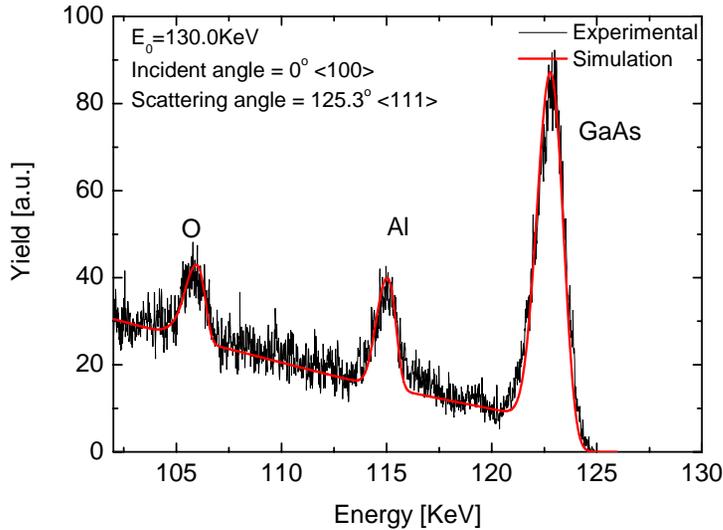
S Passivation of GaAs-based compounds



Using new wet chemical treatments, we can produce a film in which there is no native oxide on the GaAs surface and a relatively passive sulfide layer

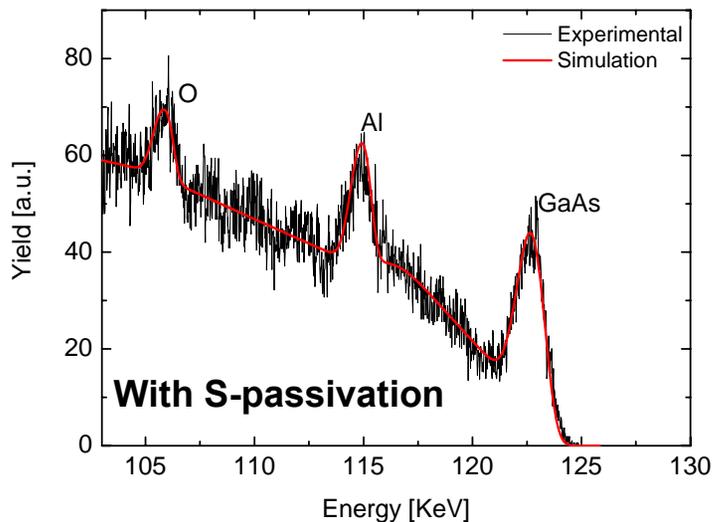
MEIS of ALD-grown Al₂O₃/GaAs

In-situ Al₂O₃/GaAs(001) without S-passivation



- One single uniform layer of Al_{1.7}O₃ (20Å, a little off-stoichiometry) on the surface fits the data well; the data indicate little roughness on this film.
- Native oxides on GaAs result in an interface GaAs peak larger than one on a passivated sample (see below).

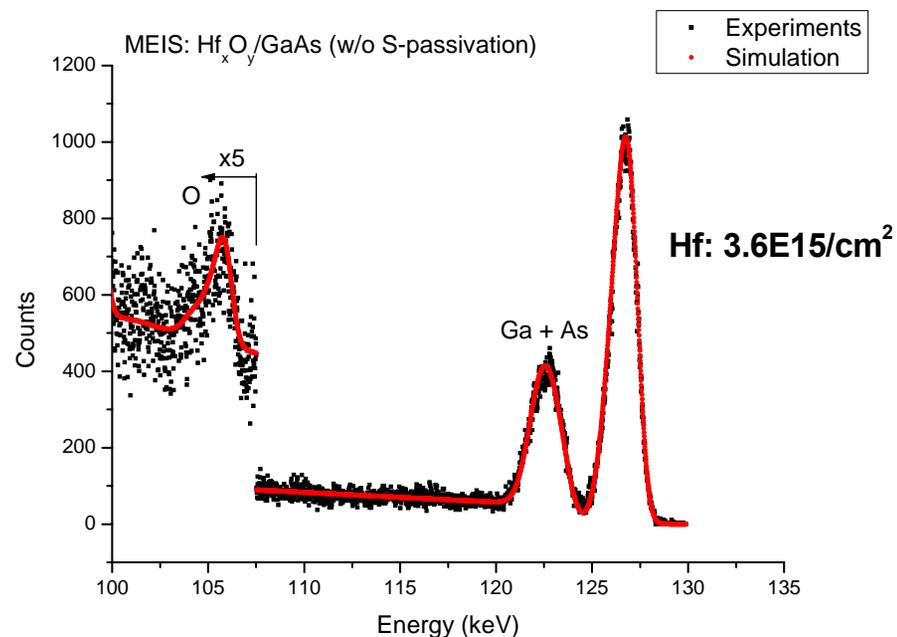
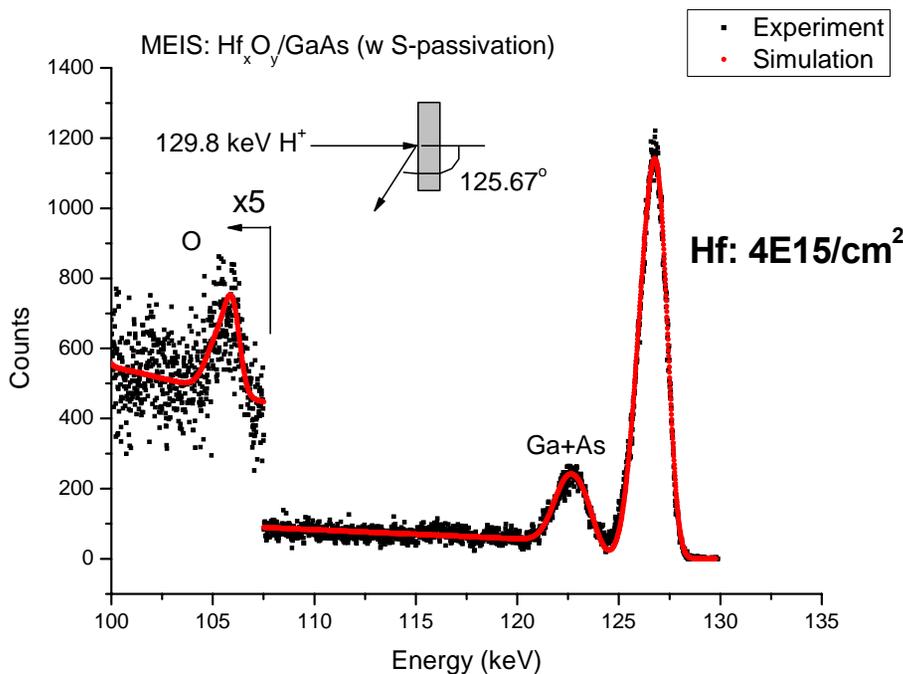
Element	Concentration $\times 10^{15}$ [atoms/cm ²]
Al	8.7
O (not including native oxide)	15.0



- One single uniform layer of Al₂O₃ (20Å, 20 cycles) on the surface fits the data well, indicating little roughness.
- High background due to poor
- No S observed.

Element	Concentration $\times 10^{15}$ [atoms/cm ²]
Al	9.4
O	14.2

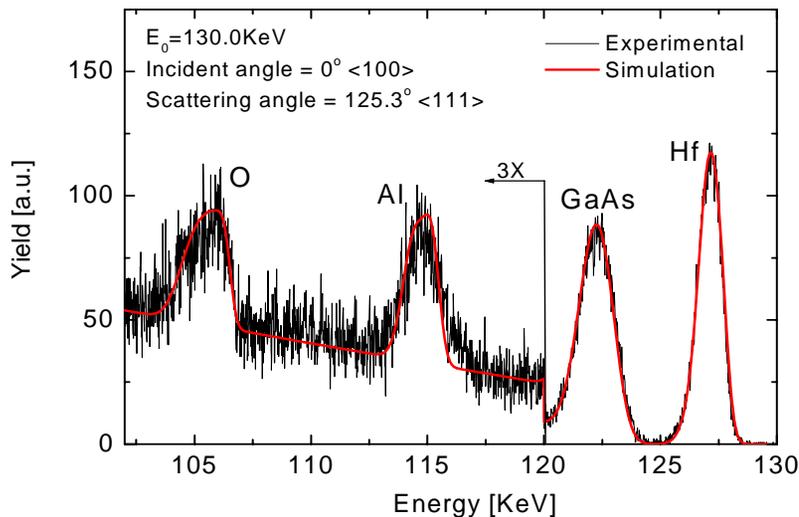
MEIS of ALD-grown HfO_2/GaAs



- No S remains on the S-passivated sample
- Film not perfectly flat (non-uniform initial nucleation).
- More oxide at the interface of HfO_2/GaAs w/o S-passivation

Multilayer $\text{HfO}_x/\text{Al}_2\text{O}_3/\text{GaAs}$ gate stack MEIS

without sulfur passivation

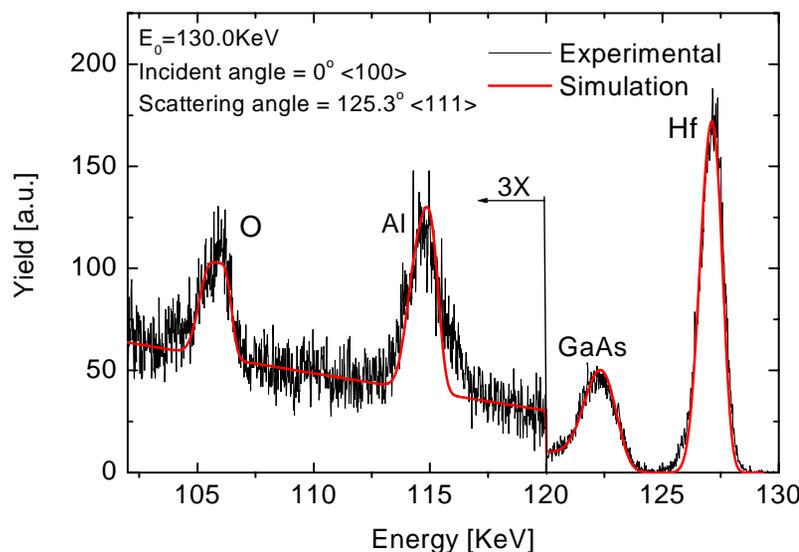


- $\text{HfO}_x \sim 20\text{\AA}$ (20cycles), $\text{Al}_2\text{O}_3 \sim 15\text{\AA}$ (15cycles), interface $\text{GaAsO}_x \sim 30\text{\AA}$.

- The HfO_x layer appears somewhat rough: Al has to be included in HfO_x layer to fit both Hf and Al peaks with a uniform-layer model.

Element	Concentration $\times 10^{15}$ [atoms/cm ²]
Hf	1.74
Al	10.54
O (not including native oxide)	20.67

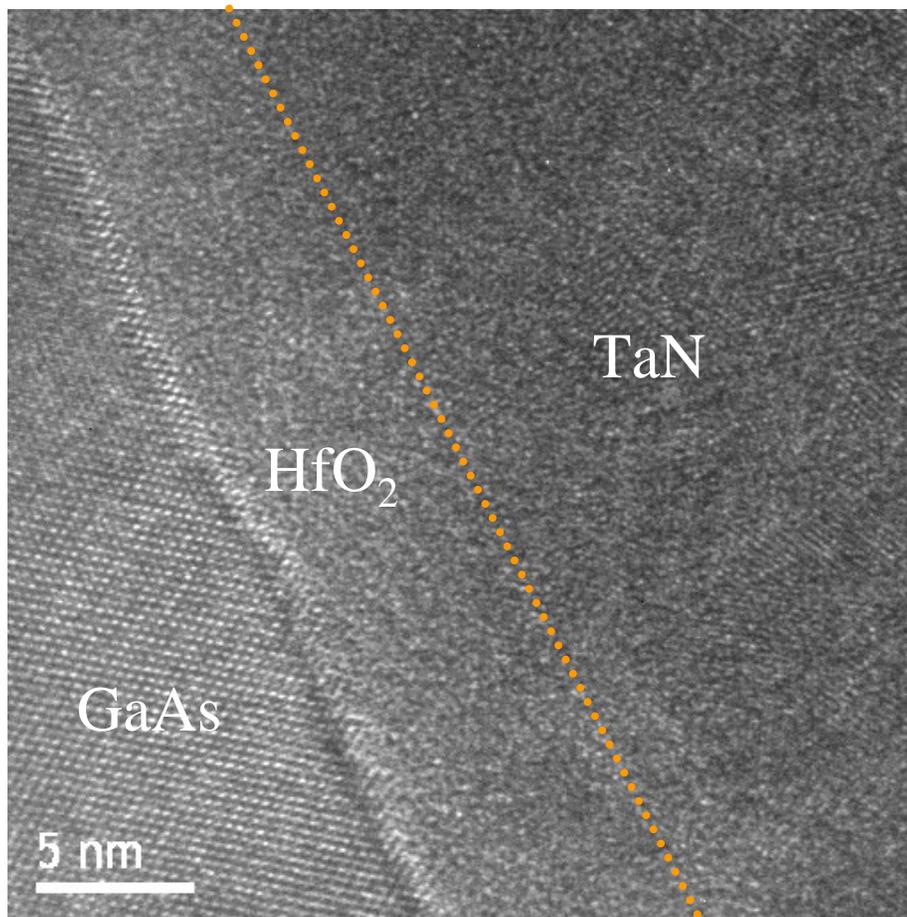
with sulfur passivation



- Similar rough structure as non-passivated sample.
- No S observed in this passivated sample.
- Reduced height of GaAs peak might be due to the removal of native GaAs oxide during etching, resulting in better crystallinity of GaAs.

Element	Concentration $\times 10^{15}$ [atoms/cm ²]
Hf	1.8
Al	10.44
O	16.14

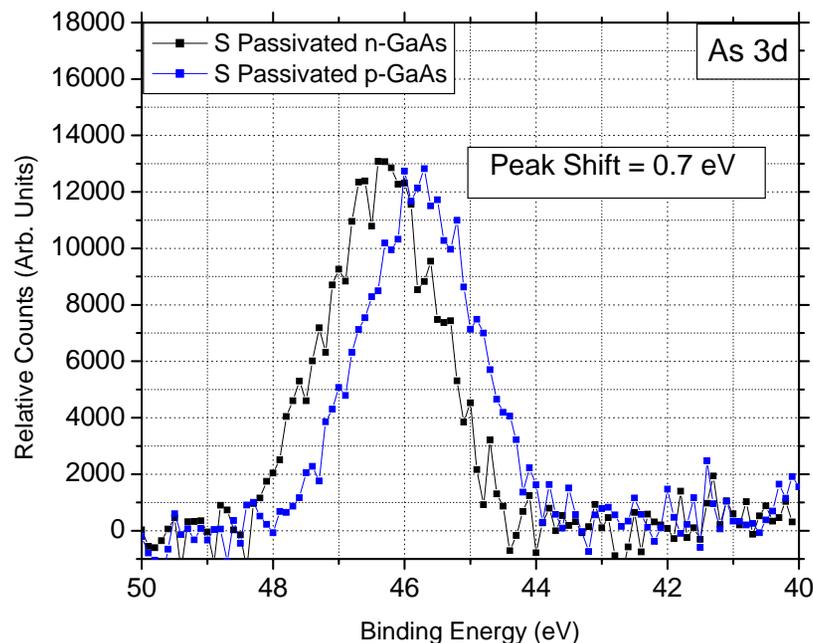
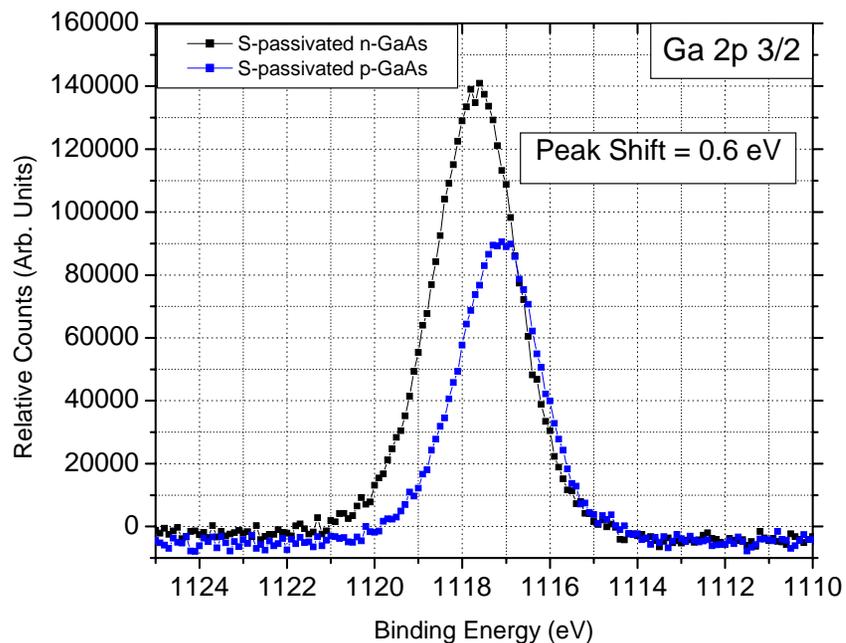
TEM for GaAs/HfO₂/TaN Gate Stack



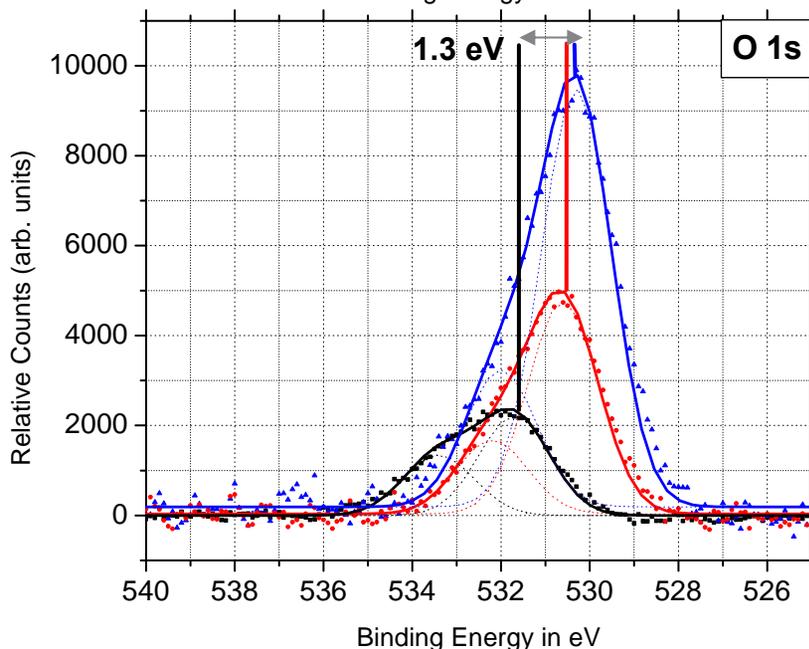
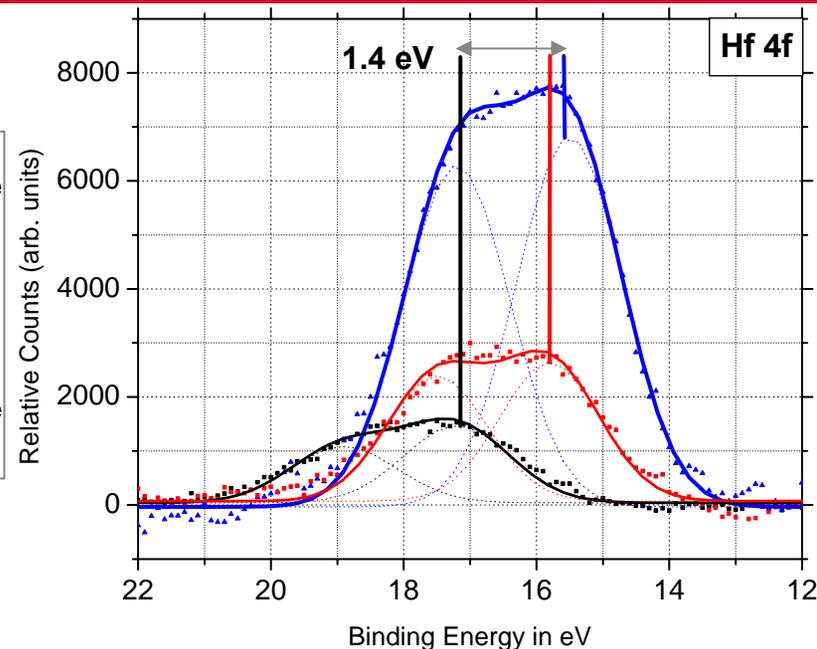
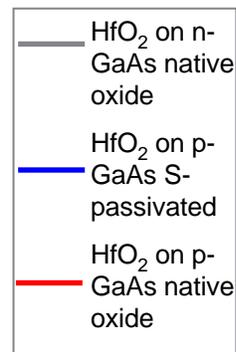
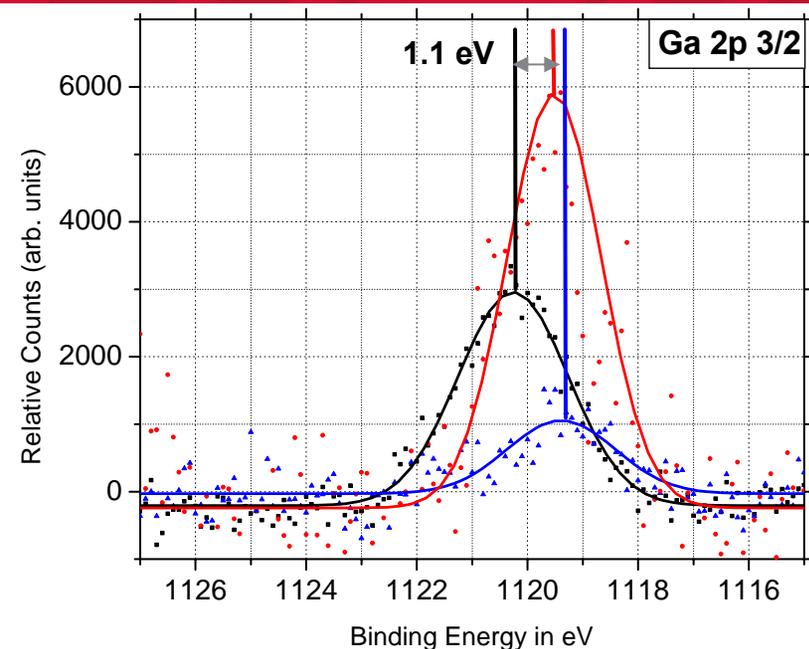
A TEM image of a GaAs sample with following process: native oxide etched, sulfur passivated, HfO₂ grown by ALD, TaN metal grown by PVD.

From TEM images (and microscopic elemental analysis, AFM, etc.), we find that the interface roughens after this specific chemical oxidation and passivation

GaAs with S-passivation XPS band alignment (highly doped n and p-type)

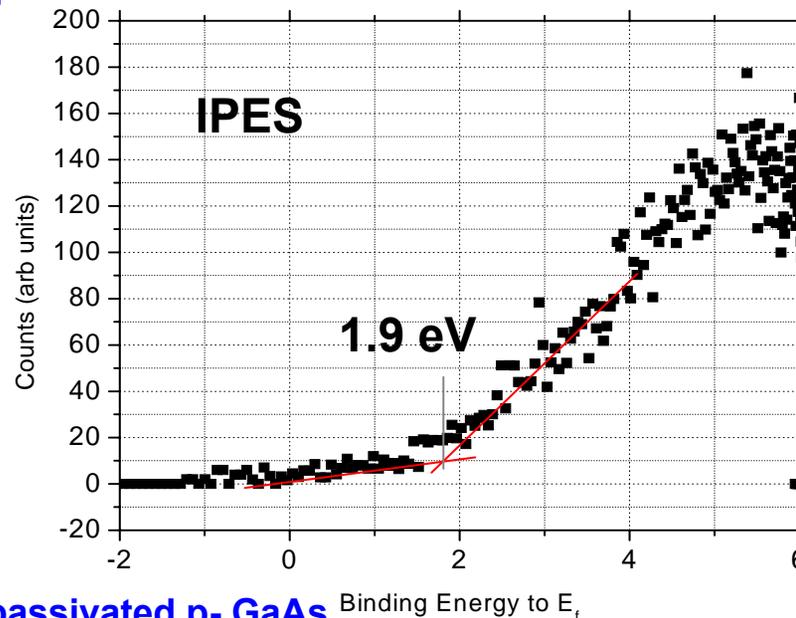
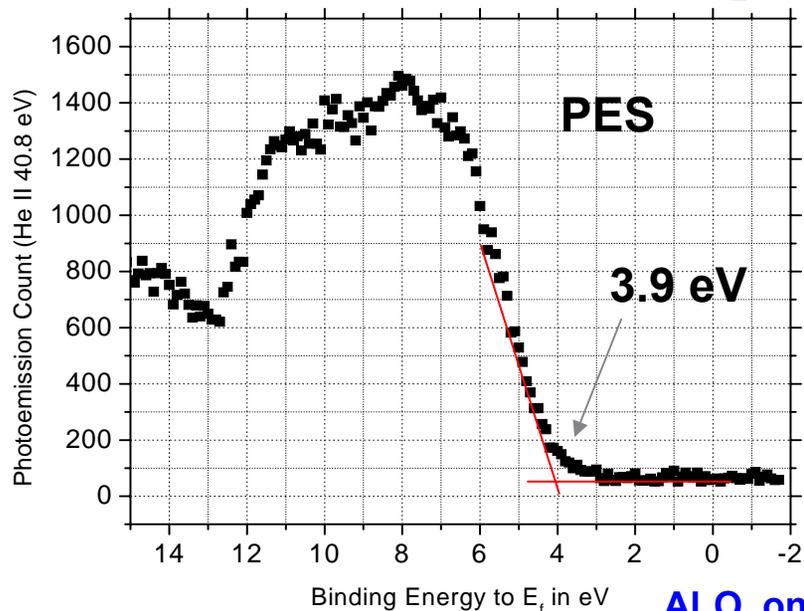


- **Partial pinning of the Fermi level at S-passivated surface**
- **Results imply a $\sim 0.4 \pm 0.05$ eV upward band bending for n-GaAs, $\sim 0.4 \pm 0.05$ eV downward band bending for p-GaAs**

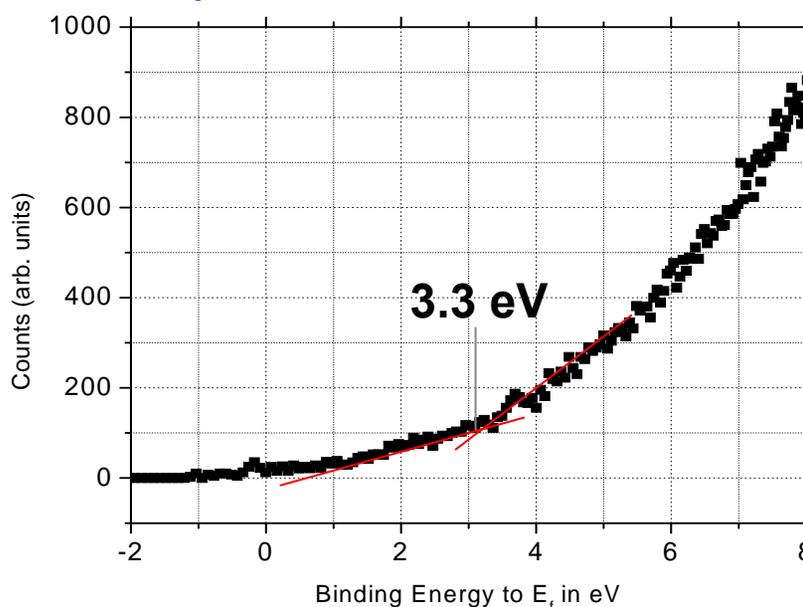
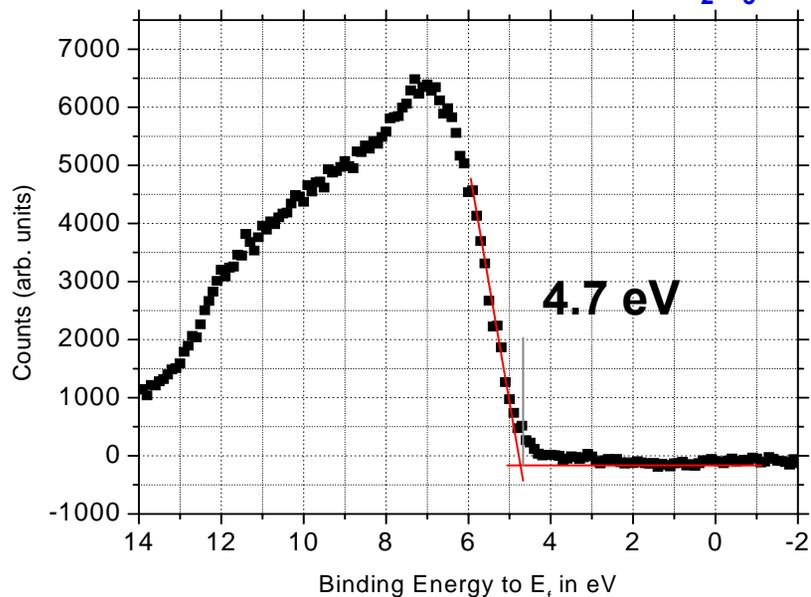


- Little difference in interface chemistry between HfO₂ on S-passivated and HfO₂ on native oxide sample.
- Ga 2p is single Gaussian (consistent with GaAs), no GaO_x or AsO_x in O 1s signal
- Shift between n-type and p-type samples ~1.2-1.4 eV means *the Fermi level is not strongly pinned.*
- Results imply that the interfacial O and S are likely removed during high-K growth.

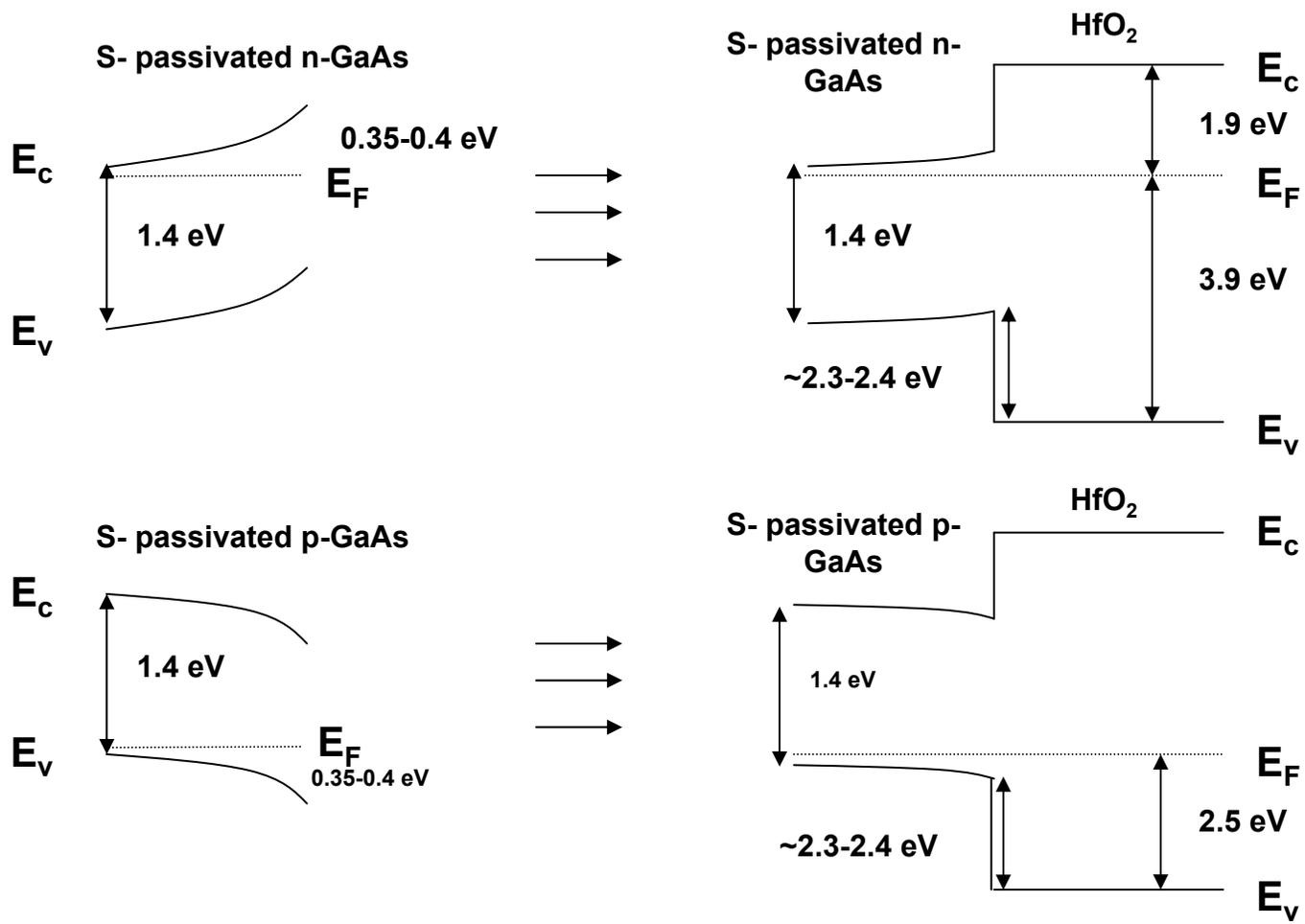
HfO₂ on S-passivated n- GaAs



Al₂O₃ on S-passivated p- GaAs



- S-passivated film Fermi levels partially pinned.
- After HfO₂ growth, little pinning.
- Conduction and valance band offsets agree with literature.

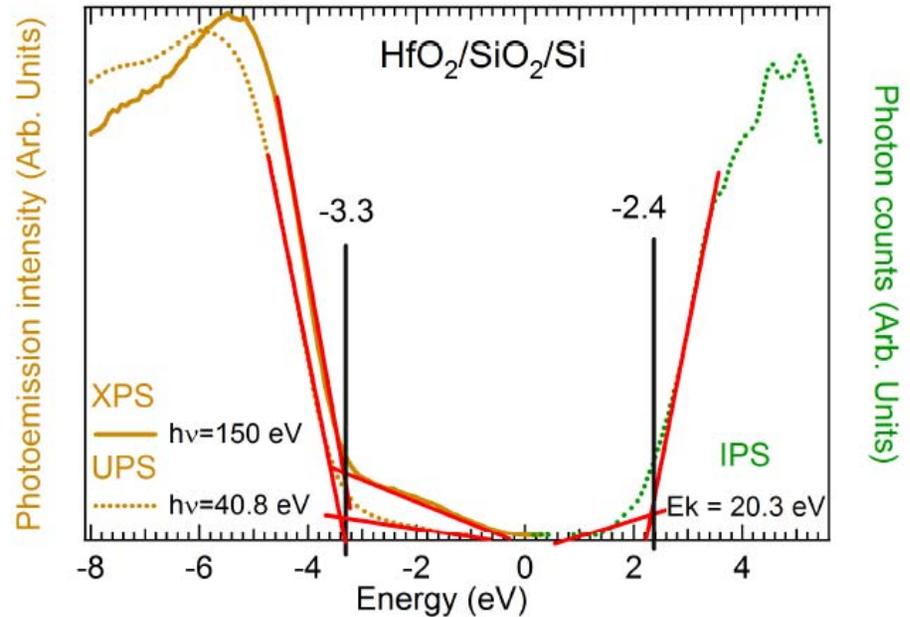


Summary GaAs results

- **Electronic structure of various films and interface passivation routes examined. The removal of the native oxide and passivation of GaAs surface is effective.**
- **Appropriate band alignment and little Fermi level pinning found for some passivation and film growth conditions.**
- **Exploring new routes to decrease roughening during the wet chemistry**
- **Device measurement in progress**

Band Edge Determination

Single chamber
 UHV measurements



Calculated bulk Fermi level
 Experimental Fermi level



Band bending

Substrate band edges determination



Band offsets

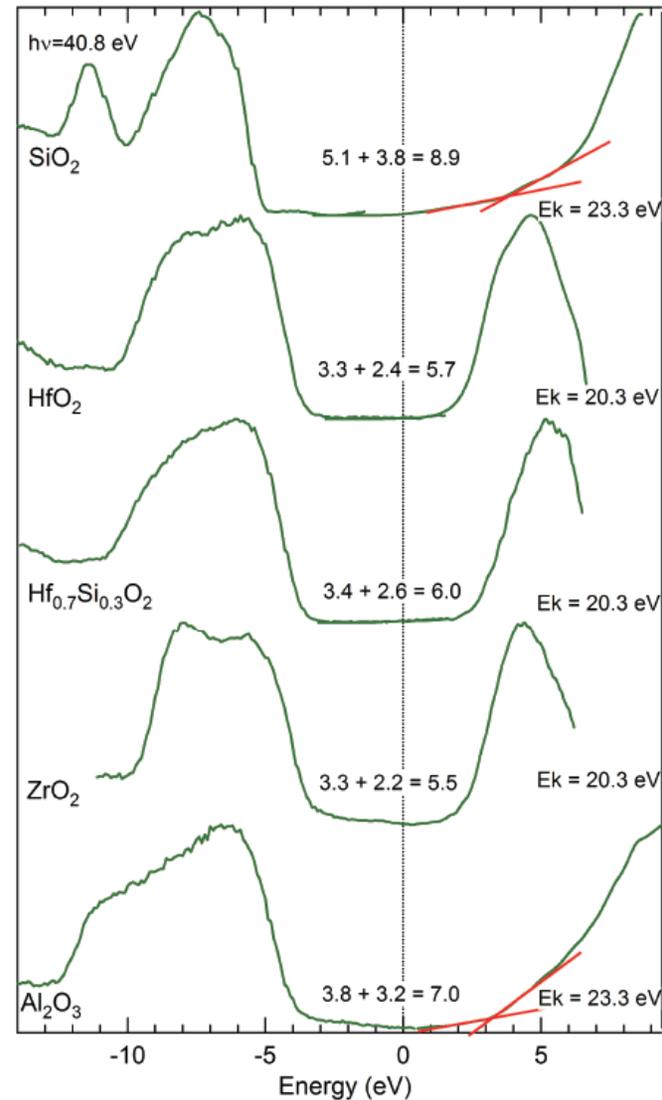
Gap determination

Band Gap Measurements

Single chamber measurements

Spectra shifted to set at zero
 The silicon midgap

Gaps and band offsets
 comparable to literature



Comparison To Literature

Method	Gap	VBO	CBO
XPS, energy loss ⁸	6.95	3.75	2.08
XPS, energy loss ¹⁵	6.52	3.03	2.37
XPS, energy loss ²⁶	6.7	2.9	2.7
IntPE ¹²	6.2	2.95	2.15
SE ²⁷	6.26	—	—
BEEM ²⁸	—	—	2.8
This work	7.0	3.2	2.7



Method	Gap	VBO	CBO
XPS, energy loss ²⁵	5.65	3.65	0.88
XPS, energy loss ⁸	5.50	3.35	1.03
XPS, energy loss ²⁶	5.6	2.5	2.0
XPS, UPS ¹¹	5.7	3.4	1.2
XPS, IPS ²³	5.68	3.40	1.16
IntPE ¹²	5.4	2.3	2.0
EELS ²¹	5.0	—	—
This work	5.5	2.8	1.6



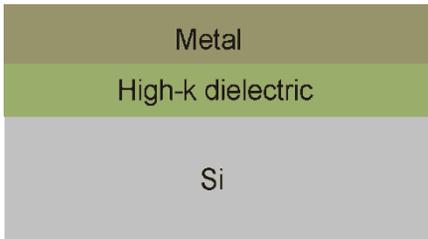
Method	Gap	VBO	CBO
XPS, energy loss ¹⁴	5.7	3.10	1.48
XPS, energy loss ¹⁵	5.25	2.22	1.91
XPS, IPS ¹⁶	5.86	3.28	1.46
XAS, XPS ¹⁷	5.1	3.0	1.0
UPS ¹⁸	—	2.75	—
IntPE ¹⁹	5.6	2.5	2.0
XAS ²⁰	6.0	—	≥1.2
EELS ²¹	5.8	—	—
SE ²²	5.8	—	—
This work	5.7	2.7	1.9



Method	Gap	VBO	CBO
XPS, energy loss ⁸	8.95	4.49	3.34
XPS, UPS ¹¹	9.0	4.4	3.5
IntPE ¹²	—	—	3.15
XPS ¹⁰	—	4.35	—
XPS ⁷	8.95	4.54	3.28
This work	8.9	4.5	3.3



Band Alignment Models

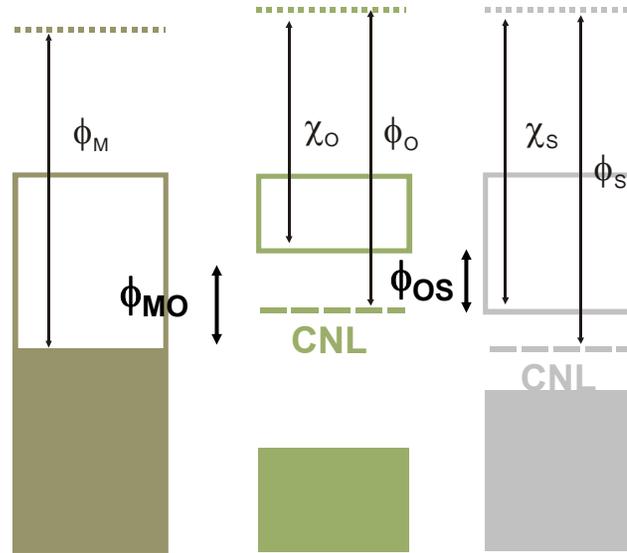


Schottky limit

$$S = 1$$

→ No pinning

Induced Gap State Model



Bardeen limit

$$S = 0$$

→ Strong pinning

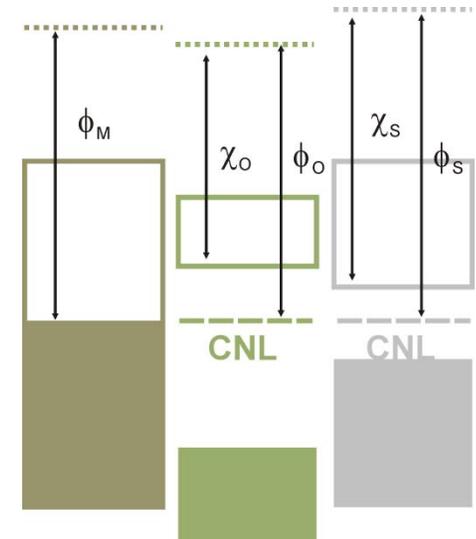
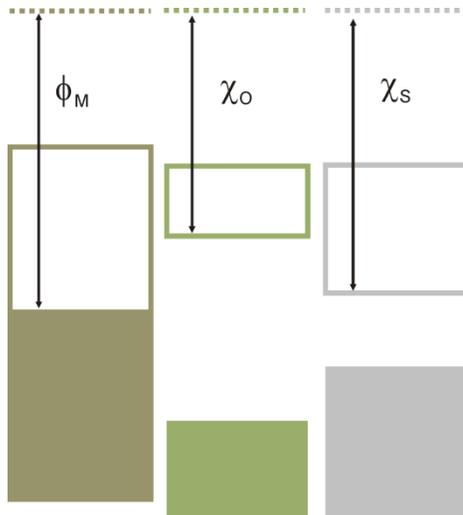
$$\phi_{MO} = S (\phi_M - \phi_o) + (\phi_o - \chi_o)$$

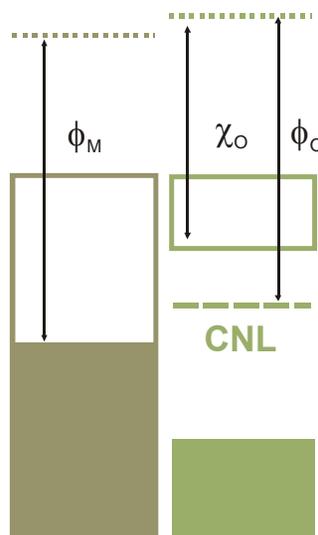
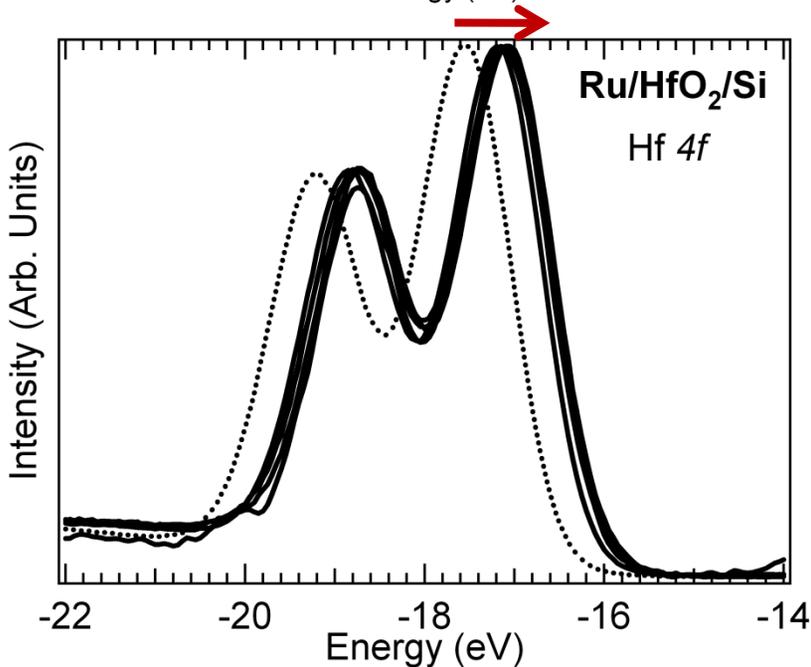
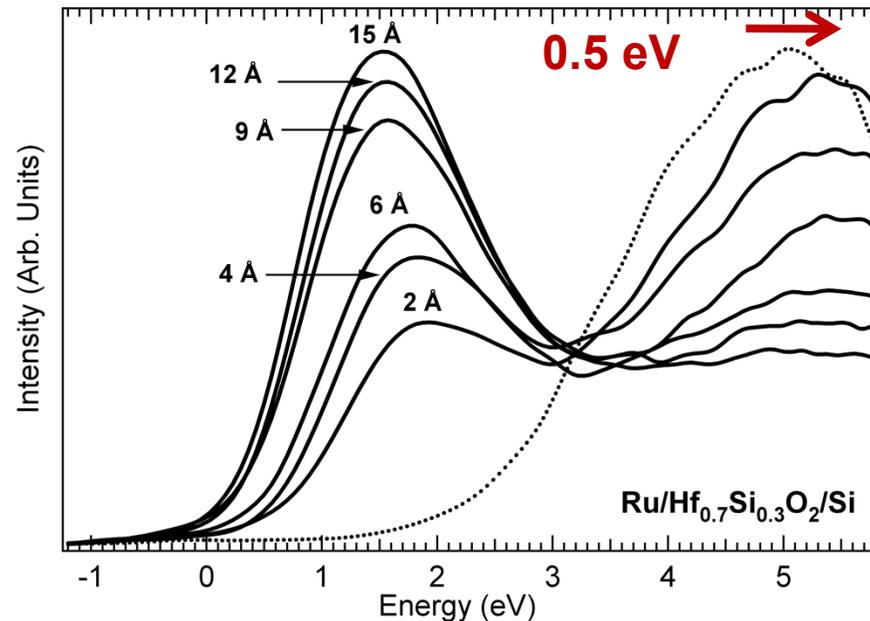
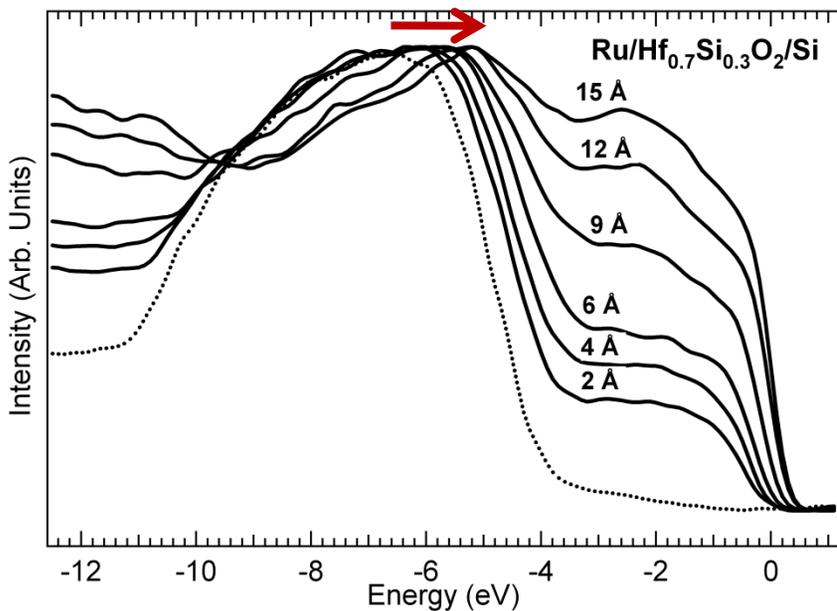
$$\phi_{os} = (\chi_o - \phi_o) - (\chi_s - \phi_s) + S (\phi_o - \phi_s)$$

S = pinning parameter

Reality is in between

Alignment of the CNL modified by S





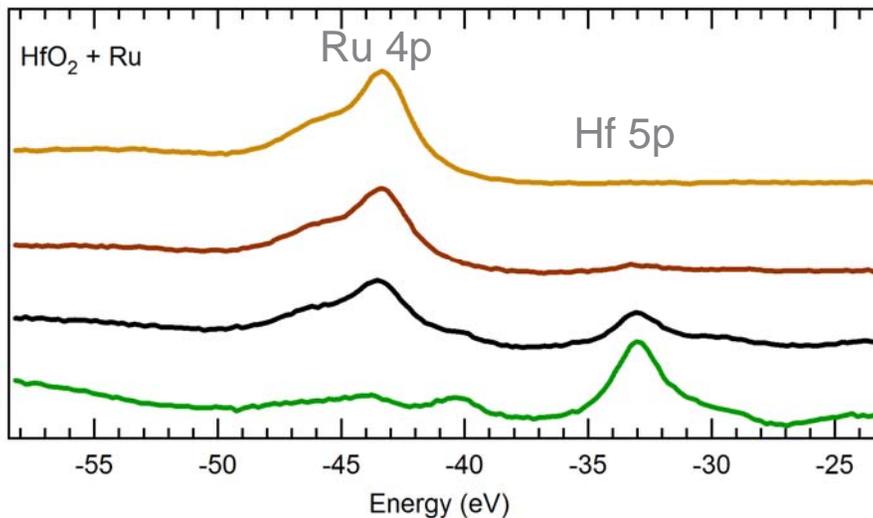
$$\phi_{MO} = S (\phi_M - \phi_O) + (\phi_O - \chi_O)$$

S=0.53 CNL=3.7

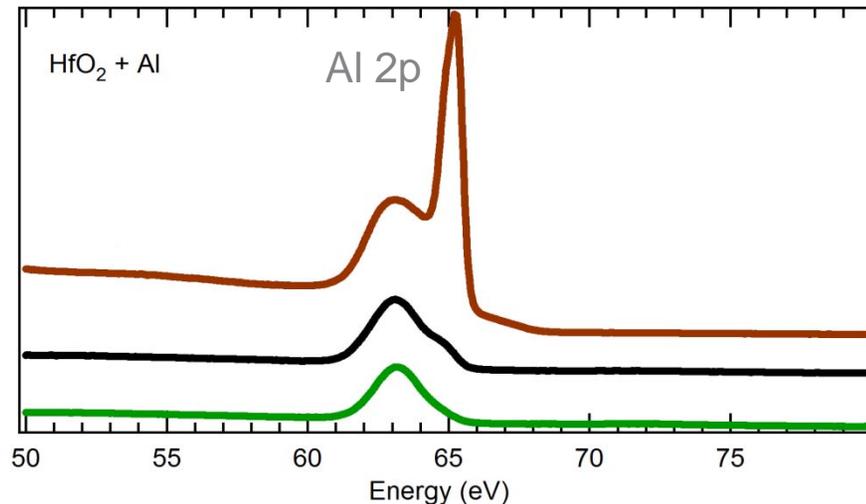
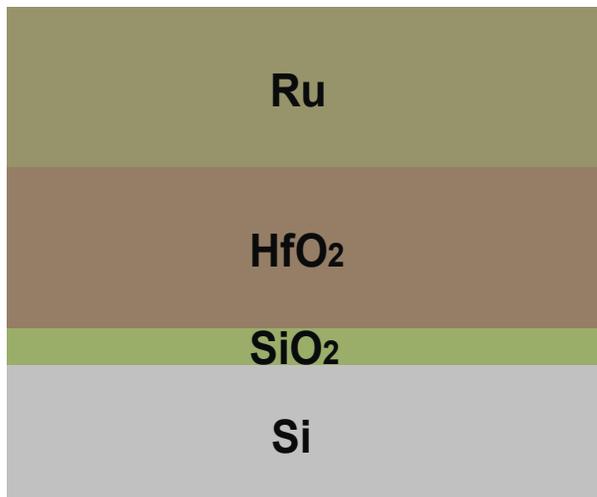
Robertson, JVSTB, 18, 1785, 2000

Theoretical shift: 0.4 eV

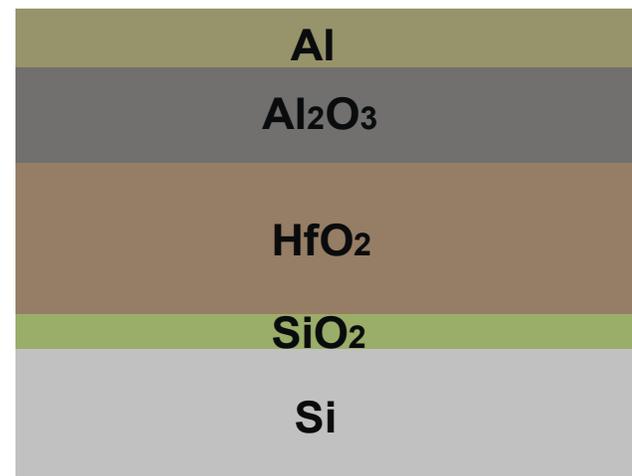
Metal Interaction with the Substrate



No oxidation of ruthenium



**Oxidation of aluminium
 Formation of a Al₂O₃ layer**



Summary

Ge and GaAs based high-k dielectric MOSCAPs have been grown. Electronic and chemical structure of various films and interface passivation routes examined.

Ge MOSCAPs show good electrical properties. Electrical properties are a strong function of surface cleaning and passivation. Wet chemistry is critical, and must be controlled with reproducible conditions (purity, temperature, concentration, pH, time etc.).

Variations in surface treatments also show up clearly in physical characterization (XPS, MEIS, etc.) of both Ge and GaAs, and can be correlated with defects such as interface state density.

Favorable band alignment found for some passivation and film growth conditions. Fermi level pinning (of interface defects?) appears not to be critical if film grown properly.

Plans

- **Pursue high-K/metal gate integration on III-V's and Ge.**
 - Correlate defect generation rate with E_{gap} and e-h pair generation probability of semiconductor and metal layers adjoining dielectric
 - Correlate physical and electrical measurements of “intrinsic” and “radiation induced/enhanced” defects
 - Thermal and chemical stability of passivation layers on III-V surfaces and relation to defect conc: Si, S, N, Al, etc.
 - Explore E_f pinning and relation to interface composition in Ge and III-V's
 - Monitor H/D concentration/profiles in post-silicon materials and radiation induced changes in them
- **Explore radiation induced defects in organic, nanowire, MEMS other novel devices.**

Recent MURI-related publications:

- L.V. Goncharova, et al; *Metal-gate-induced reduction of the interfacial layer in Hf oxide gate stacks*, J. Vac. Sci. Tech. A **25**, 261 (2007).
- N. Goel, et al; *Band offsets between amorphous LaAlO₃ and InGaAs*, Appl. Phys. Lett. **91**, 113515 (2007).
- M. Dalponte, et al. *MEIS study of antimony implantation in SIMOX and vacancy-rich Si*, J. Phys. D: Appl. Phys. **40**, 4222, (2007).
- S. Rangan, et al, *GeO_x interface layer reduction upon Al-gate deposition on a HfO₂/GeO_x/Ge stack*, Appl. Phys. Lett. **92**, 172 (2008).
- E. Garfunkel, G. Bersuker and J. Gavartin, *Defects in CMOS Gate Dielectrics*, to be published (2008).

These and other papers can be downloaded at:

<http://rutchem.rutgers.edu/faculty/garf/publications.html>