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Single-Event Transient Measurements in Advanced Technologies

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MURI Review

May 25, 2010

Outline

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- Introduction
  - Single-Event Mechanisms
  - Digital Single-Event Transients (SETs)
- SET Measurements in Bulk Technologies
  - Pulse Broadening
- Temperature Characterization of SETs
  - Experimental Measurements
  - Discussion of Mechanisms
- Conclusions

Ph.D. Research Contributions

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- **Performed an examination of SETs in bulk 130-nm and 90-nm CMOS technologies**
  - Gadlage et al. TNS 2007, Narasimham et al. TNS 2007, ***Narasimham et al. TNS 2008[1]***, Gadlage et al. EDL 2008, Gadlage et al. JRERE 2008, Narasimham et al. TDMR 2009, ***Ahlbin et al. TNS 2009[2]***, Narasimham et al. TSM 2009
- **Determined SET pulse-widths in a unique 180-nm FDSOI process via experimental measurements and TCAD simulations**
  - Gouker et al. TNS 2008, Gadlage et al. TNS 2009, Gouker et al. TNS 2009
- **Compared SET vulnerability in bulk and SOI technologies**
  - Gadlage et al. TNS 2009
- **Explored the effect of temperature on SET widths**
  - ***Gadlage et al. TNS 2009[3]***, Gadlage et al. TDMR 2009, Ramachandran et al. ISDRS 2009, Gadlage et al. presented at IRPS 2010
- **Developed and tested new SET structures in a 65-nm bulk technology**
  - Gadlage et al. submitted to 2010 RADECS, Gadlage et al., Ahlbin et al., and Jagannathan et al. accepted to NSREC 2010

Over two dozen authored/co-authored publications in the last three years.

[1]Best paper at the 2007 RADECS
[2]Nominated for best paper at the 2009 NSREC
[3]Best paper by a Vanderbilt Engineering Student in 2009

Single-Event Mechanisms

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- As feature sizes and transistor spacing have shrunk, single event mechanisms have become more complex.
- A single ion strike can modulate the electric potential in an entire well region.
- Multiple devices can be affected by an ion strike.

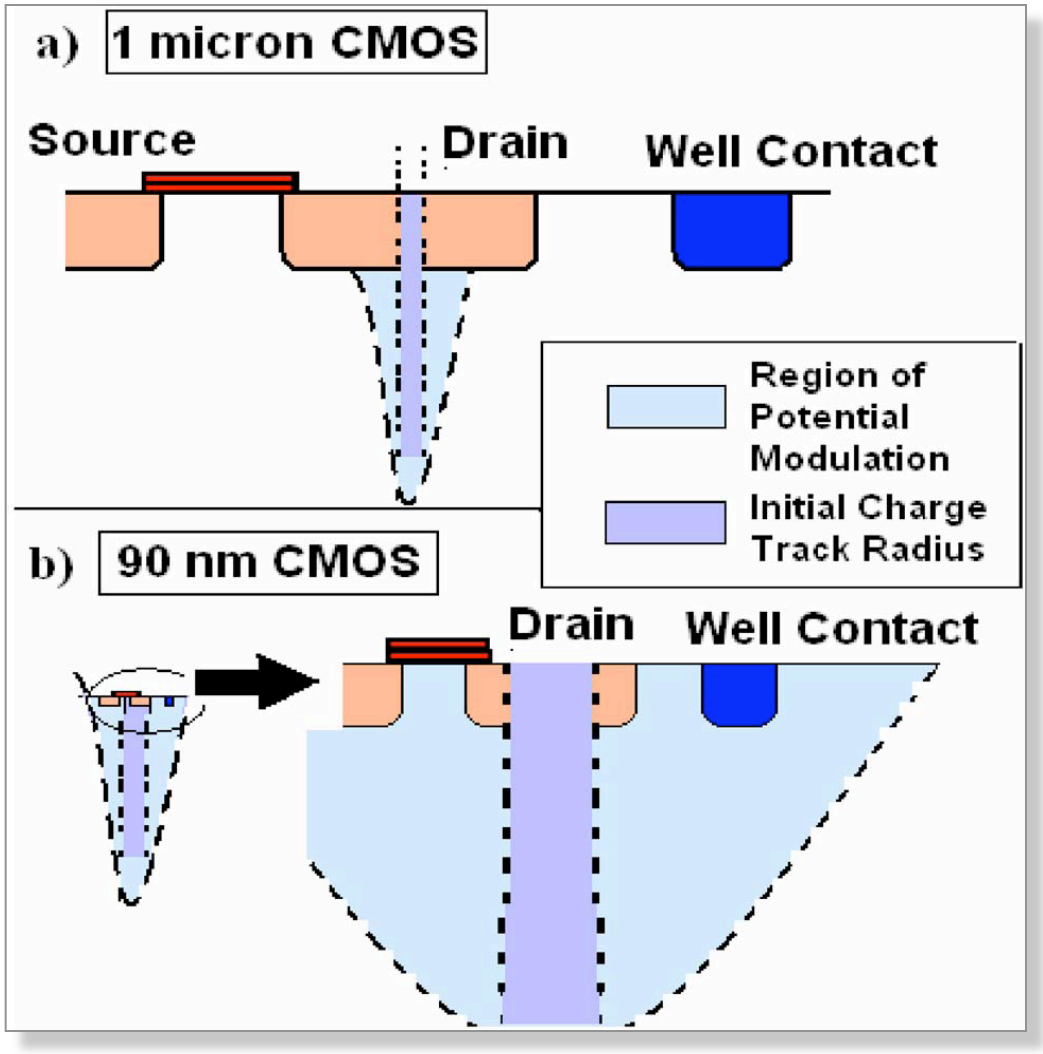

Image from DasGupta et al., *TNS 2007*

What is a Single-Event Transient?

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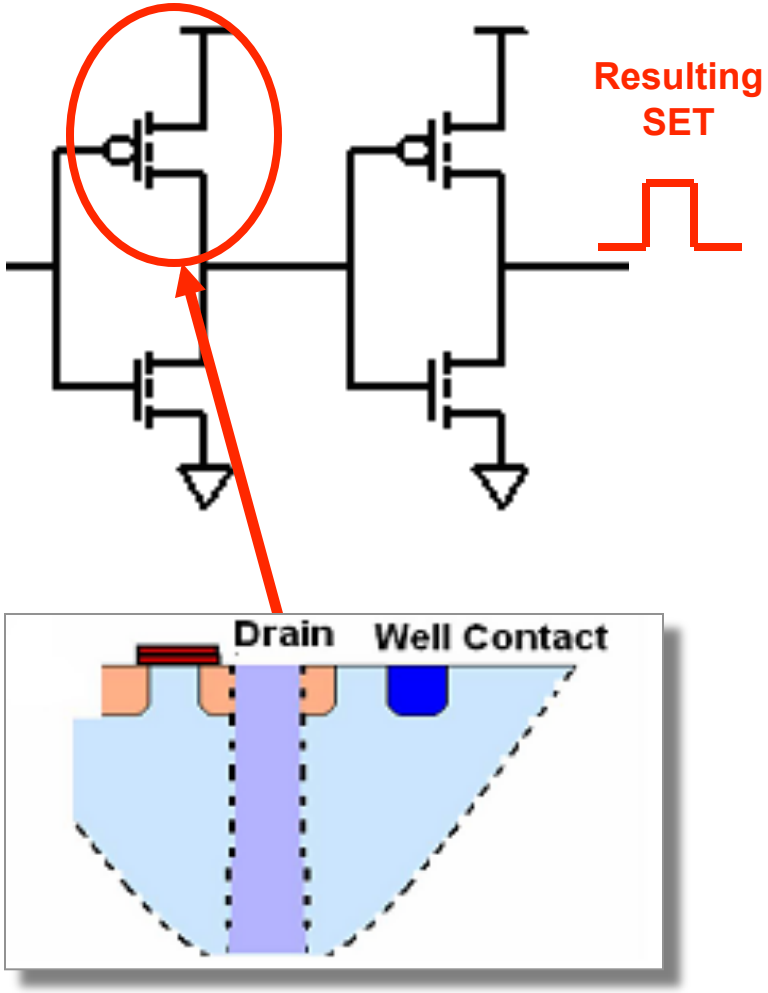


Energetic Particle Strike

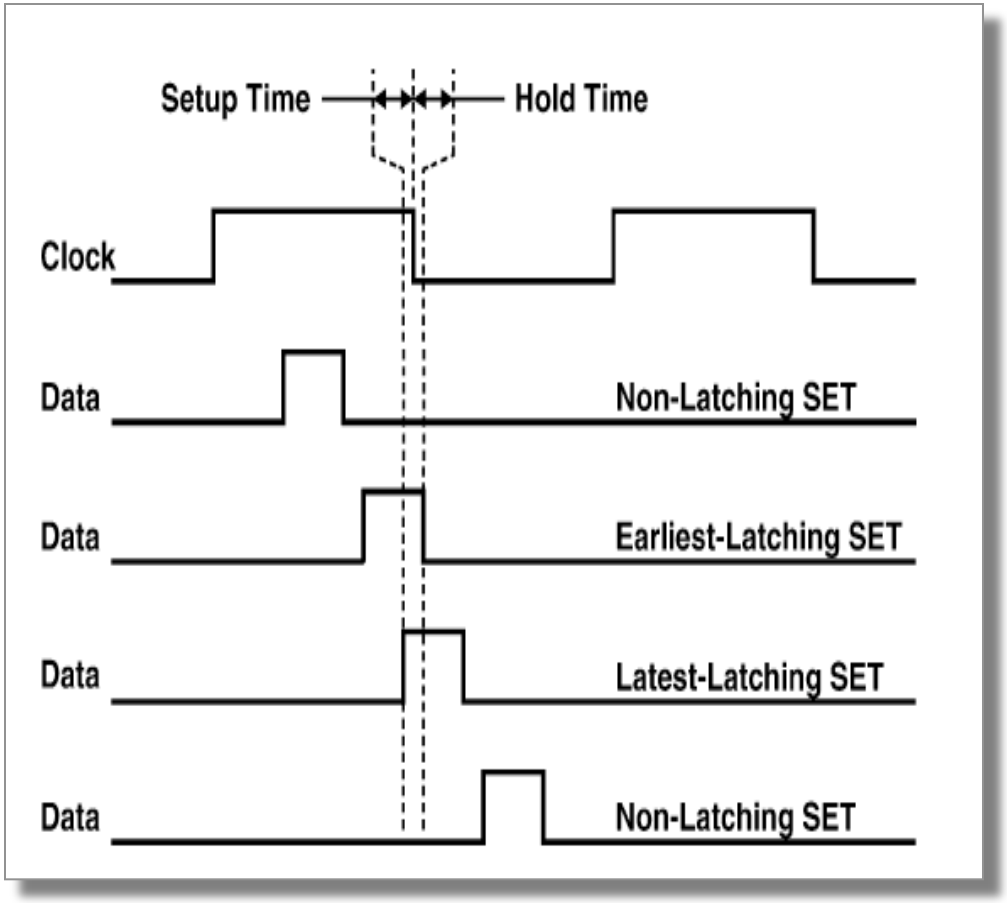
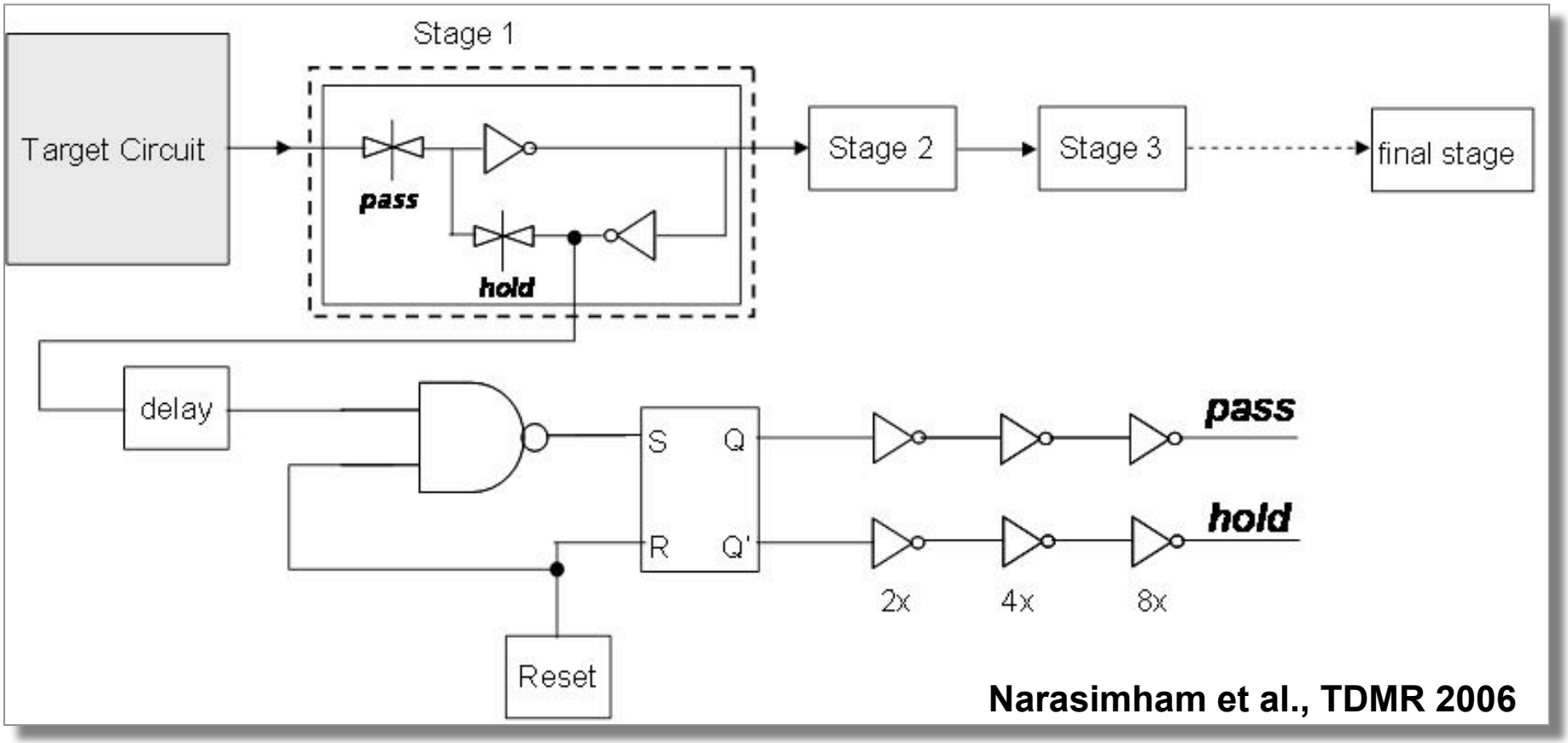


Illustration Detailing the Significance of SET Pulse Widths

Image from Mavis et al. 2002. However, the idea behind the image was discussed in Reed et al. 1996 and Massengill et al. 2000

SET Measurement Technique



- Circuit measures SET pulse width in units of stage delay
  - Delay changes with technology and temperature
- Target circuit can consist of almost any combinational logic chain
- Structure has been successfully implemented and tested in 130-nm bulk, 90-nm bulk, 65-nm bulk, 180-nm FDSOI, and 150-nm FDSOI

Previous SET Measurements in Bulk CMOS

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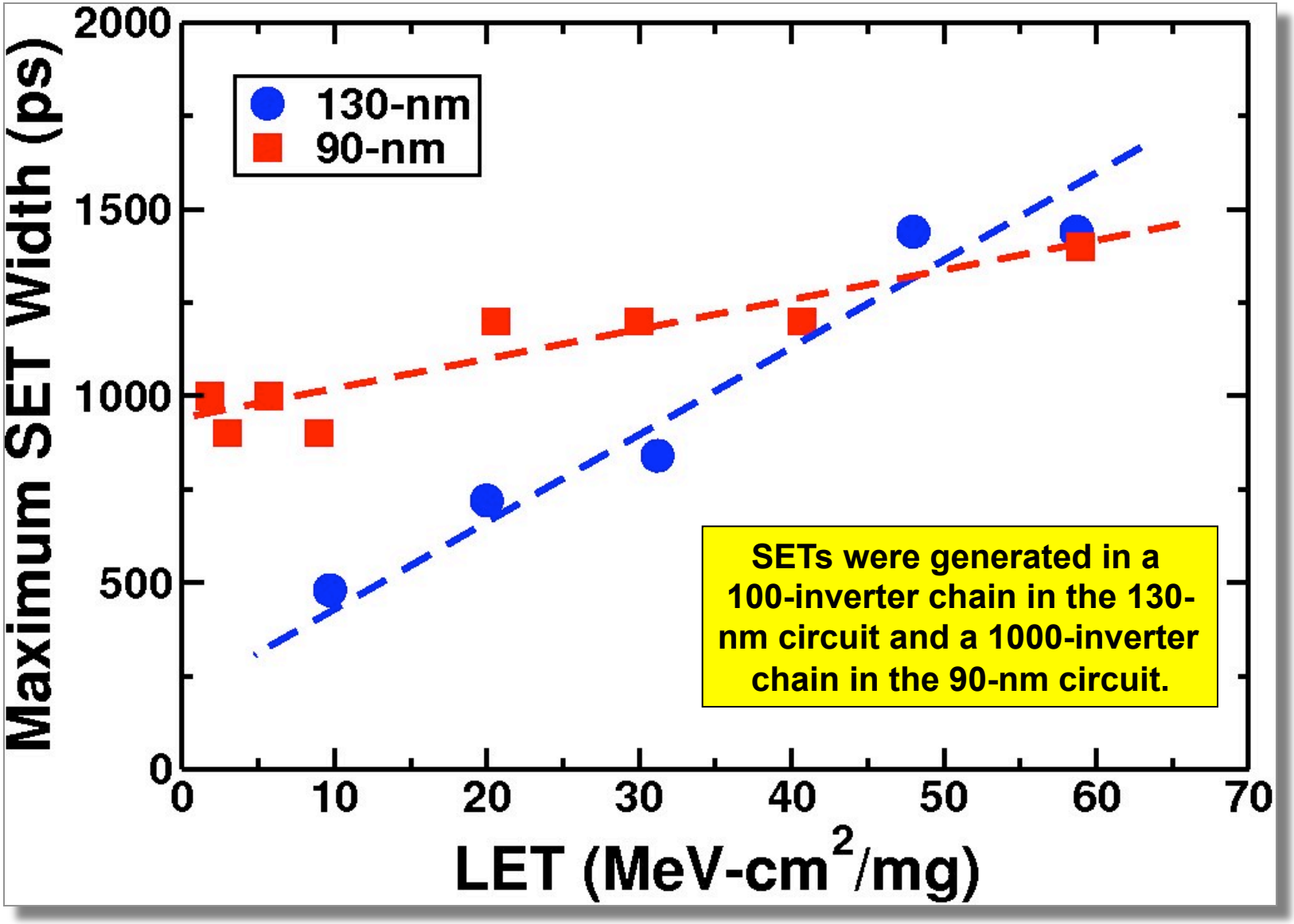

90-nm Pulse Broadening Experiment

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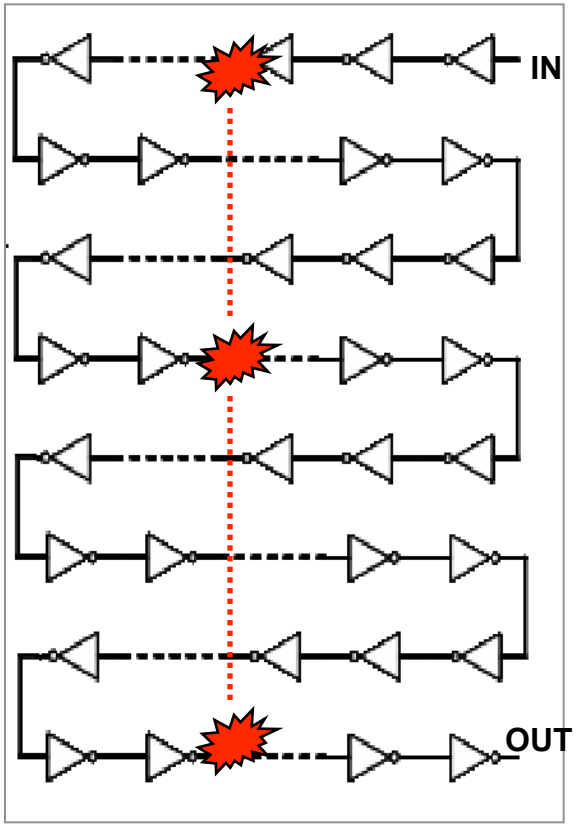
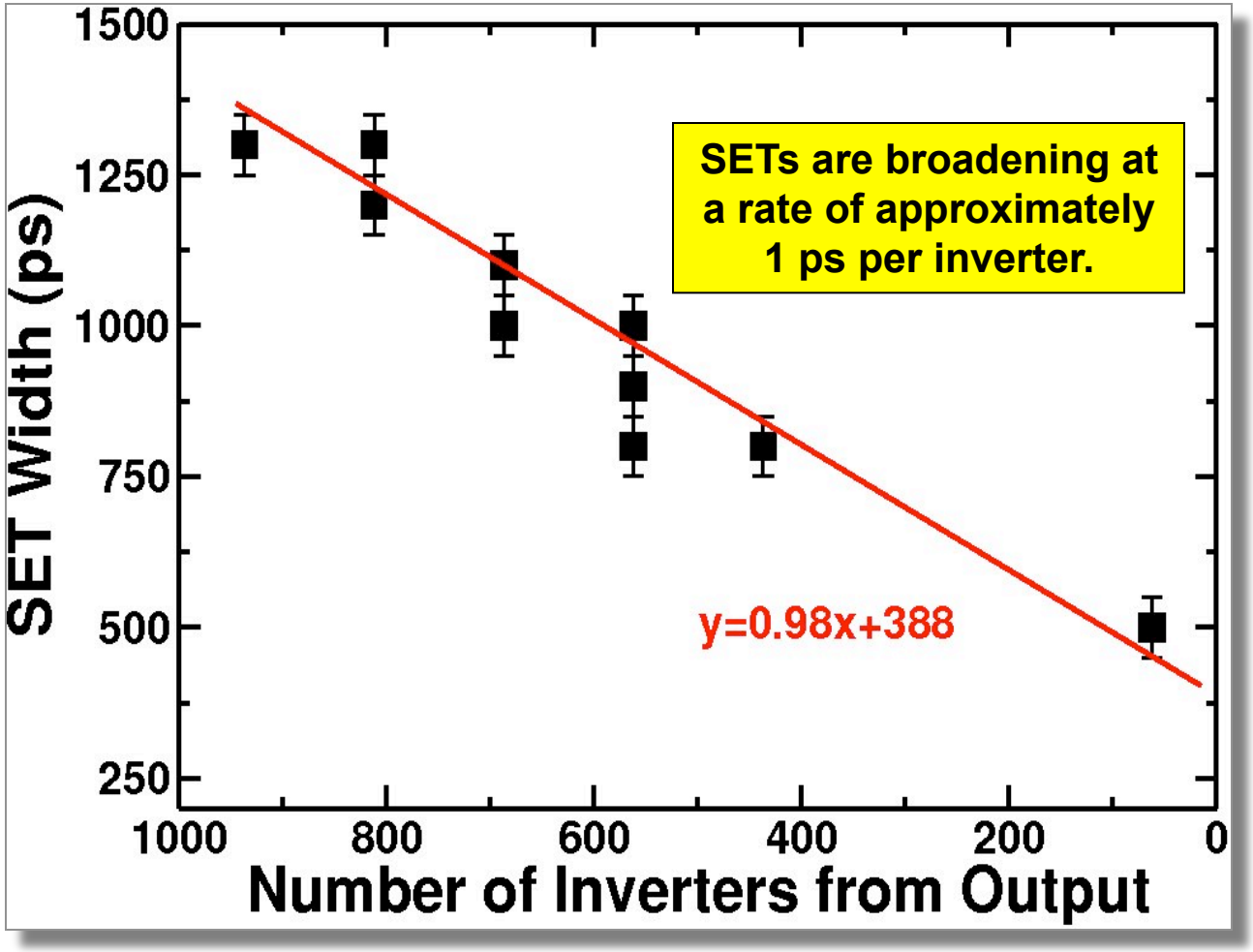
Target circuit consists of eight rows of 125 inverters



Laser strike location was center of each row



Pulse broadening is why long SETs were measured at the low LET values in the 90-nm Narasimham et al. data.

SET Measurements in Bulk CMOS

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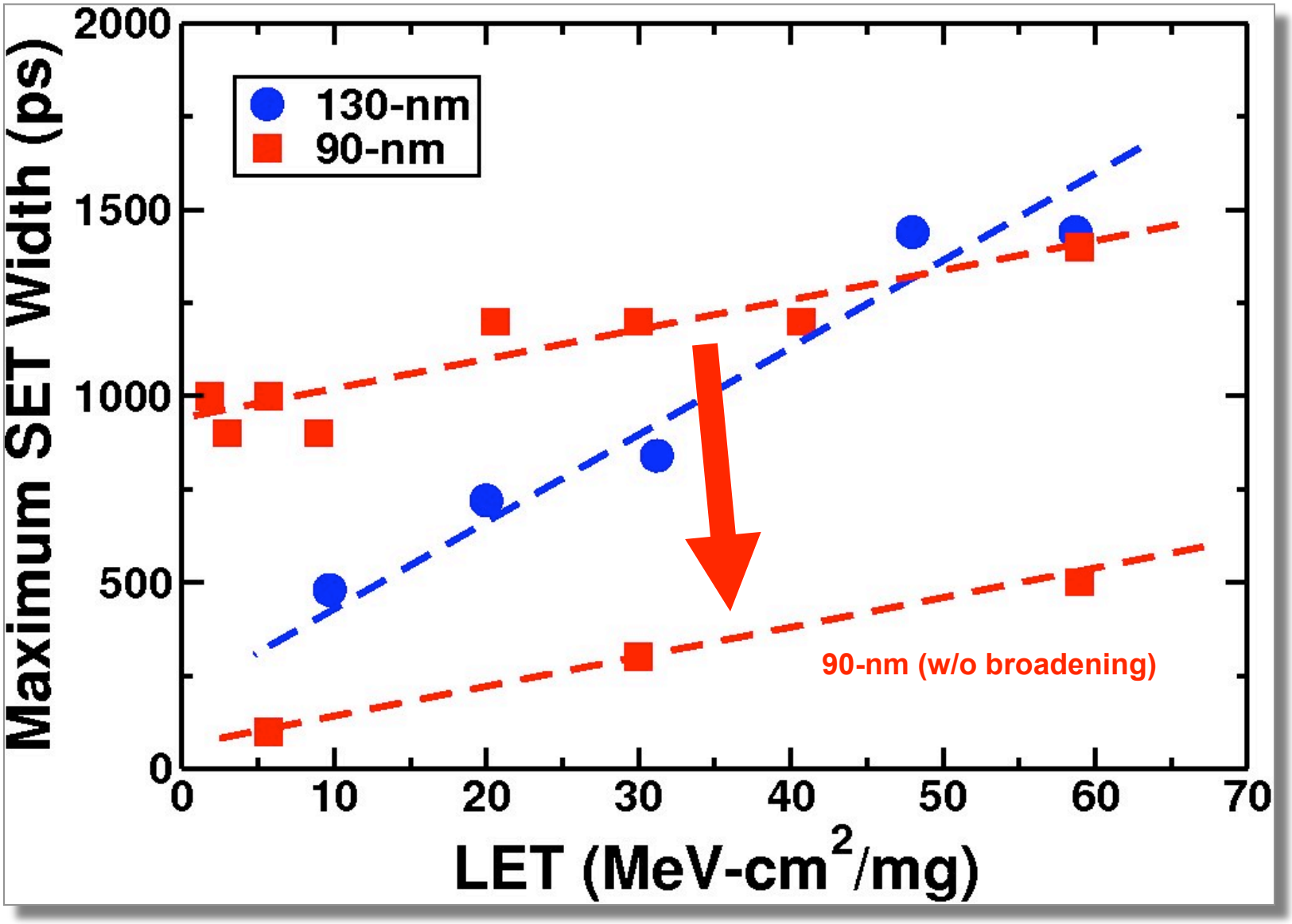

SET Measurements in Bulk CMOS

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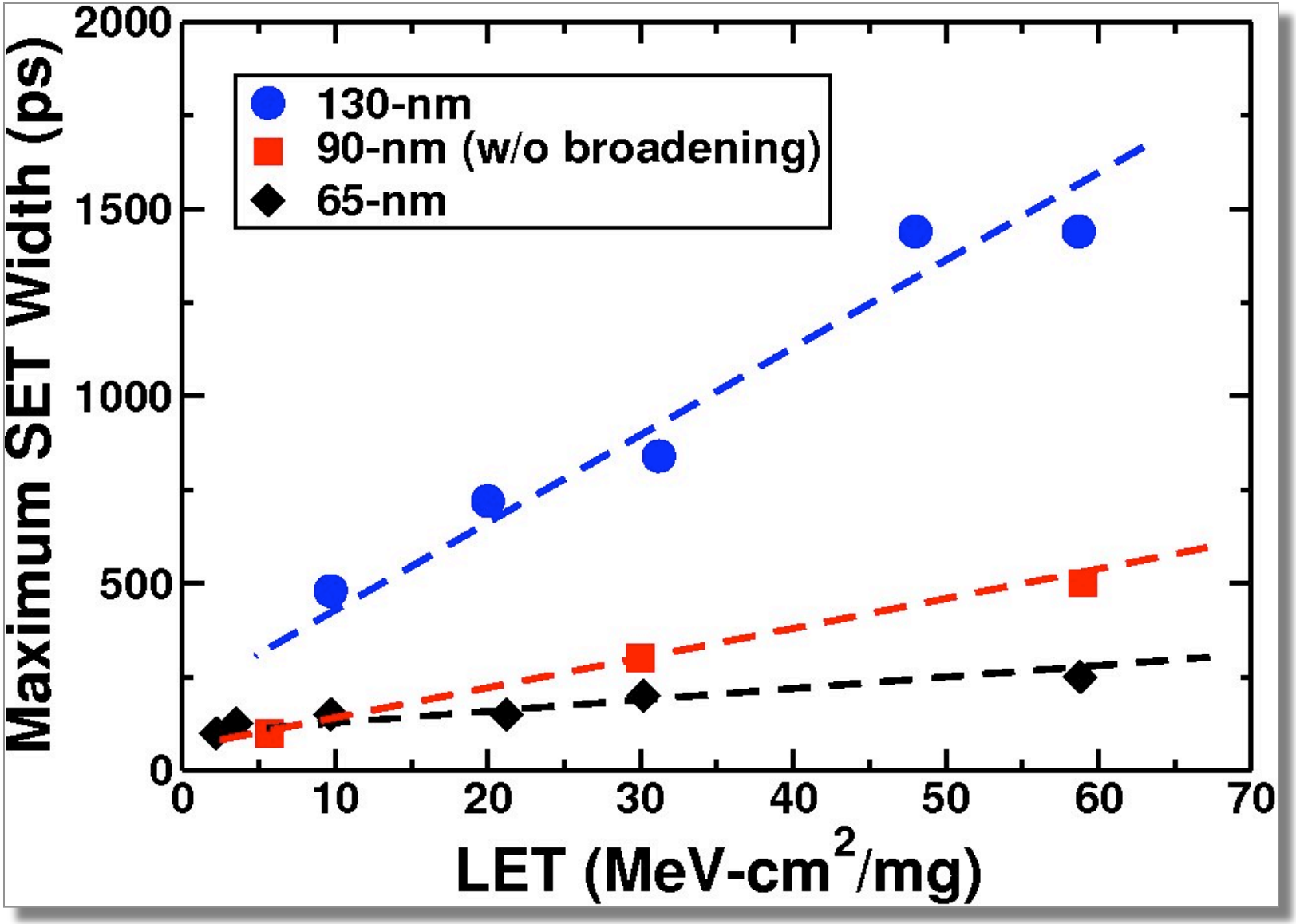

65-nm Pulse Broadening Experiment

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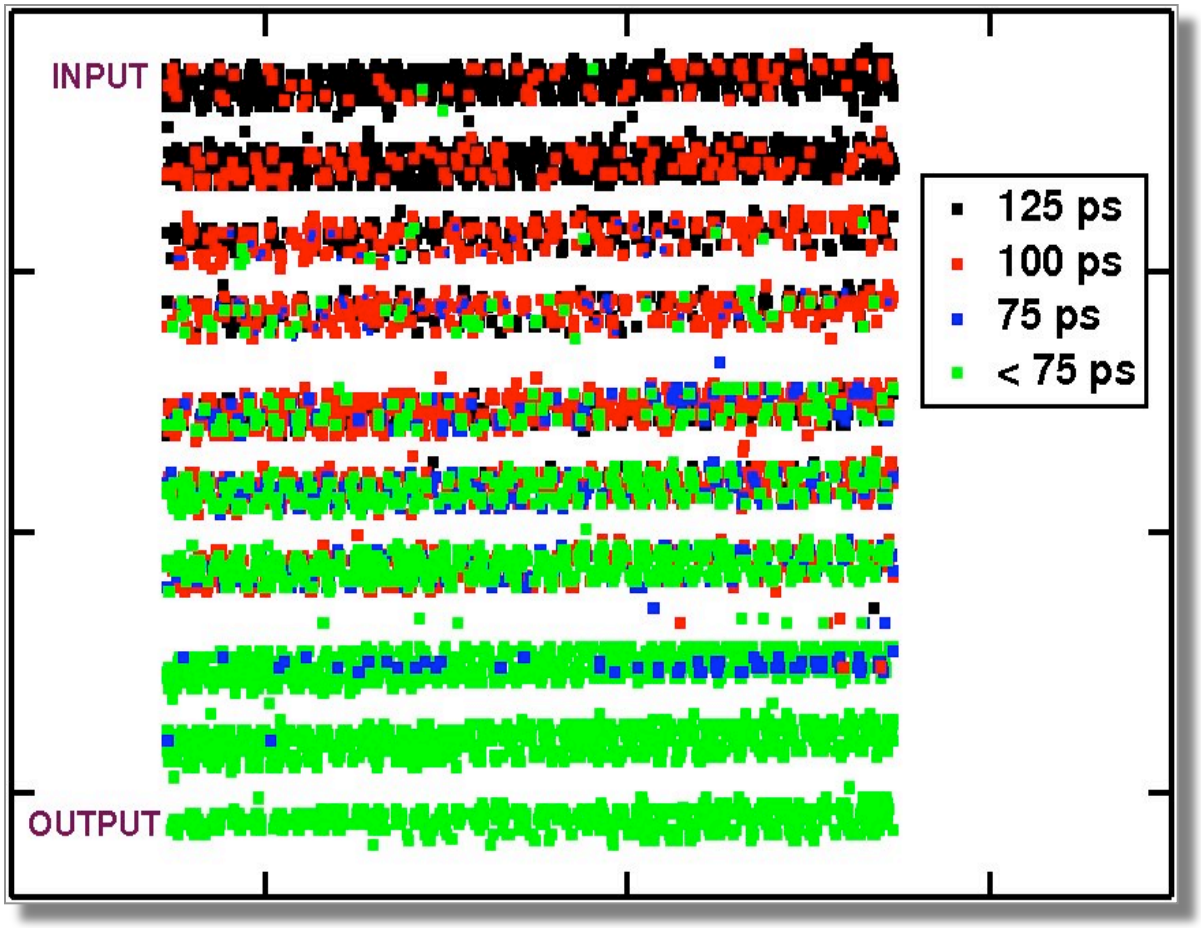
- Experiment performed at Sandia's Microbeam Facility using an ion with an LET of 5.4 MeV-cm^2/mg.
- The broadening rate was found to be about 0.1 ps/inverter.
- The 65-nm broadening rate is about an order of magnitude less than that of the 90-nm.



Each dot in this figure represents a location in the inverter chain target circuit at which an ion was able to create an SET.

SET Measurements in Bulk CMOS

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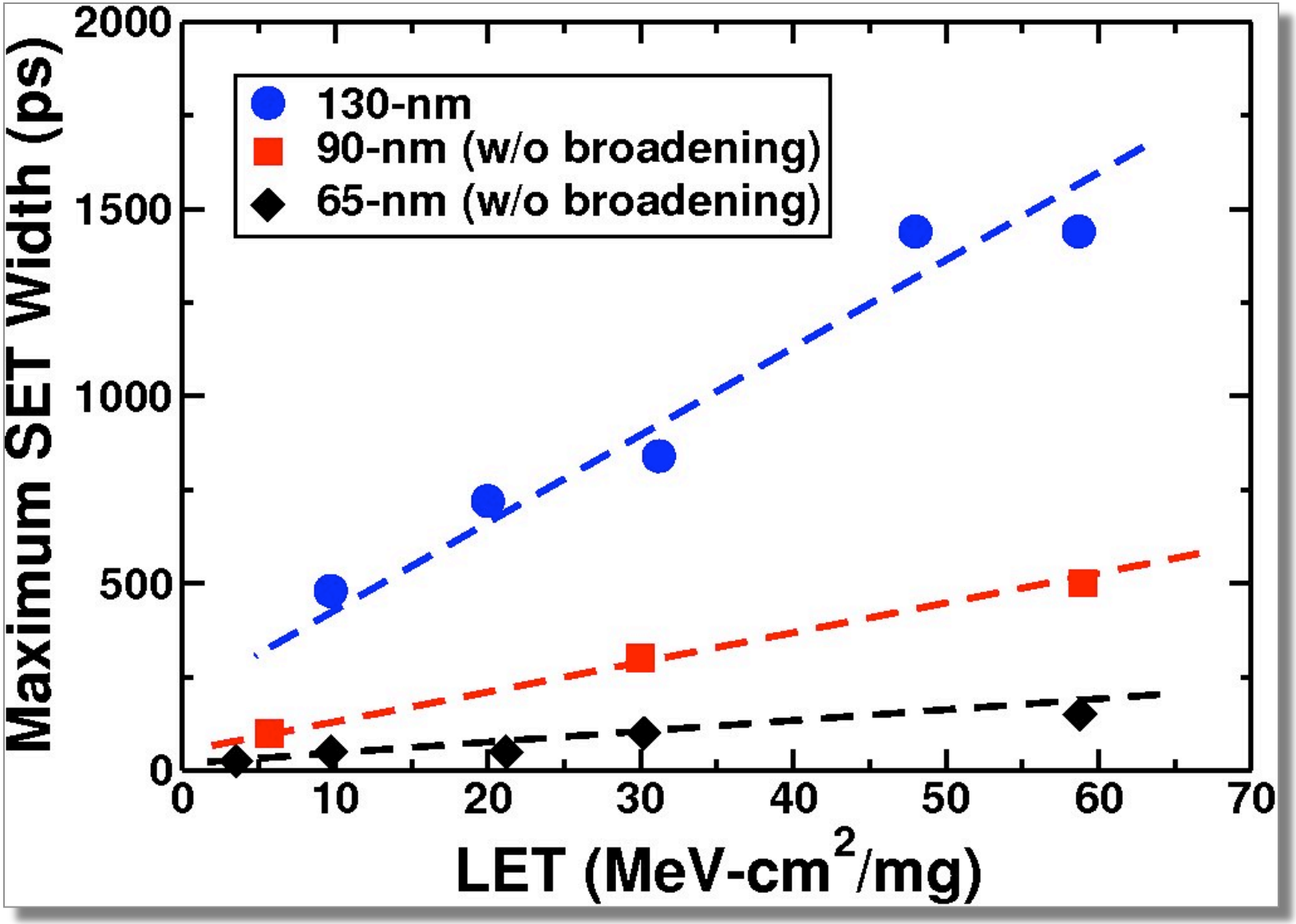

Elevated Temperature Experimental Results (Bulk)

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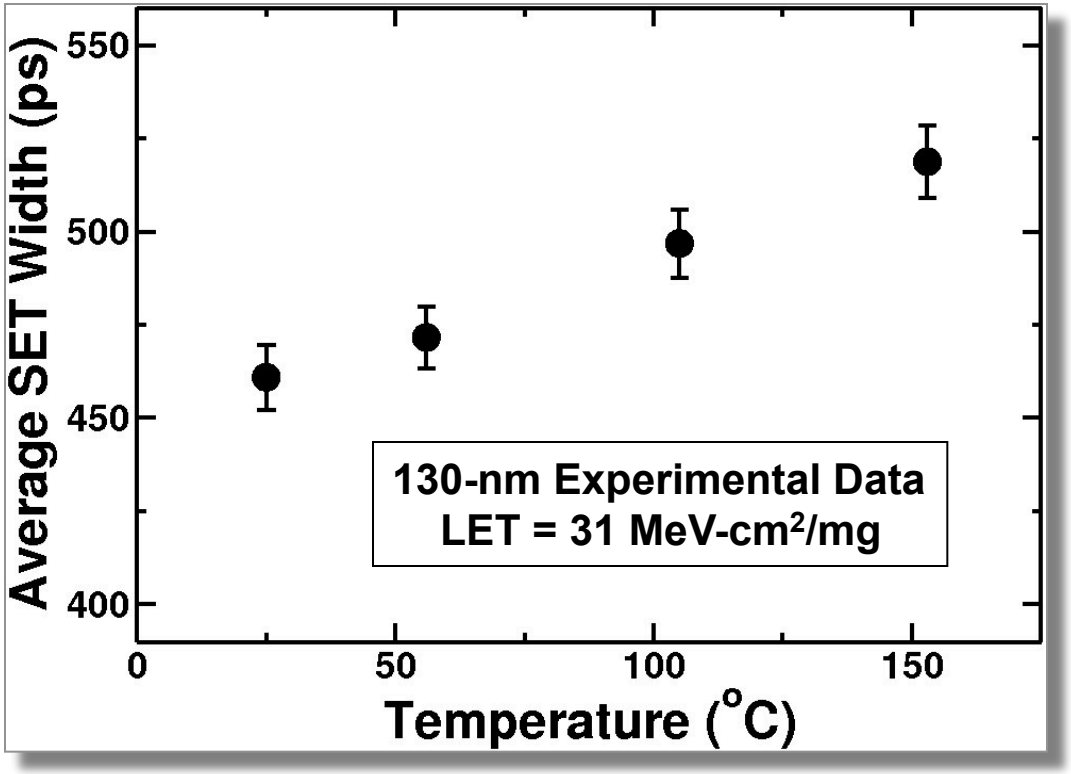

Data from Gadlage et al., IEEE TNS 2009

SET widths increased with temperature in all three bulk processes.

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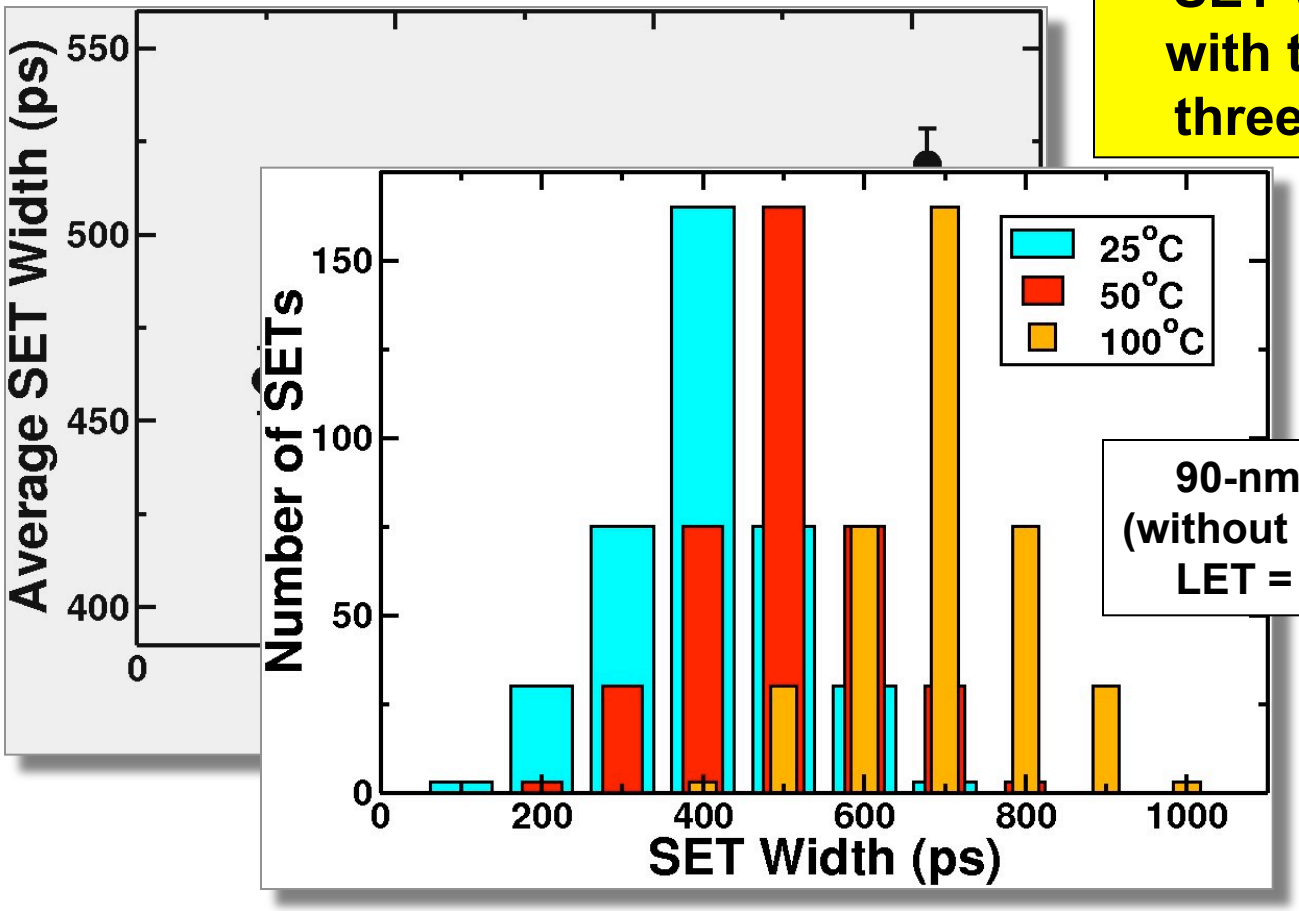

90-nm SET Histogram (without pulse broadening) LET = 52 MeV-cm^2/mg

Data from Gadlage et al., IEEE TDMR 2009

Elevated Temperature Experimental Results (Bulk)

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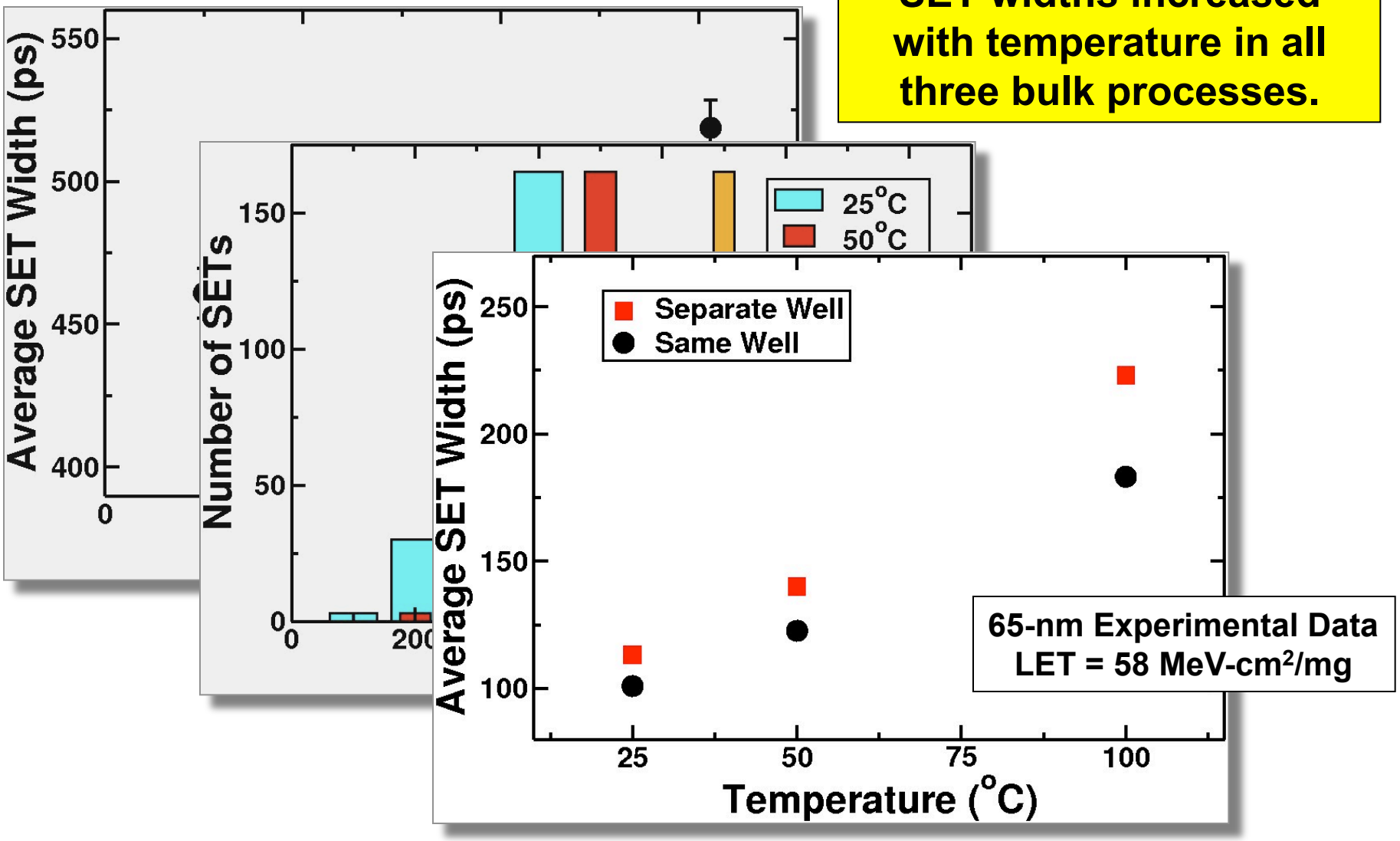

Data from Gadlage et al., IRPS 2010

130-nm Bulk TCAD Simulations

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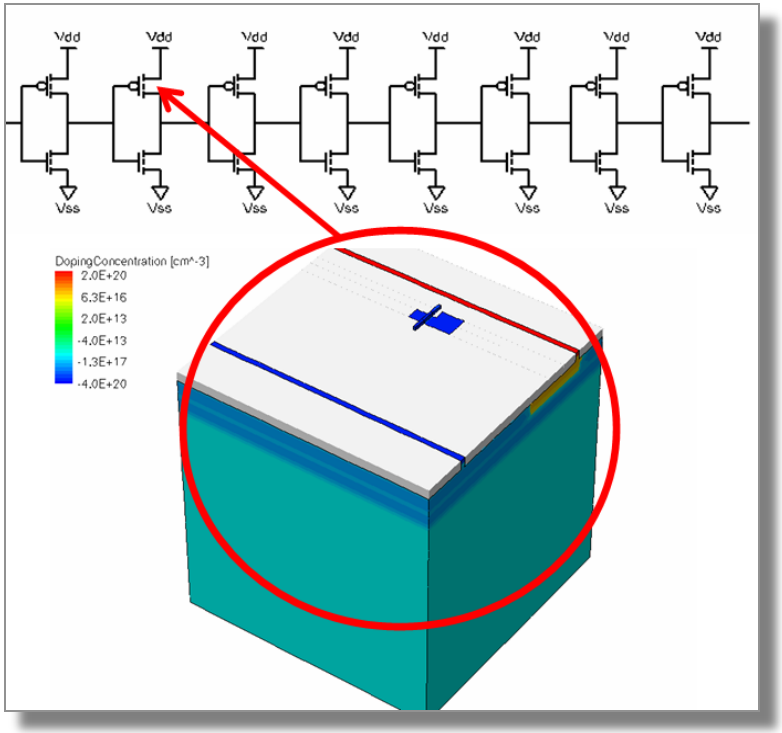
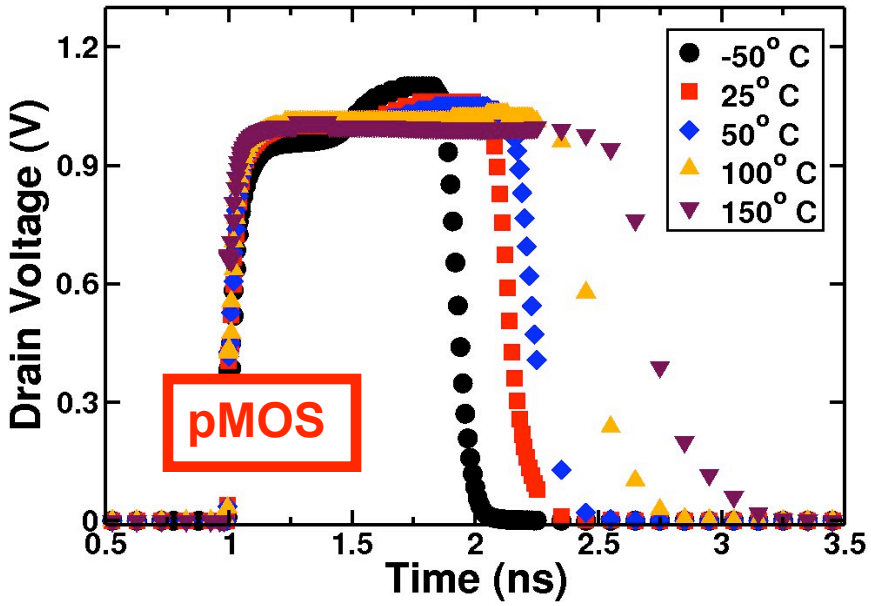
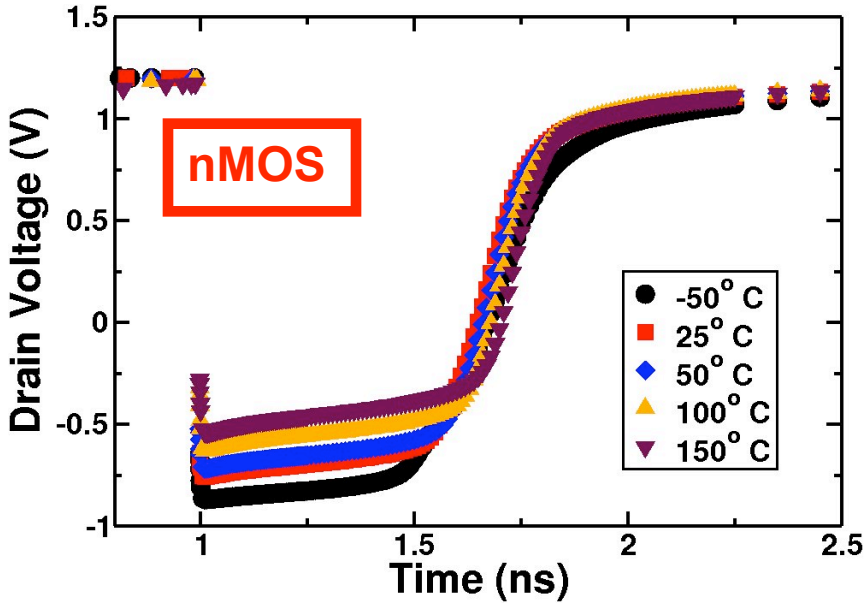
- TCAD simulations were performed to explore the mechanisms behind the increase in SET pulse widths in the bulk processes.
- Only pMOS strikes showed a change with temperature.







Bipolar Amplification Simulations

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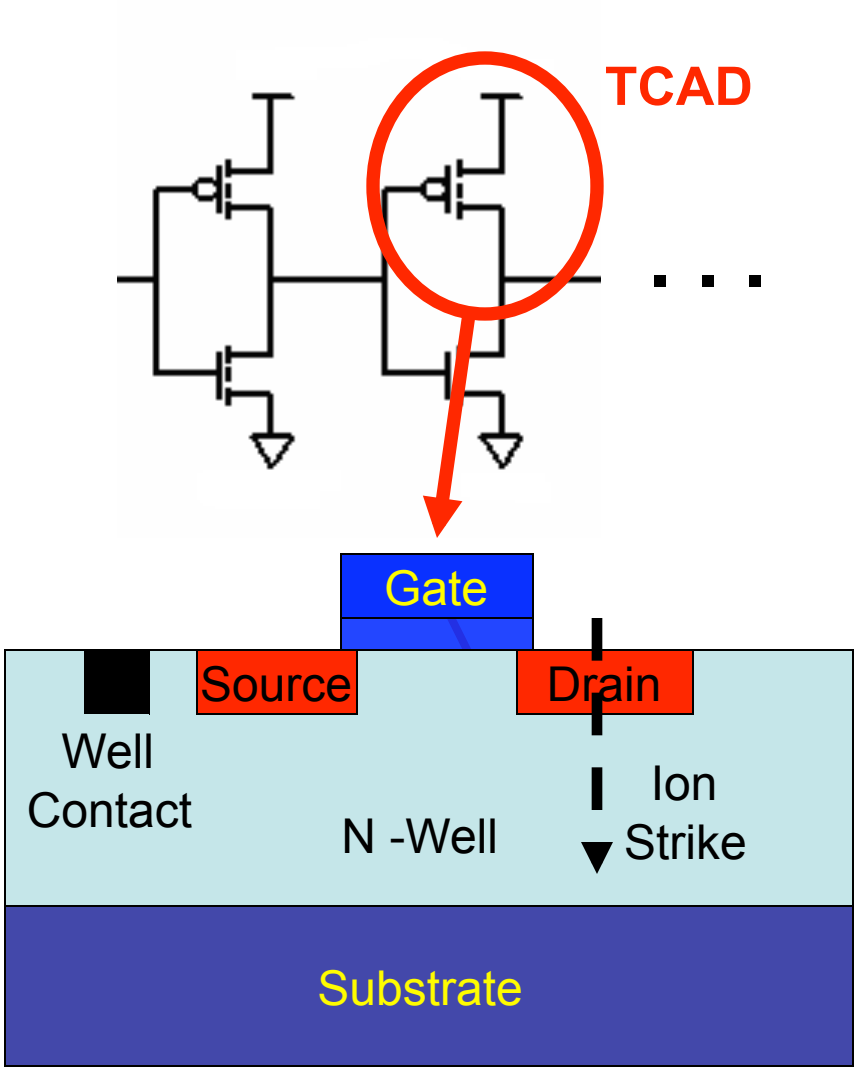
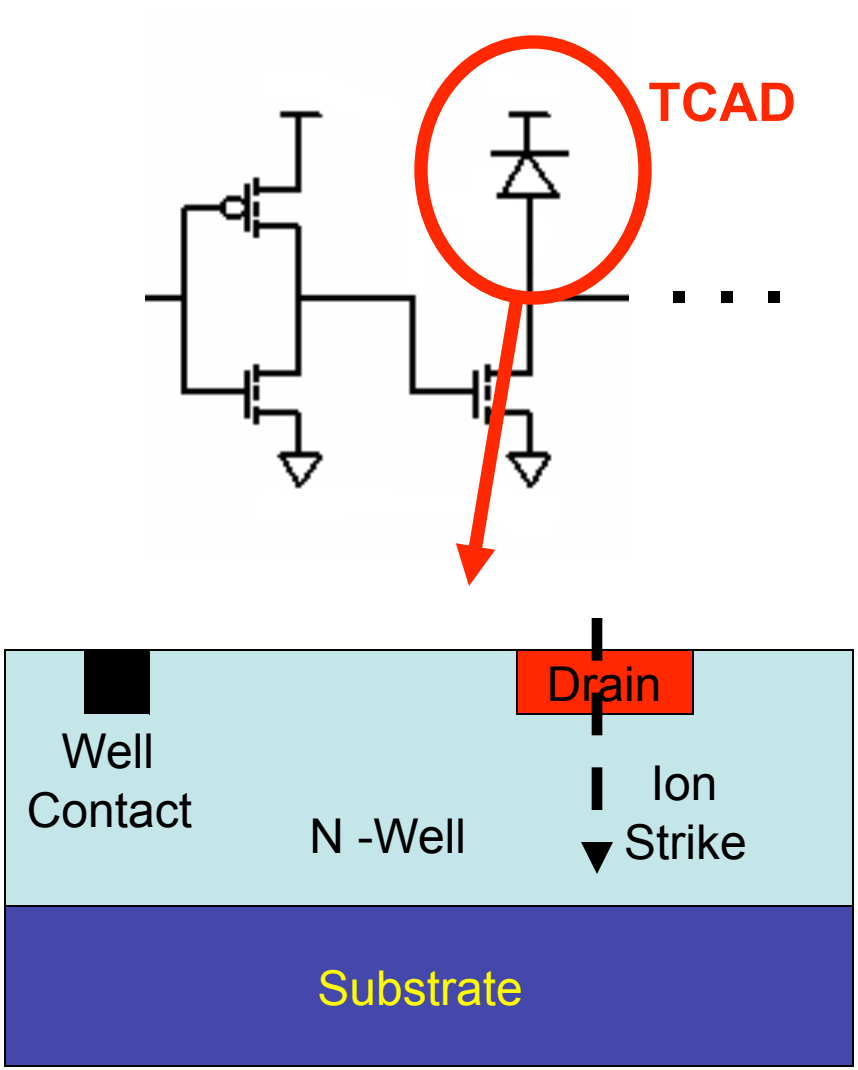
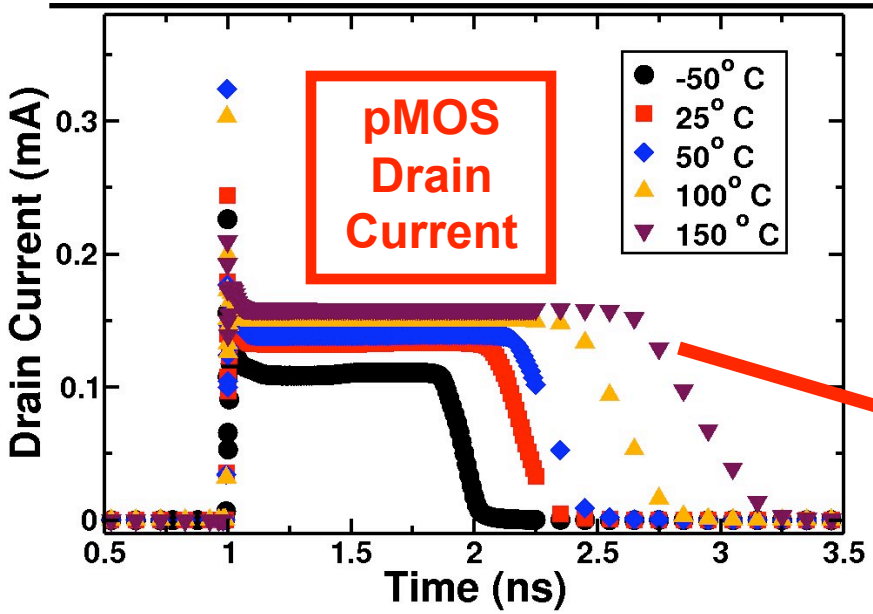


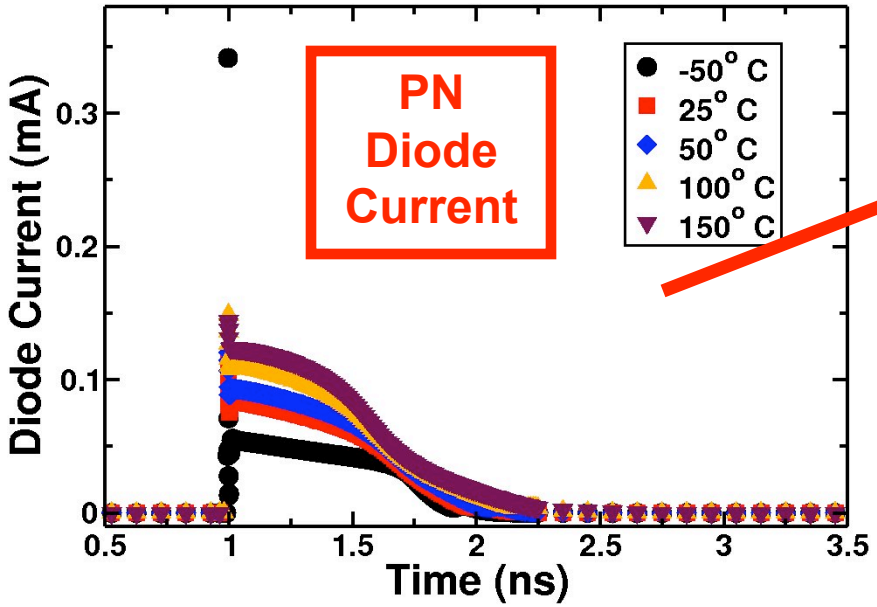
PMOS Simulation

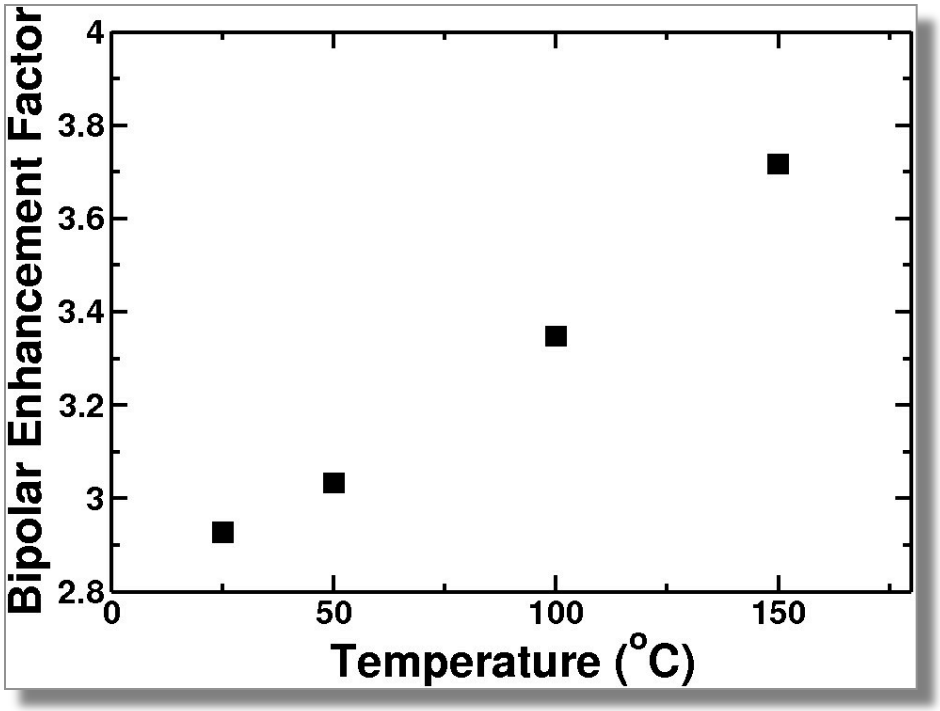


Diode Simulation

Bipolar Amplification Simulations







The parasitic bipolar effect increases with increasing temperature.

65-nm nMOS/pMOS Target Circuits

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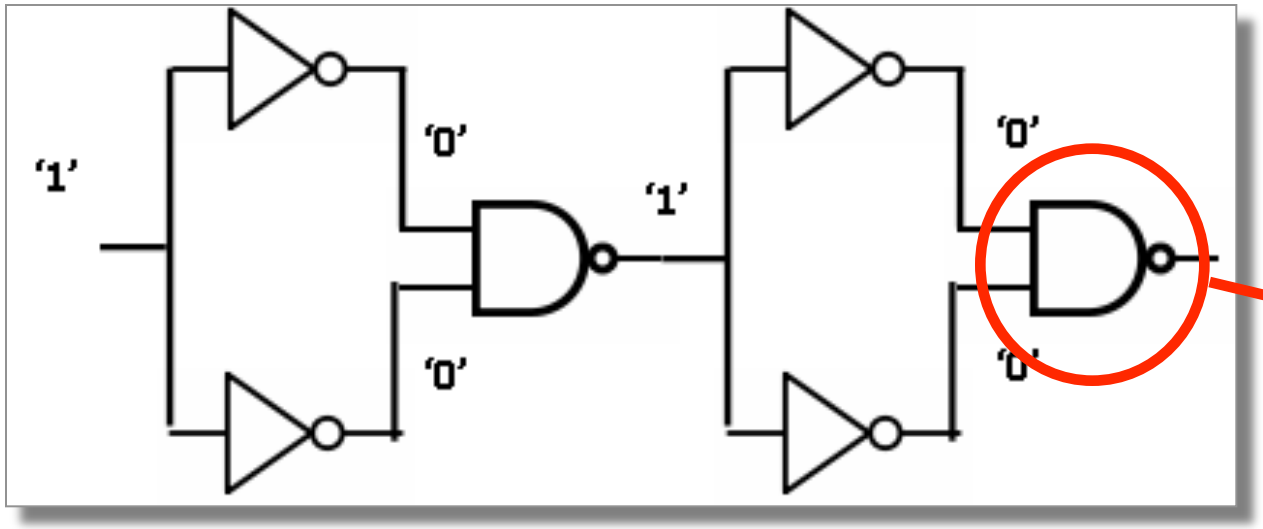
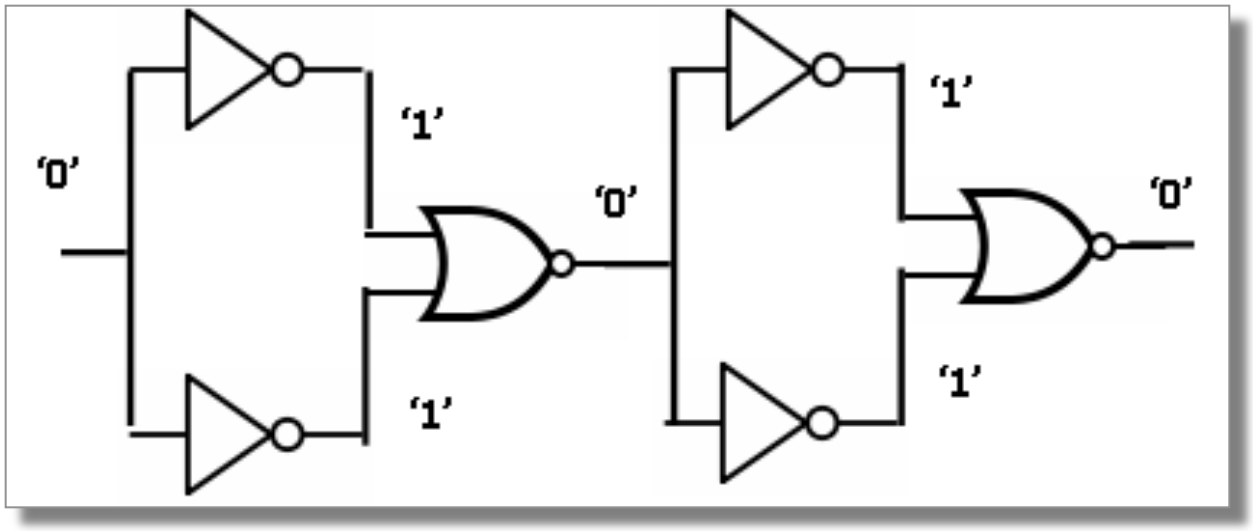
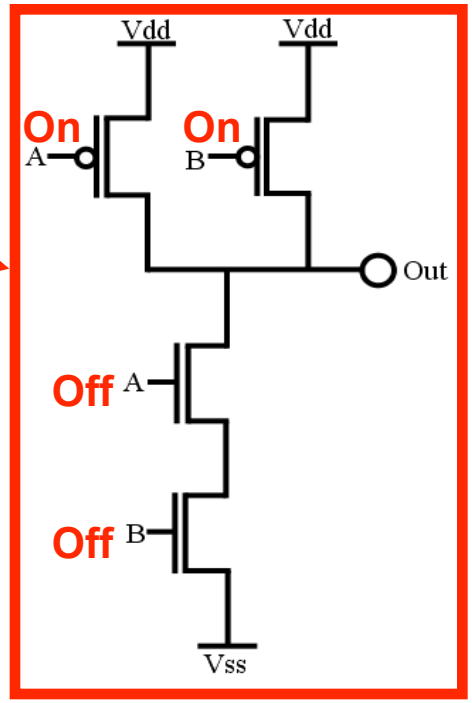


N-Hit Circuit



P-Hit Circuit



These test structures enable one to observe differences in SET widths between strikes on nMOS and pMOS devices.

Effect of Temperature on N/P Hits

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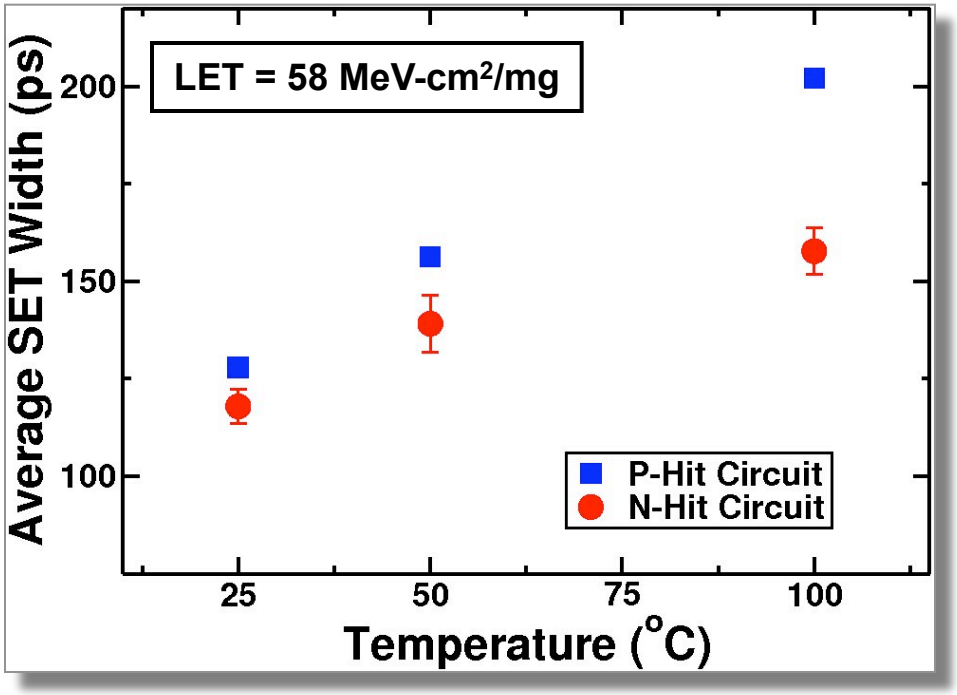
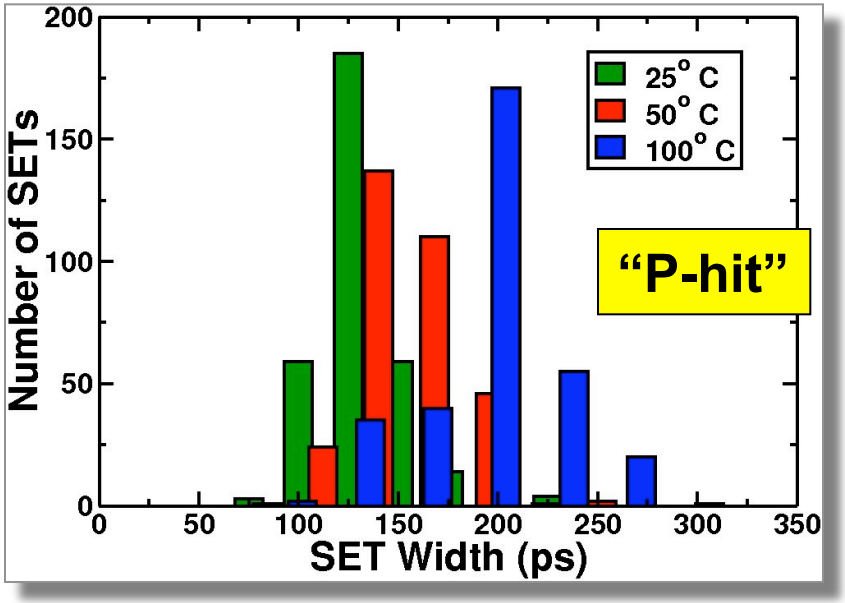
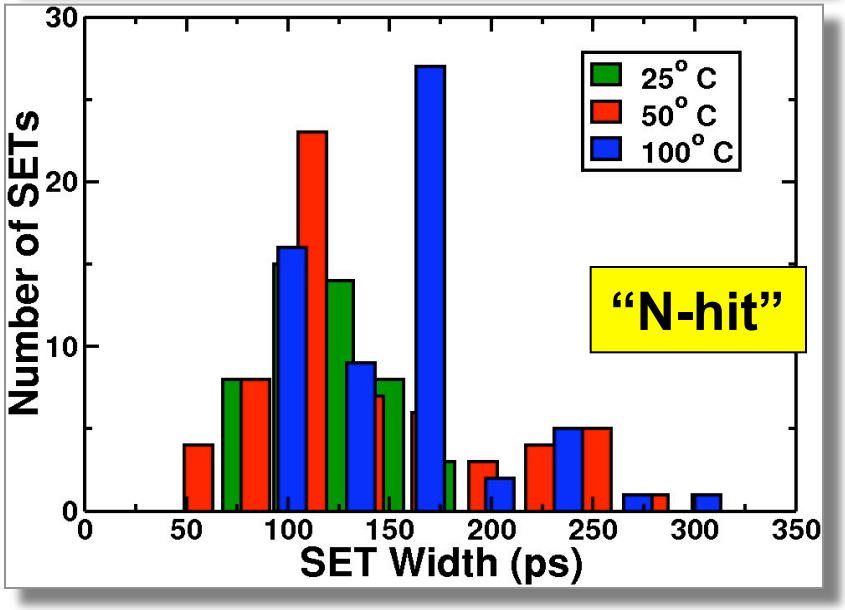
- Less change in SET width with temperature was observed in the "N-Hit" circuit than in the "P-Hit" circuit.
- Experimentally confirms that SETs induced on pMOS transistors increase more with temperature than SETs induced on nMOS transistors.







Conclusions

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- **Presented some of the first SET measurements in a 65-nm bulk silicon technology**
  - Provided insight into SET width trends in bulk technologies as feature sizes shrink
- **SET pulse width measurements over temperature in three bulk technologies**
  - SET widths increased with temperature
- **The increase in SET widths in bulk technologies with temperature was shown to be due primarily to an enhancement in bipolar amplification in pMOS transistors.**
- **Elevated temperature data from "N/P Hit" test structures confirm that temperature changes affect SETs induced in pMOS transistors more than in nMOS transistors.**