June , 2009

Radiation Effects on Emerging Electronic Materials and Devices

# Radiation Effects in Emerging Materials

# Overview


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Vanderbilt University

and

Rutgers University

# Topics of Interest

I. New defect profiling technique

II. Progress with SiC

1. Nitrogen induced trapping

2. Mobility limitations

III. Comments on oxides

# Disorder-induced electronic structure modifications in GaAs studied using coherent acoustic phonon spectroscopy

**A. Steigerwald**, Y. Xu, J. Qi, J. Gregory1, X. Liu, J.K. Furdyna
K. Varga, A.B. Hmelo, G. Lüpke, L.C. Feldman, **N. Tolk**

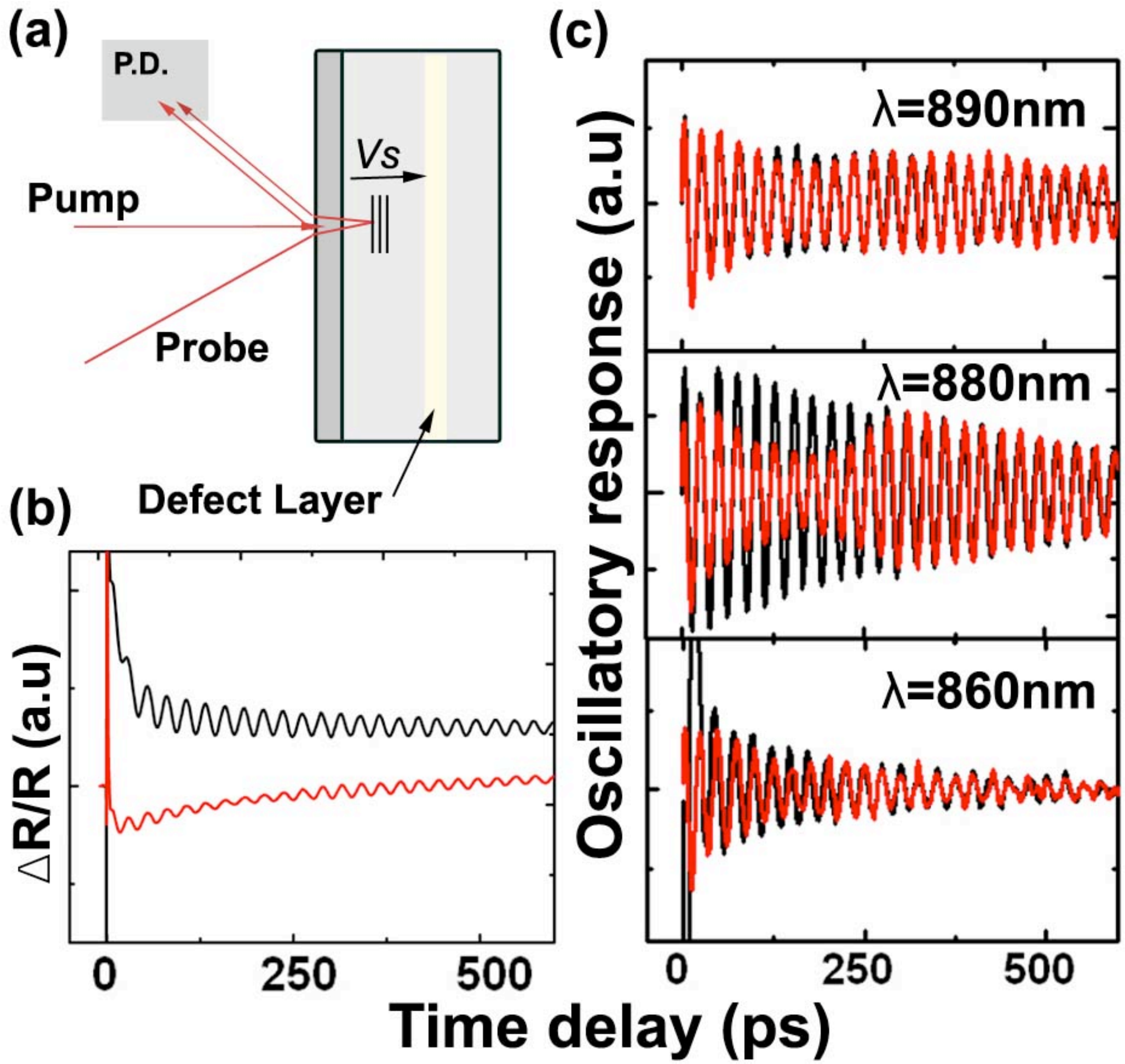
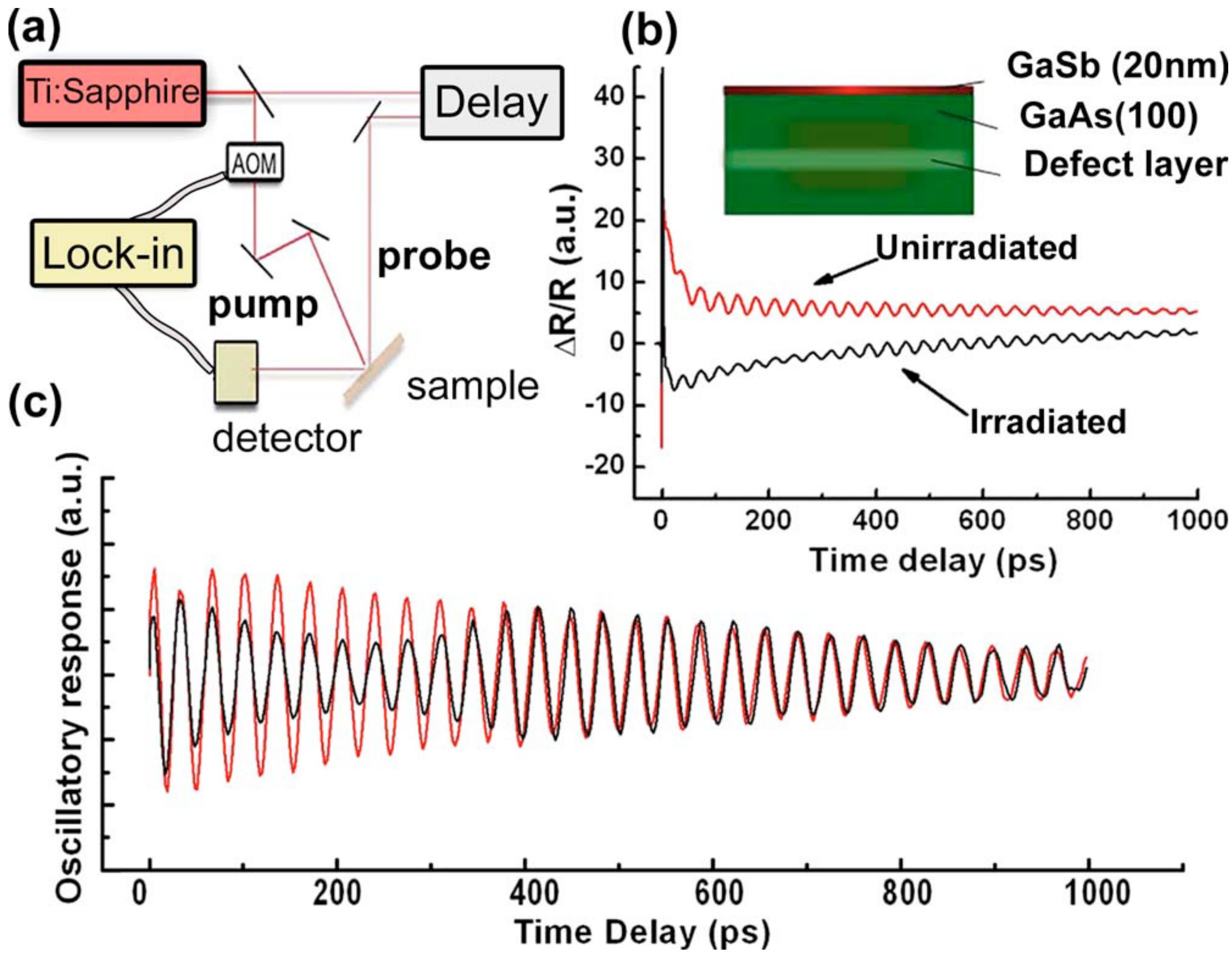
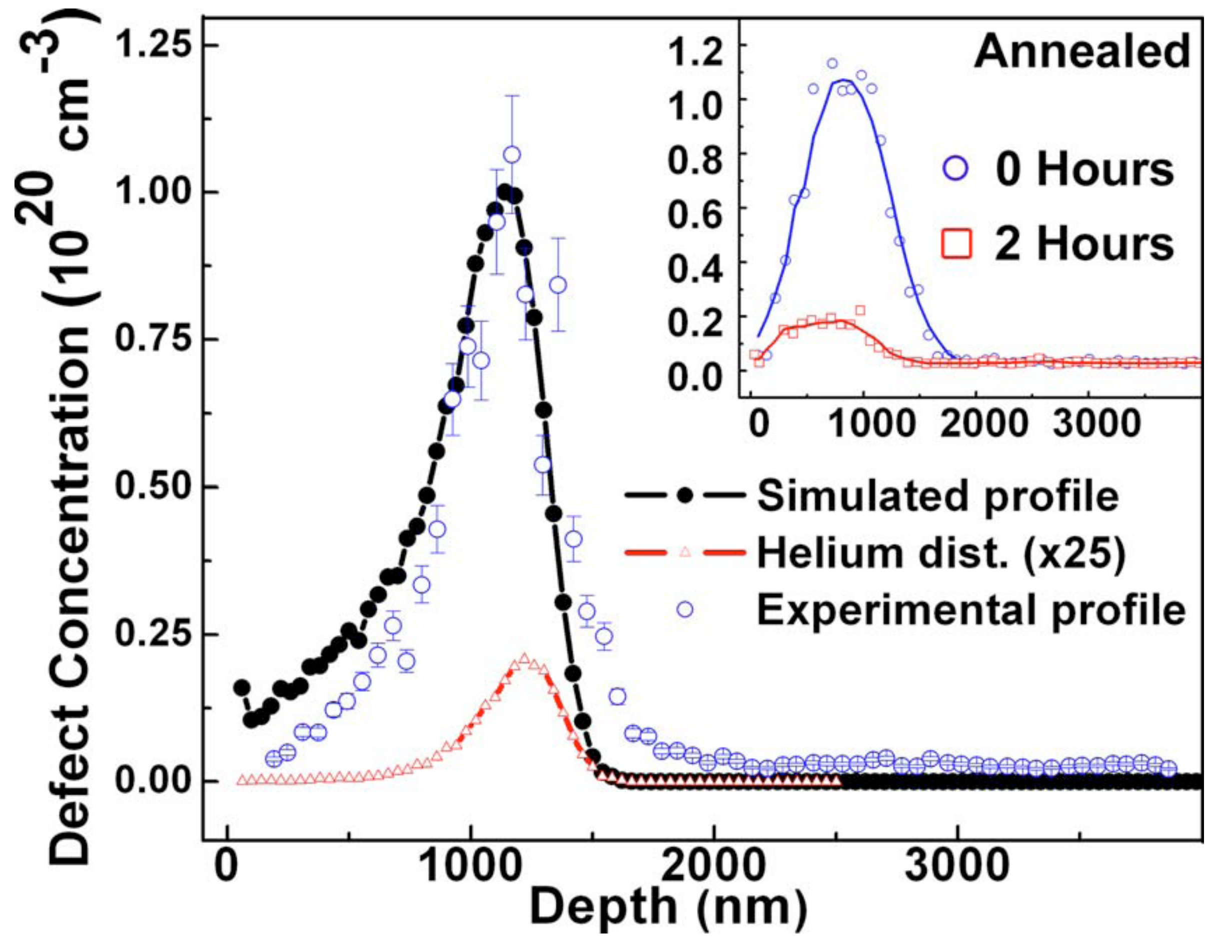

(a)
P.D.
Pump
Vs
Probe
Defect Layer
(b)
ΔR/R (a.u)
0
250
500
(c)
λ=890nm
λ=880nm
λ=860nm
Oscillatory response (a.u)
0
250
500
Time delay (ps)

Figure 1




Showing the (a) experimental setup, (b) total timeresolved pump-probe optical response of the undamaged and damaged samples, and (c) the subtracted oscillatory responses displaying strong amplitude modulation observed in the damaged sample in the first 400 ps, as compared to the undamaged response.




(a) Experimental defect concentration profile for a sample irradiated at 325 keV at a dosage of 7 X $10^{13}$ ions/cm$^2$. Peak defect concentration observed to be near 1.1 X $10^{20}$ cm$^{-3}$, agreeing well with simulated profiles for total damage (black) and helium ion distribution (red, enhanced 25X) from TRIM code. (b) Experimentally measured defect profiles before (blue) and after (red) 2 h of thermal annealing at 300 °C.

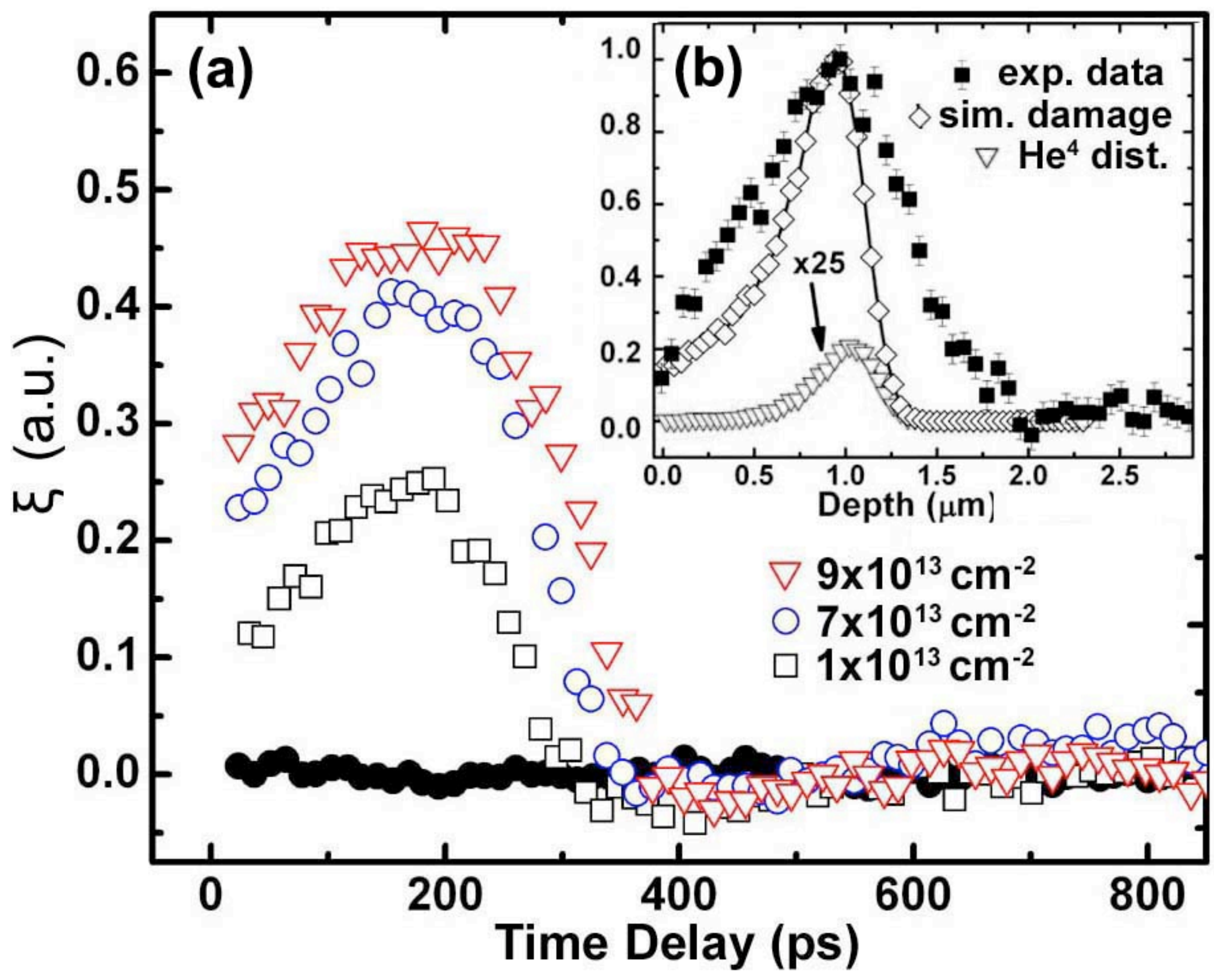

(a)
(b)
exp. data
sim. damage
He⁴ dist.
x25
Depth (μm)
ξ (a.u.)
Time Delay (ps)
9x10¹³ cm⁻²
7x10¹³ cm⁻²
1x10¹³ cm⁻²

Figure 2

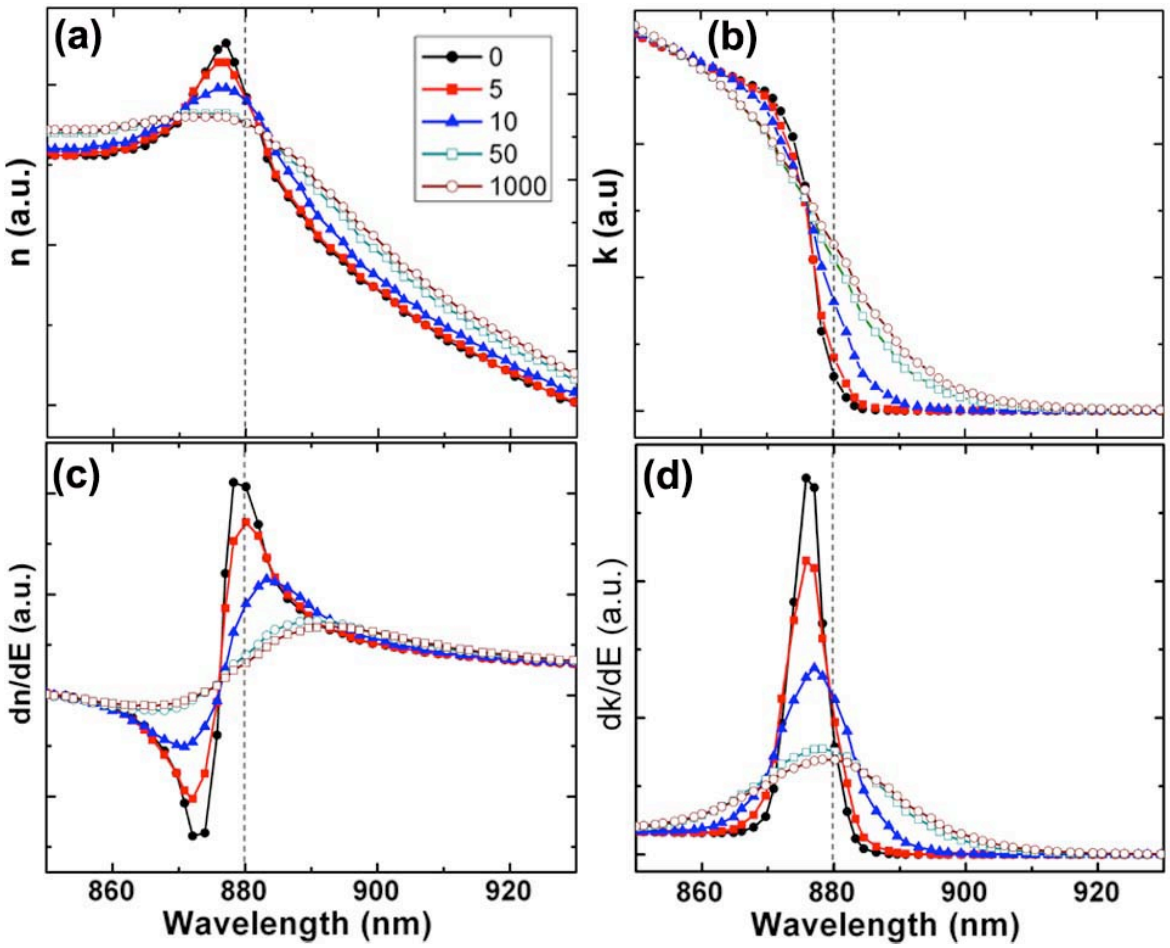

(a)
(b)
(c)
(d)
0
5
10
50
1000
n (a.u.)
k (a.u)
dn/dE (a.u.)
dk/dE (a.u.)
860
880
900
920
Wavelength (nm)

Figure 3

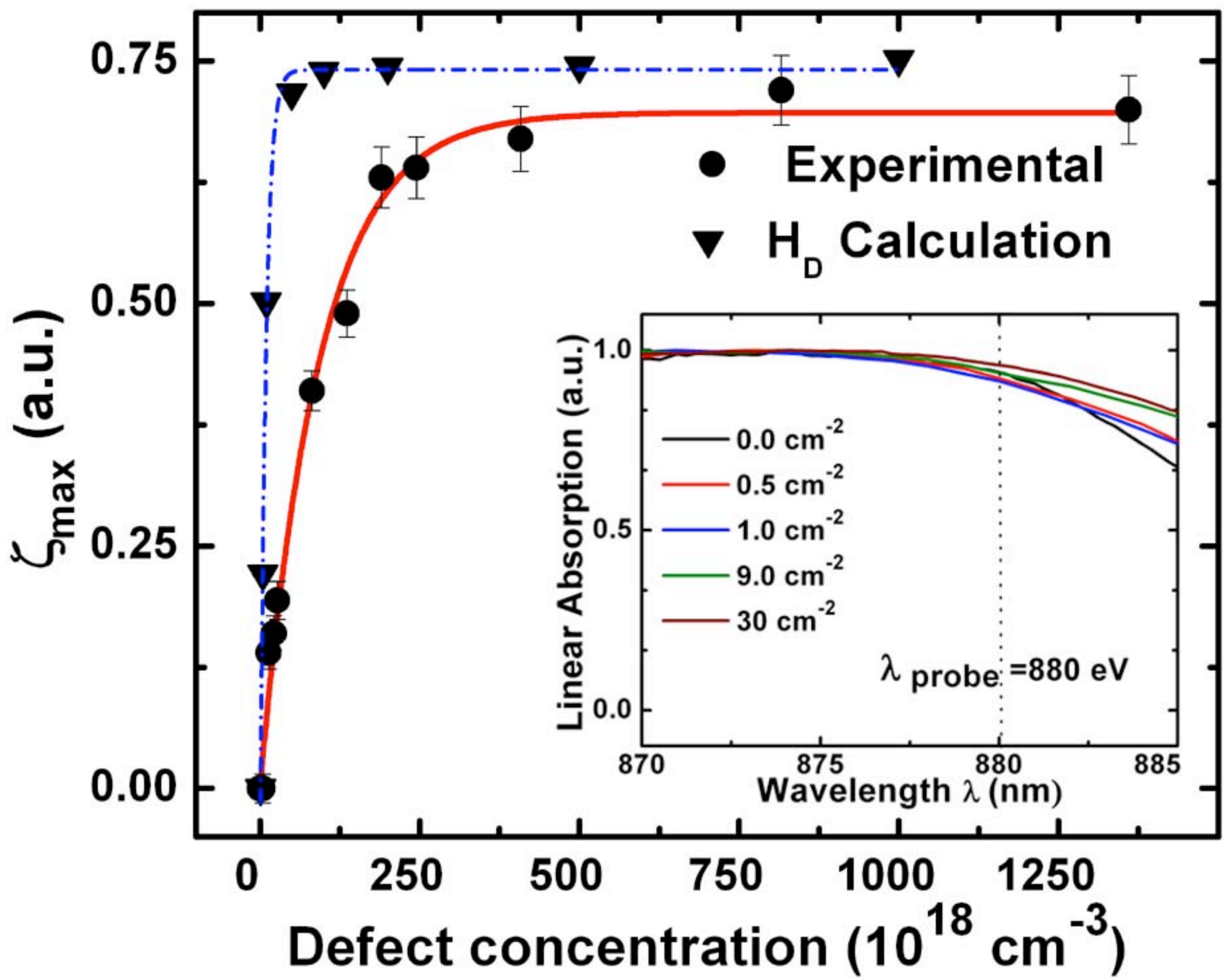

0.75
0.50
0.25
0.00
$\zeta_{max}$ (a.u.)
0
250
500
750
1000
1250
Defect concentration ($10^{18}$ $cm^{-3}$)
Experimental
$H_D$ Calculation
Linear Absorption (a.u.)
1.0
0.5
0.0
870
875
880
885
Wavelength λ (nm)
0.0 $cm^{-2}$
0.5 $cm^{-2}$
1.0 $cm^{-2}$
9.0 $cm^{-2}$
30 $cm^{-2}$
$\lambda_{probe}$ =880 eV

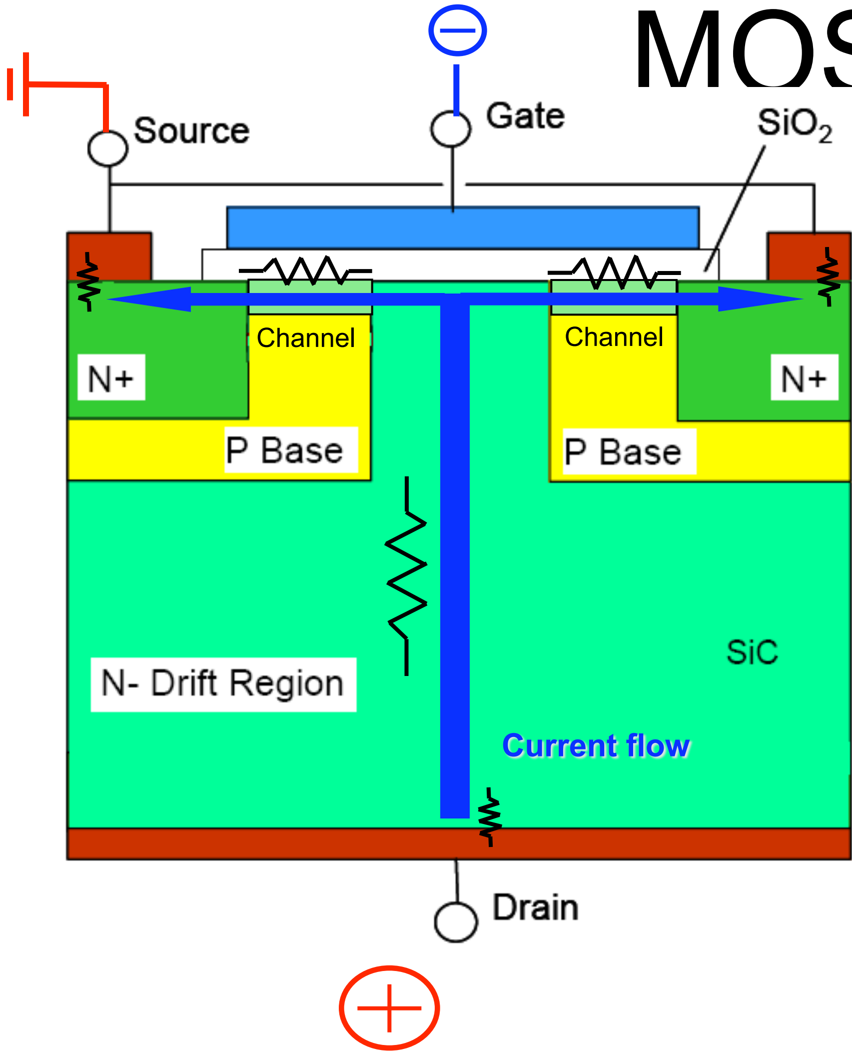
Figure 4

# Scaling between nitrogen content and carrier trap densities at the $SiO_2$ / SiC interface

Vanderbilt University
J. Rozen, L. C. Feldman

Auburn University
J. R. Williams

# The SiC vertical power MOSFET




- OFF state

For a given blocking voltage, the SiC drift region can be **thinner** and/or **more highly doped** than Si

- ON state

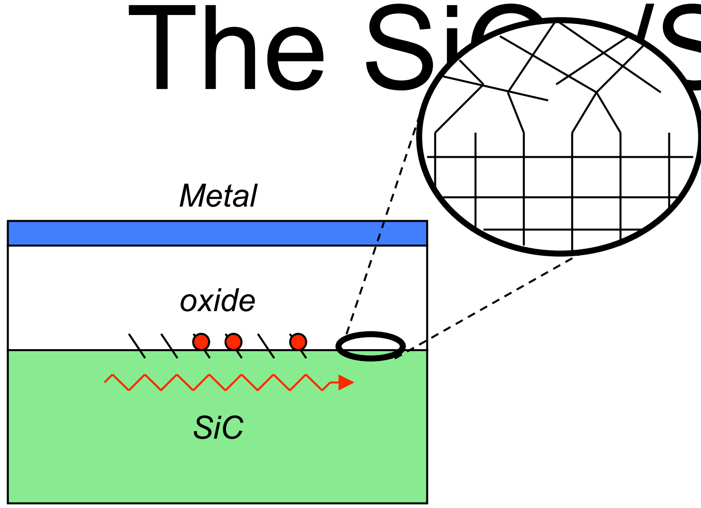
$R_{Tot} = R_{Drift} + R_{Channel} + R_{Contacts} + \ldots$

High breakdown field → small in SiC

poor $SiO_2$ / SiC interface → large in SiC

$\mu_{INT} \ll \mu_{BULK}$

# The SiO$_2$/SiC interface




- The interface state density

  $D_{it}$

  is responsible for $R_{Channel}$

- Probed by capacitance-voltage measurements on MOS capacitors

**Origin of interface states**

Complex oxidation

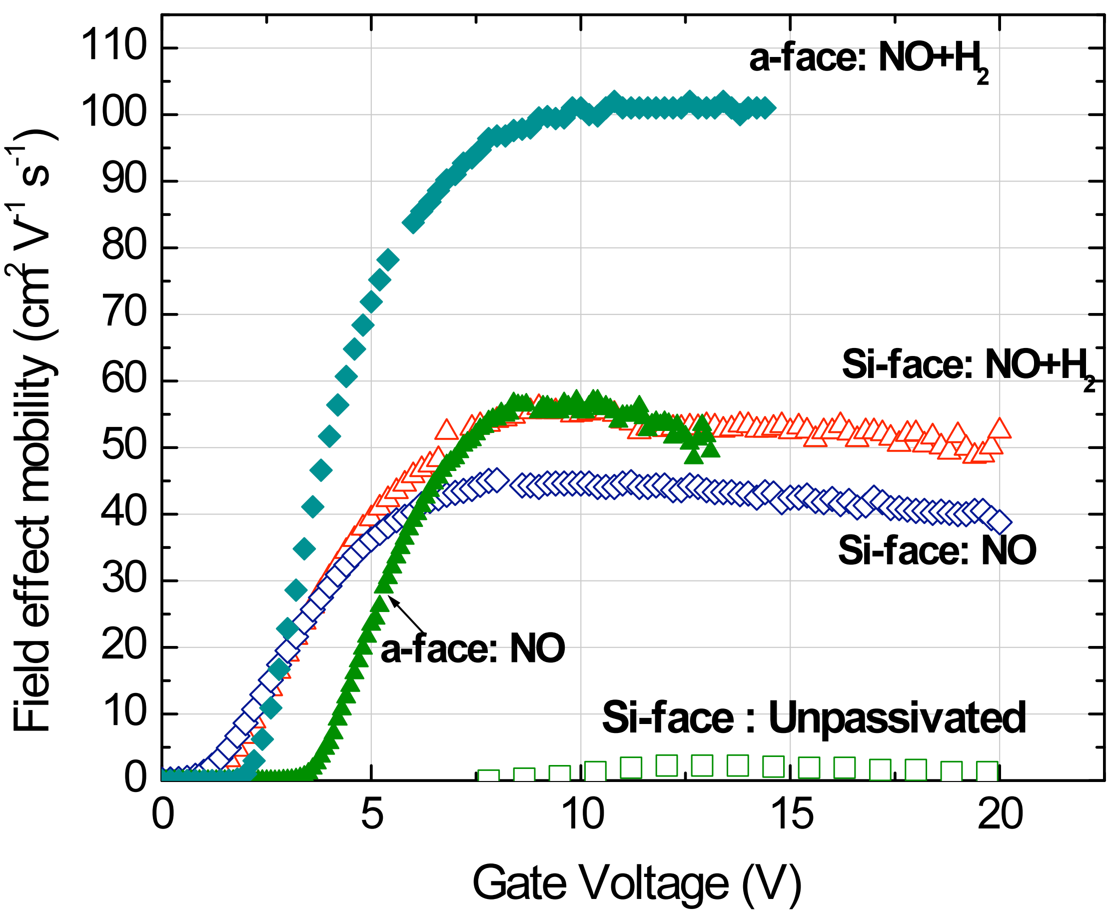
Wide band-gap

# MOSFET Mobility: Si-face and a-face

• **Record high mobility for (NO+$H_2$) a-face MOSFETs**

**$\mu_{max} \approx 100\ cm^2\ V^{-1}\ s^{-1}$**

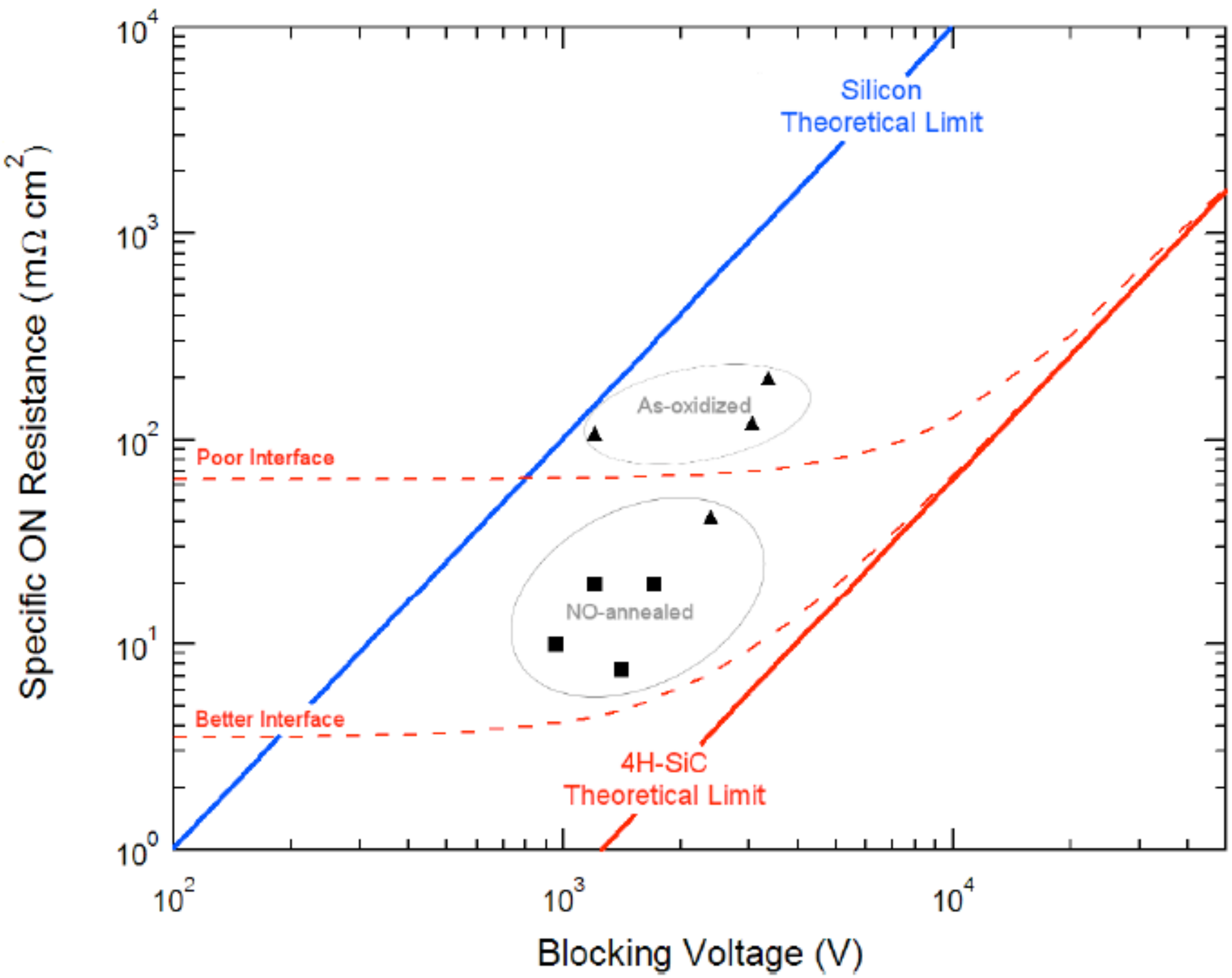
S.Dhar, L. C. Feldman, S. Wang and J. R. Williams, to be published in MRS bulletin (April 2005).




• Highest field effect mobility inspite of having similar $D_{it}$ as Si-face

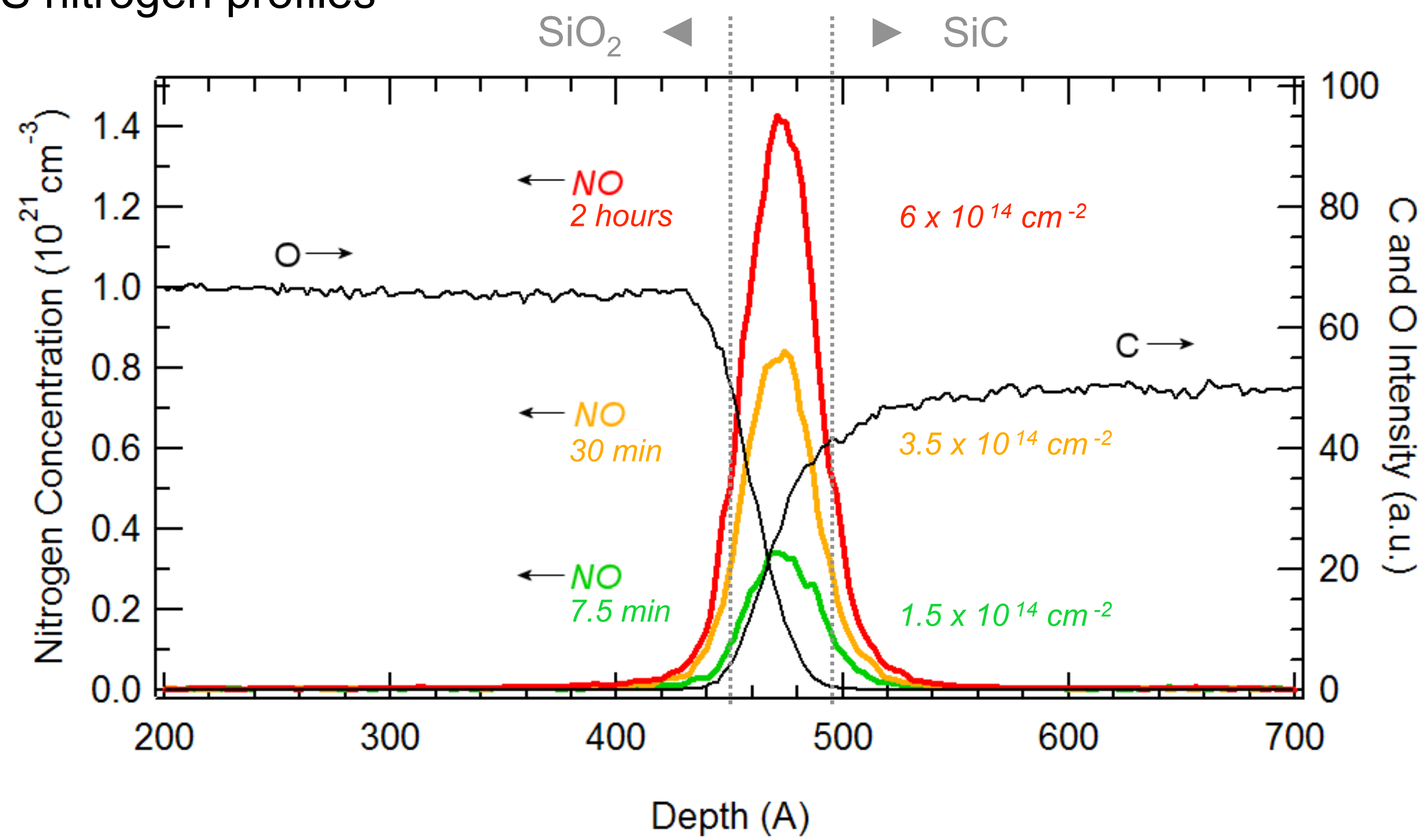
- Traps $E_C$- E < 0.1 eV?
- Interface roughness?
- Other reasons?

# Reduction of MOSFET



# Kinetics of the nitrogen uptake

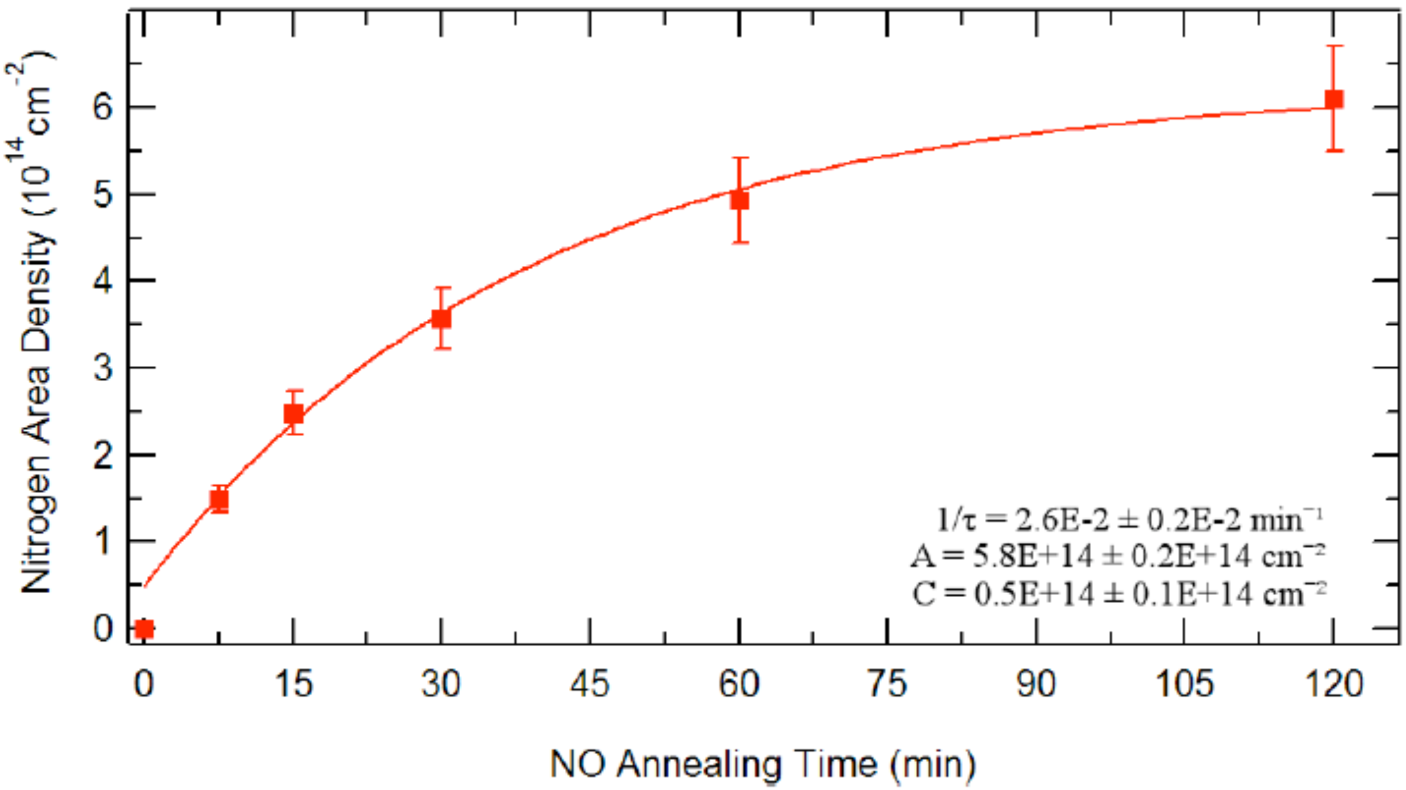
SIMS nitrogen profiles




→ Nitrogen confined at the interface (within ~ 1nm from EELS)

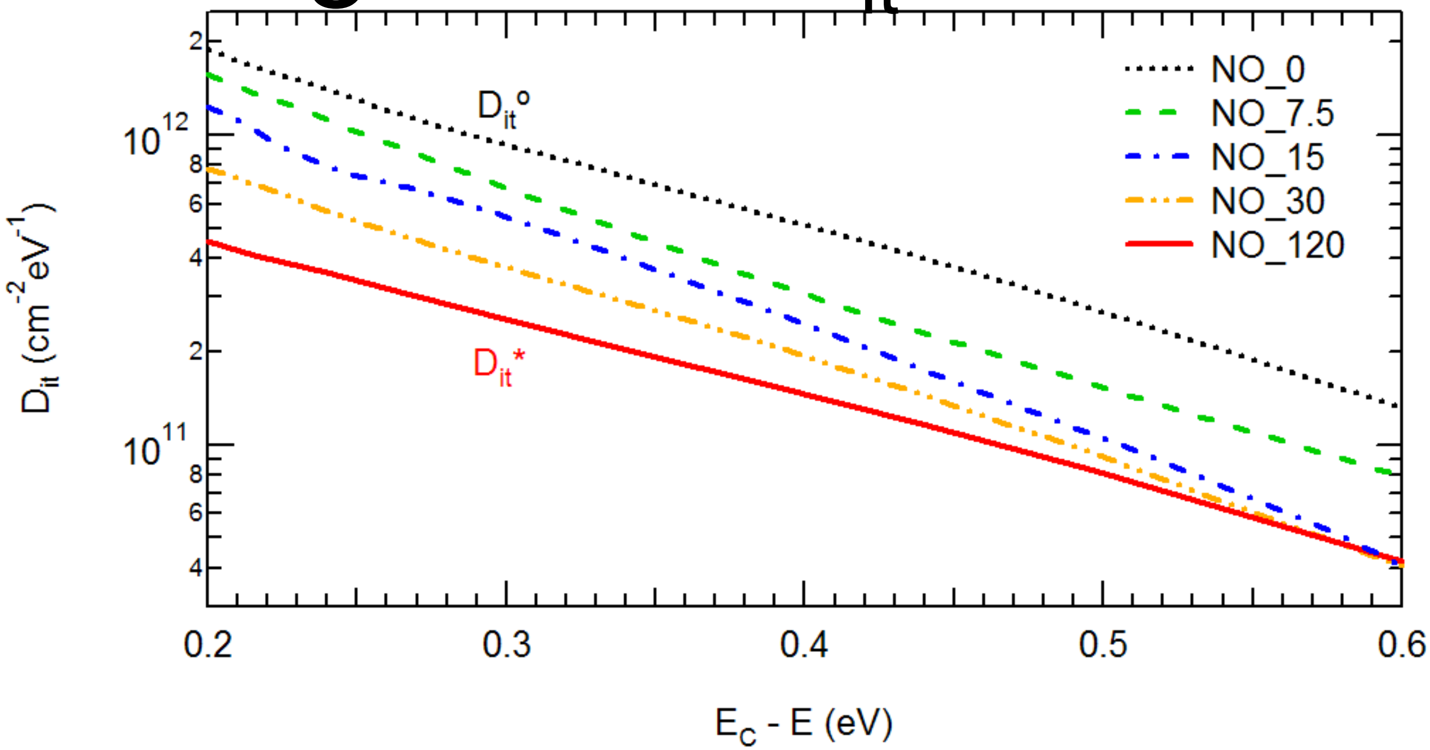
# Kinetics of the nitrogen uptake

Integrated Nitrogen density




→ How does trapping scales with N density ?

# Progressive $D_{it}$ reduction



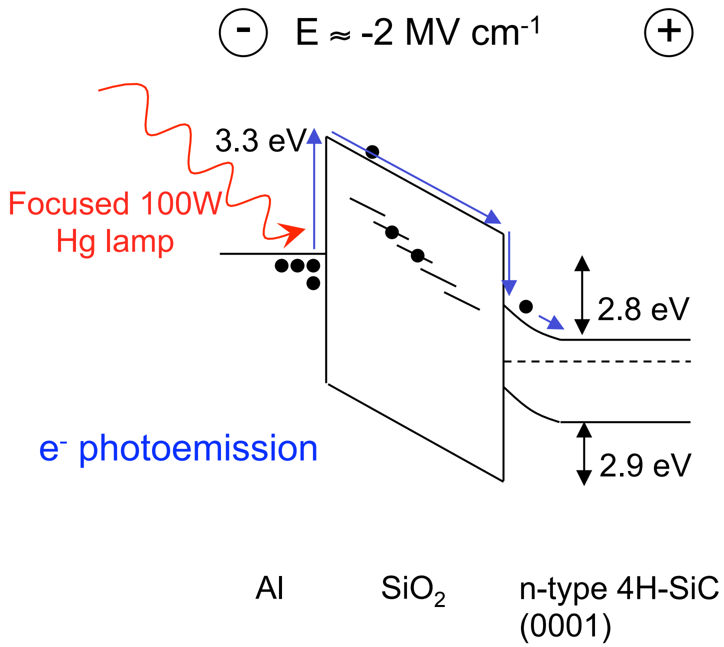

→ **NO annealing reduces *$D_{it}$* by an order of magnitude close to $E_c$**

→ It leads to a tenfold increase in MOSFET channel mobility

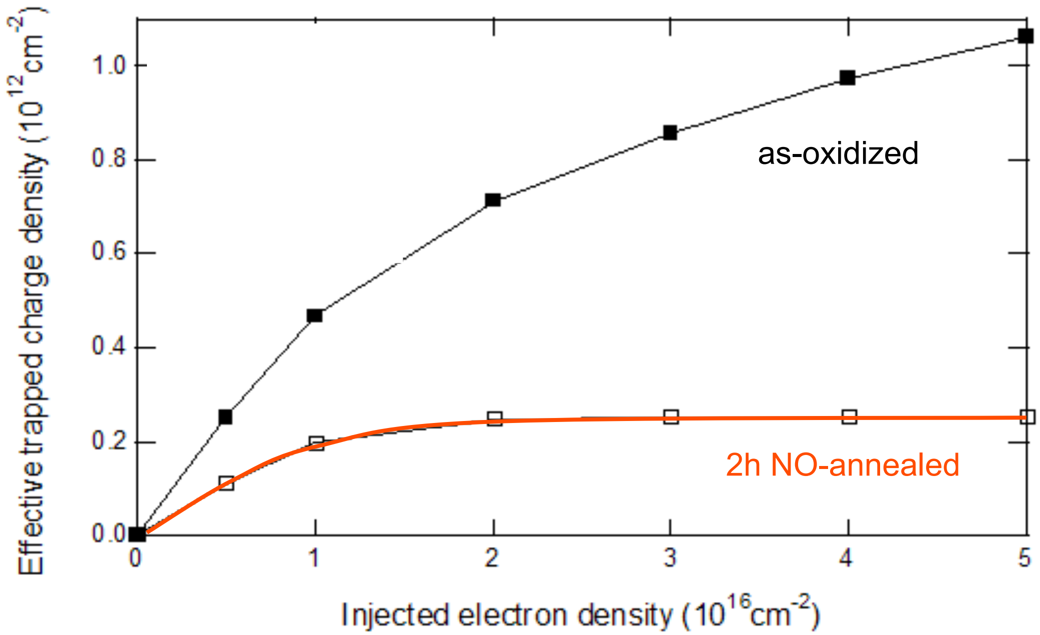
Before NO $\mu_{INT} \approx 5$ cm$^2$ / V.s

After NO $\mu_{INT} \approx 50$ cm$^2$ / V.s

# Electron trapping




Electron trap density



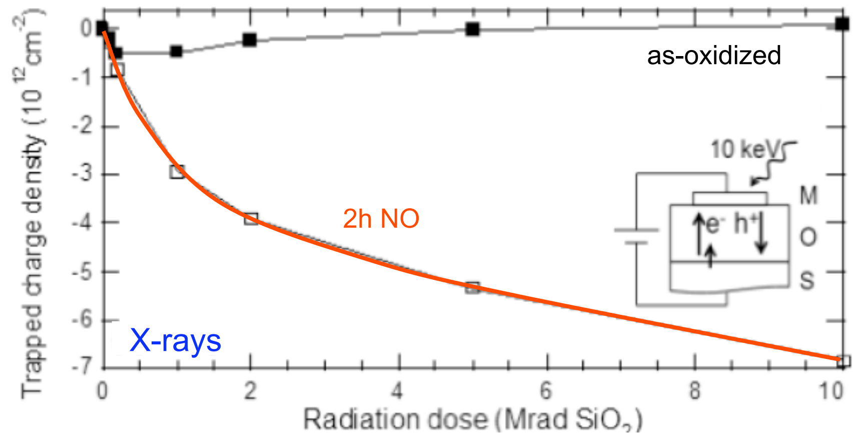

→ Reduced negative charge buildup in nitrided samples

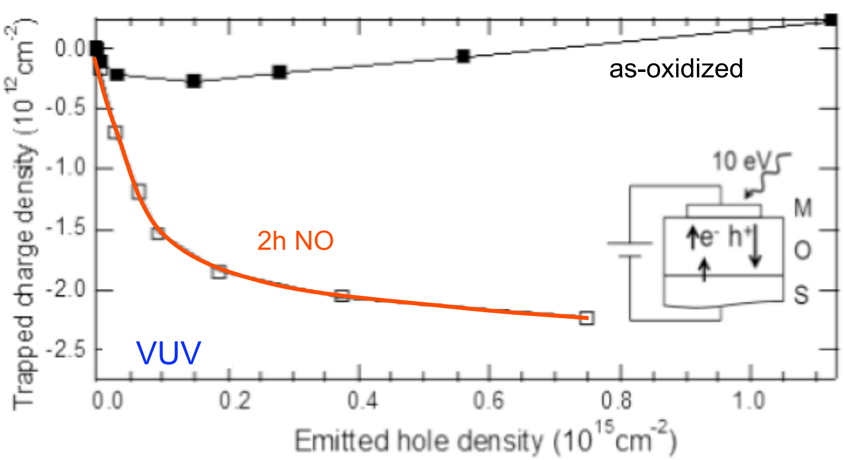
→ NO annealing suppresses generation of acceptor states at the interface

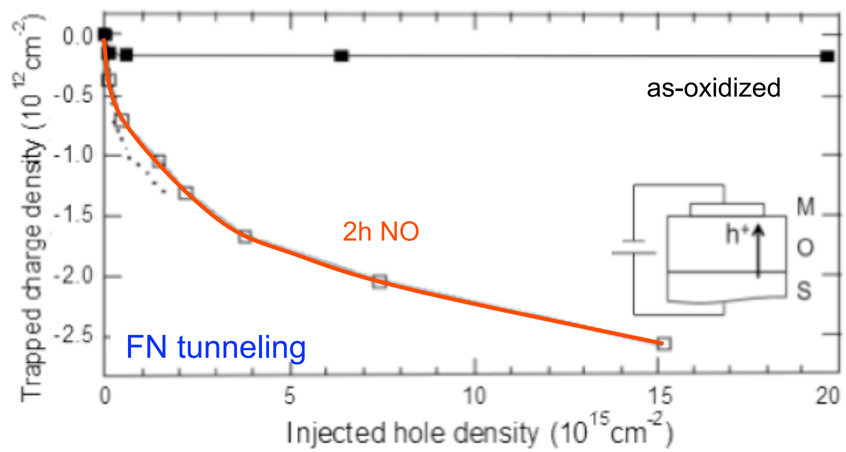
# Hole trapping

NO anneal dramatically increases hole trapping

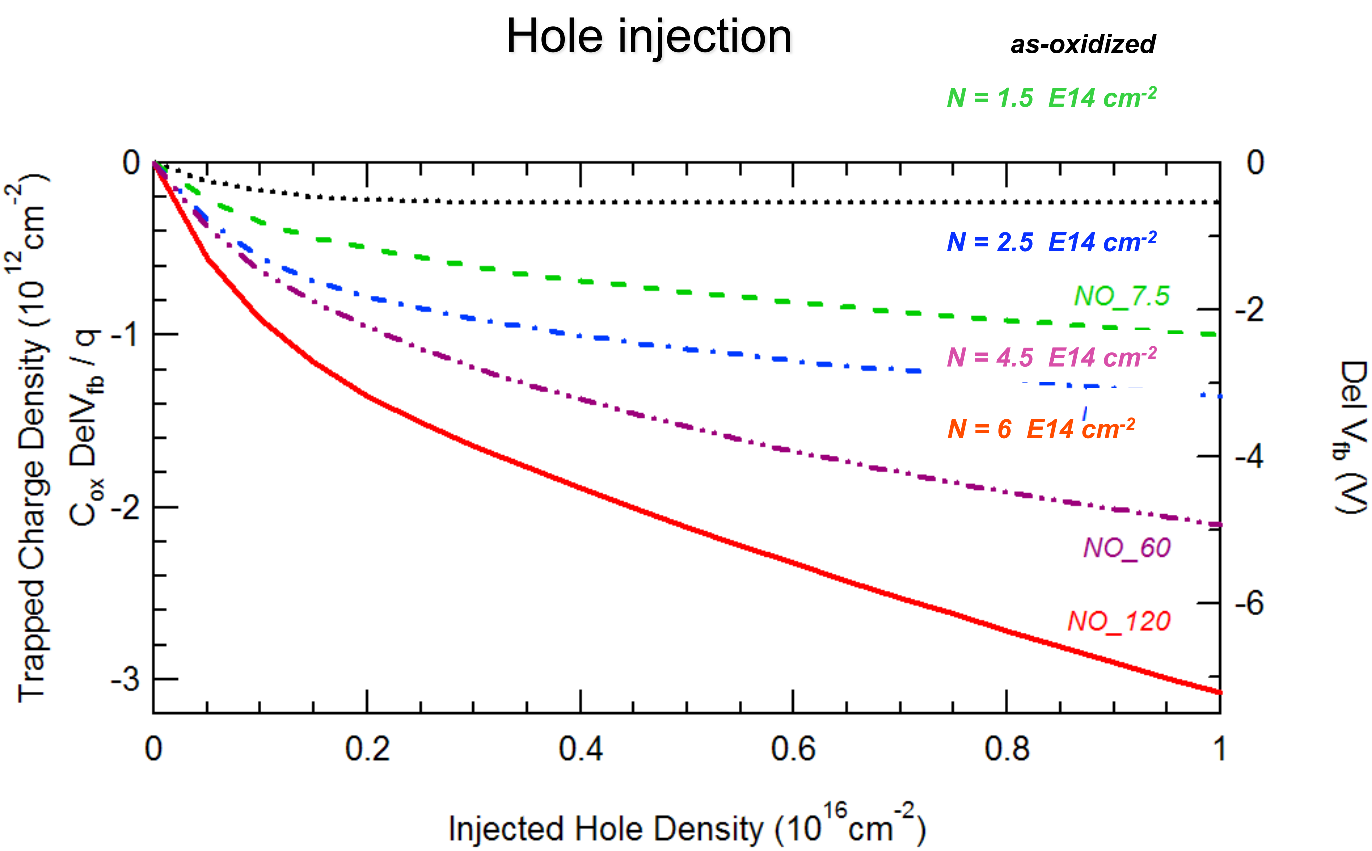
Drawback of the nitridation



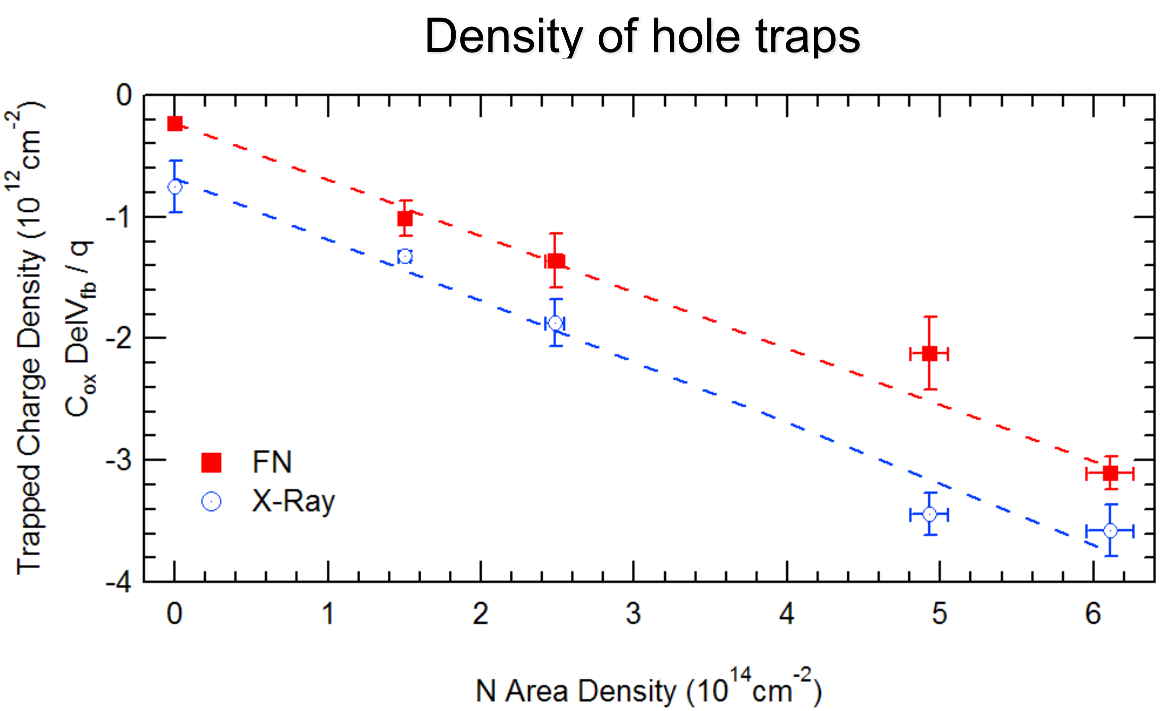



# Hole trapping scaling with N content



# Hole trapping scaling with N content




→ Hole traps are directly related to nitrogen incorporation

→ The standard NO annealing process needs to be optimized

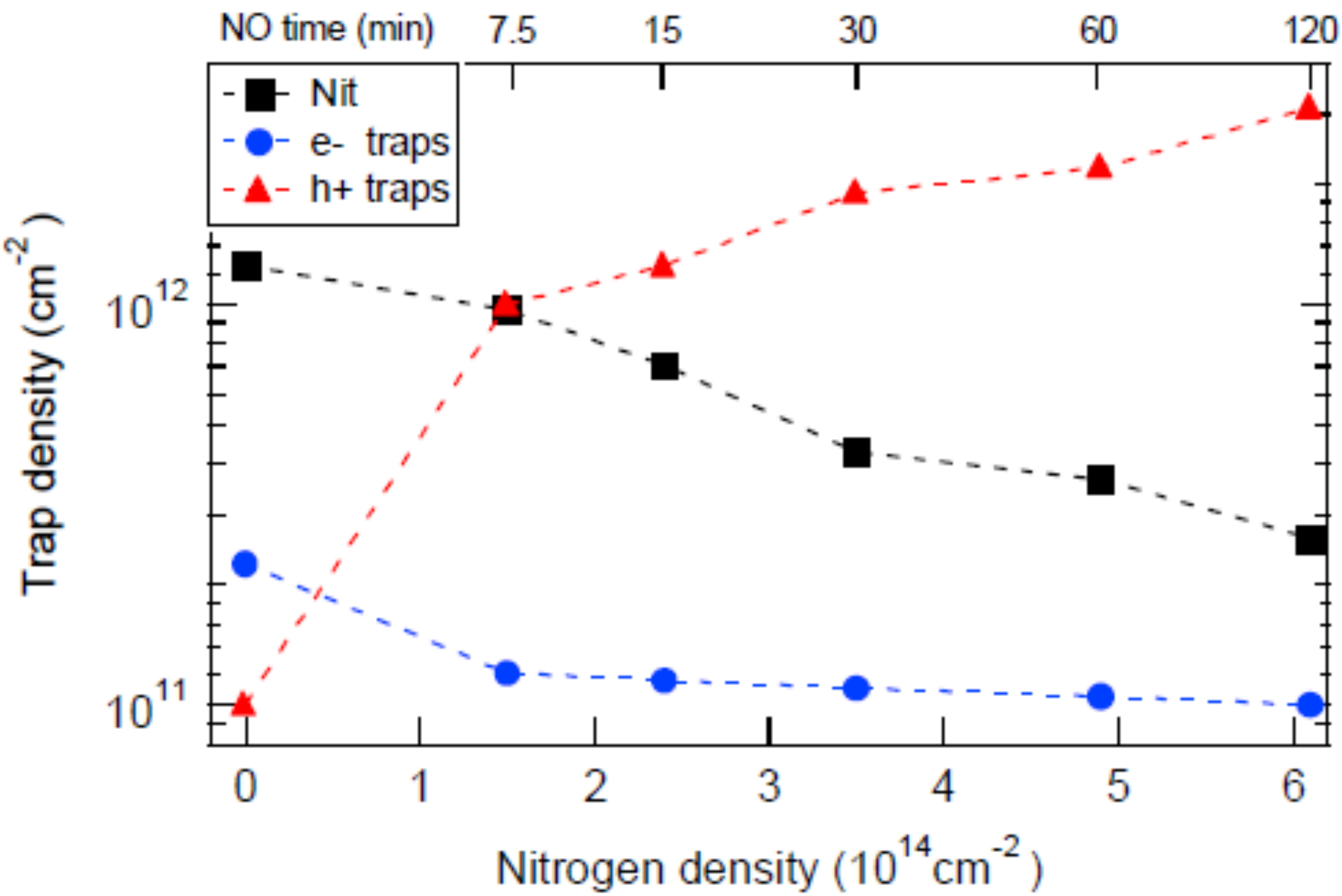



Fig. 1: Various trap densities vs N content

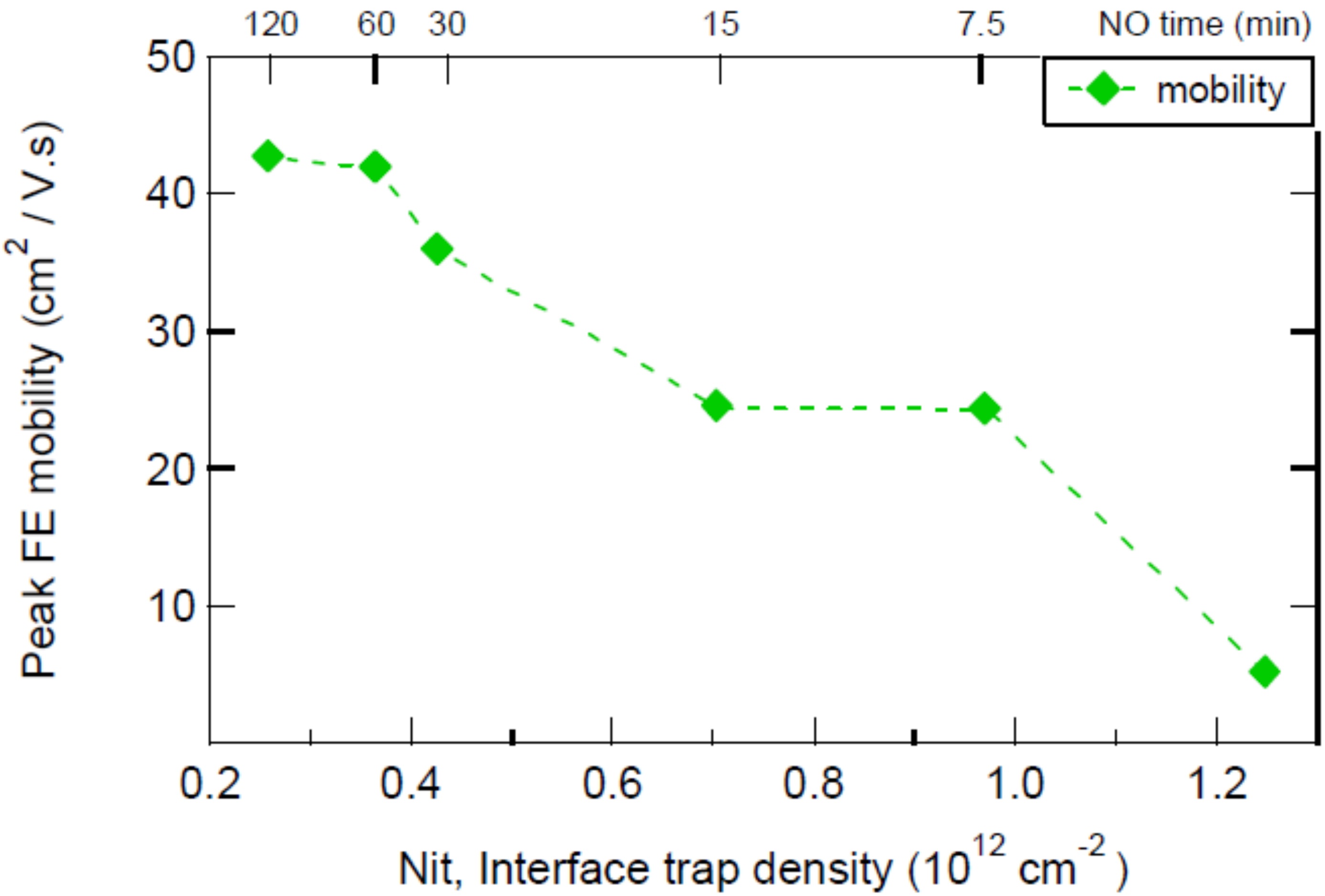



Fig. 4: Peak FE mobility vs charged $D_{it}$

# The oxide near-interface region

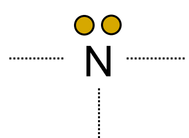
**What is the nature of the hole trap?**

In Si technology: hole trap = E’ center
(oxygen vacancy)

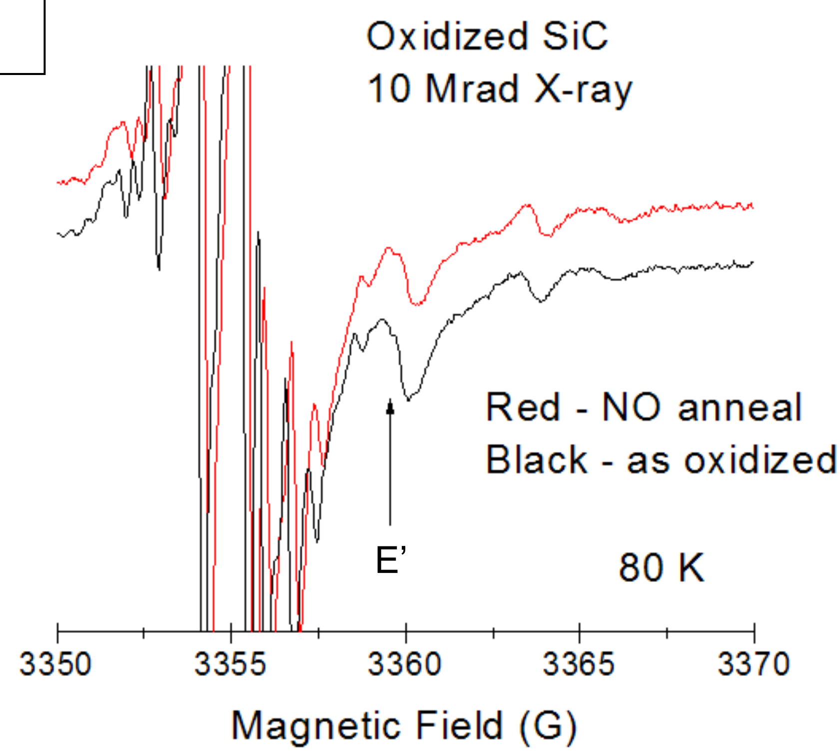
- ESR measurements

→ NO annealing does not increase the density of E’ precursors

→ Enhanced trapping has another origin



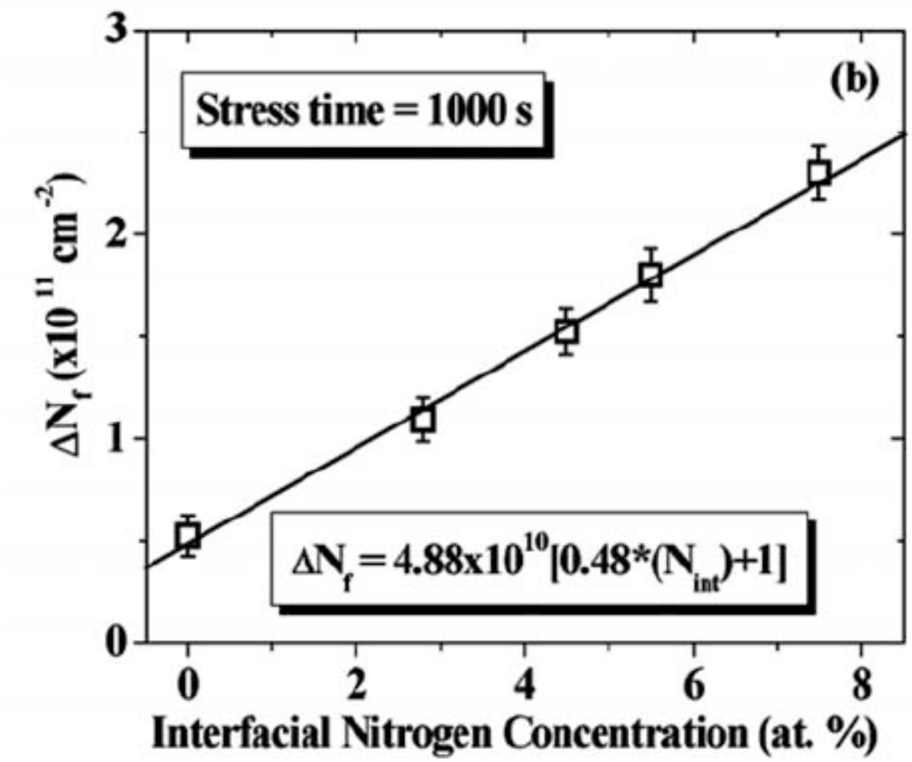

*The Nitrogen lone electron pair…*




Courtesy of M. E. Zvanut
*University of Alabama at Birmingham*

# The oxide near-interface region

… N-induced NBTI is well known in $SiO_2$ on Si !!!




The oxide hole trap density scales linearly with the nitrogen content after NO annealing both on both Si and SiC.

Tan *et al.*
Microelectron. Reliab. **45** (2005)

Like on SiC, hole traps are not E' centers

Charged defects recently identified as charged Si backboned to N as in $Si_3N_4$

Penn State group: Campbell *et al.* J. Appl. Phys. **103** (2008)

# Conclusions

✓ N reduces $D_{it}$

✓ N suppresses electron-induced interface state generation

The nitrogen incorporation needs to be optimized

✗ The hole trap density scales with the amount of incorporated N

…Next experiment: correlate $D_{it}$ and mobility by varying N

# Remaining Issues in SiC/$SiO_2$ Interfaces for Power Mosfets

1. Sub-surface stoichiometry---Si:C regions non-stoichiometry

2. Nitridation without oxidation-plasma processes

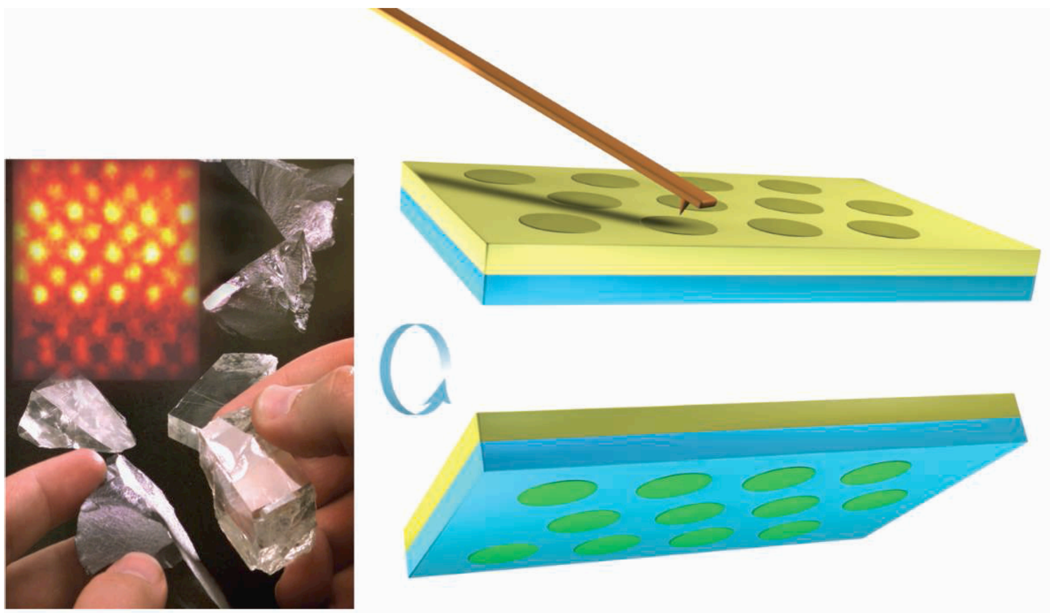
3. Effects of alkalai ions– Na improves mobility, immobilization

4. Beyond nitrogen ?

# Atomically Engineered Oxide Interfaces

J. W. Reiner, F. J. Walker, C. H. Ahn

SCIENCE PERSPECTIVE------Feb. 2009;    Reiner et al.



Researchers are using composite oxide materials structures to address numerous applications, including environmental energy harvesting, thermoelectric energy conversion, nonvolatile memory devices, chemical sensors, and more densely integrated logic circuits.Many of the electronics applications will benefit greatly from creating complex crystalline oxide structures directly on silicon (11) (see the figure, panel A), making it possible
to combine all these applications on a single silicon-based chip.

# Some Recent

# SCIENCE & NATURE Articles

**Oxide Nano-electronics on Demand--- Feb. 2009-Science— $LaAlO_3/SrTiO_3$**

**Enhancement of Ferroelectricity at Metal-Oxide Interfaces----May, 2009—Nature- -$PbTiO_3$**

**A Ferroelectric Oxide Made Directly on Silicon—April, 2009-Science— $SrTiO_3$**

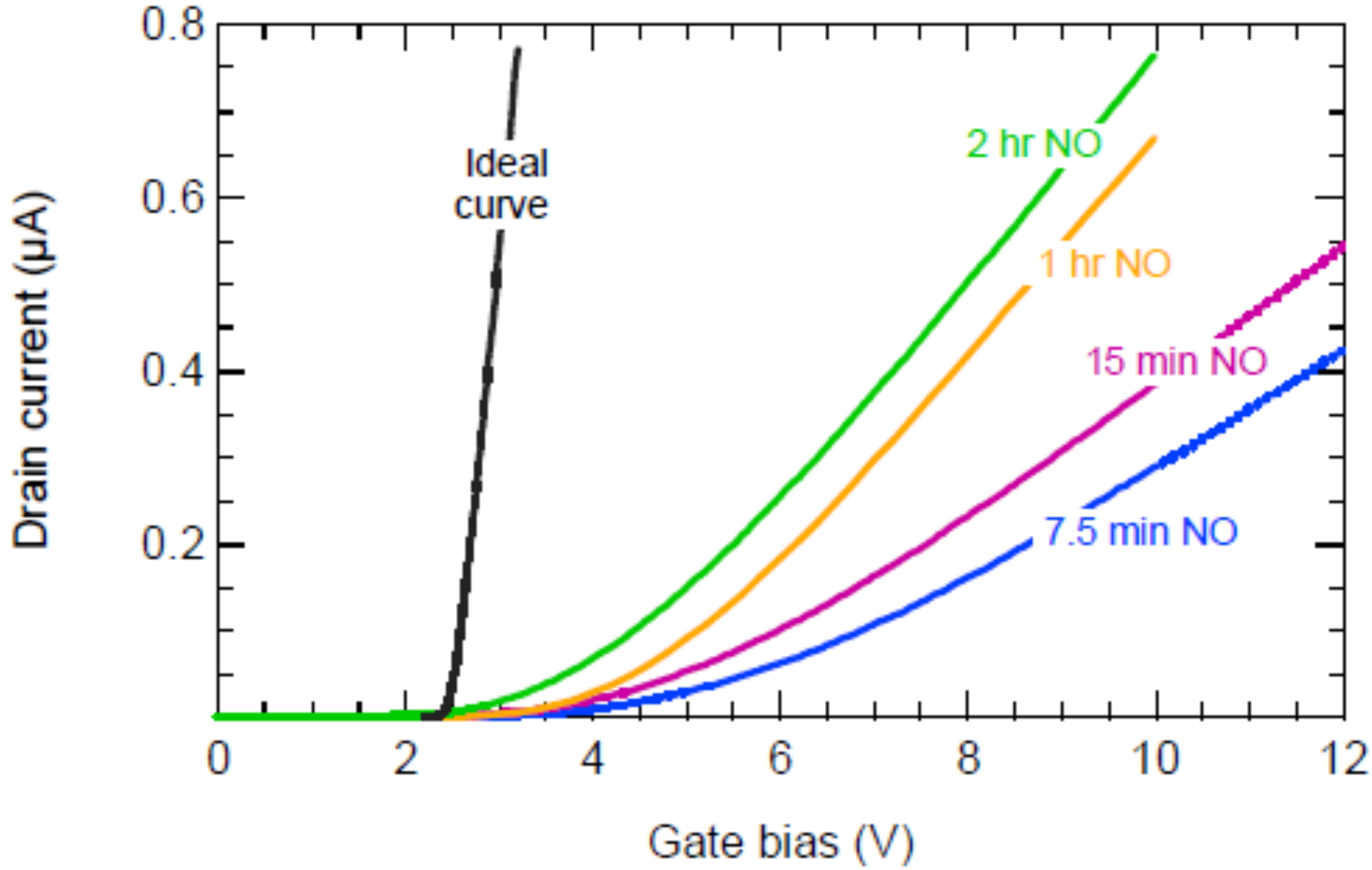
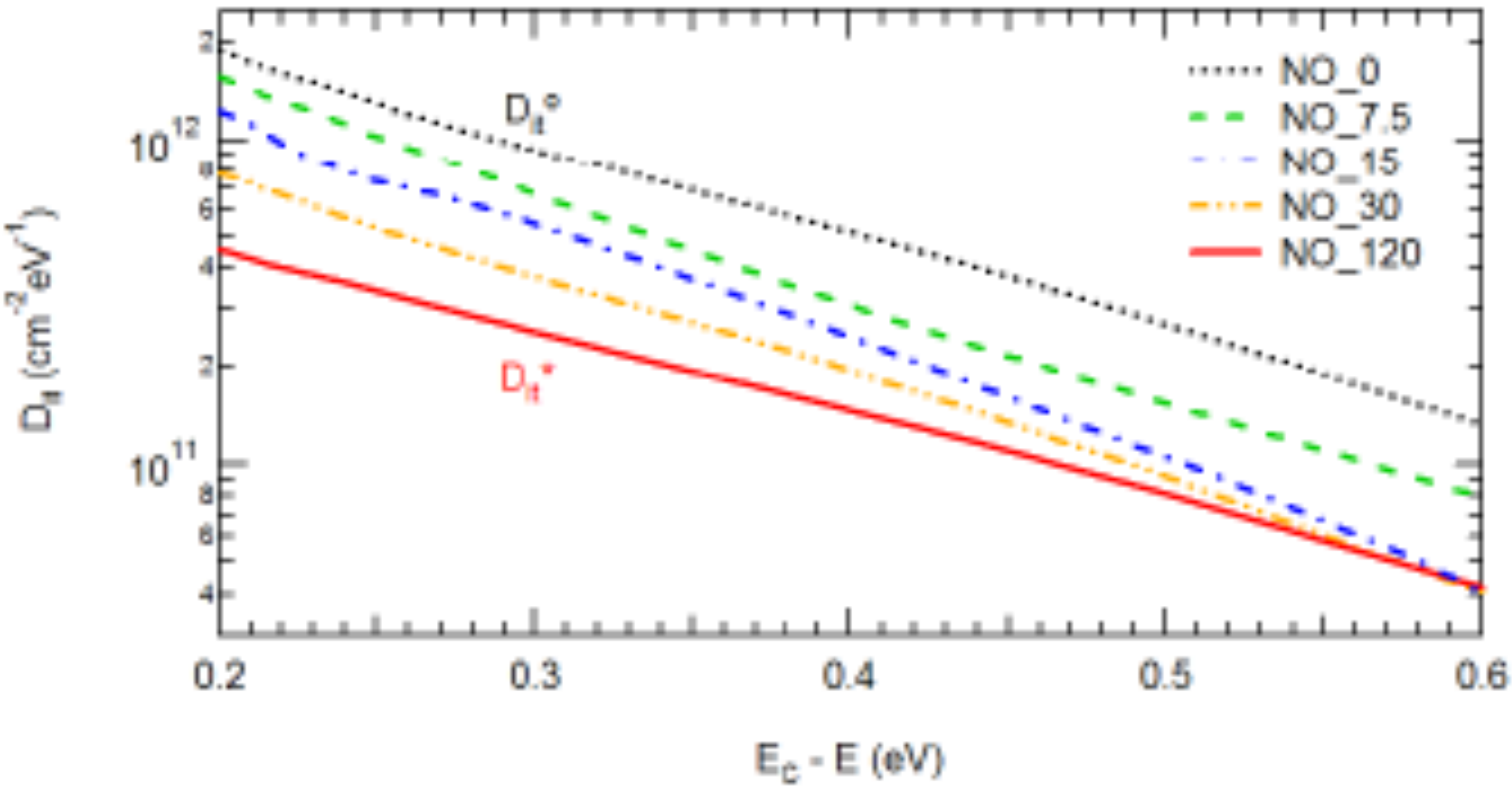


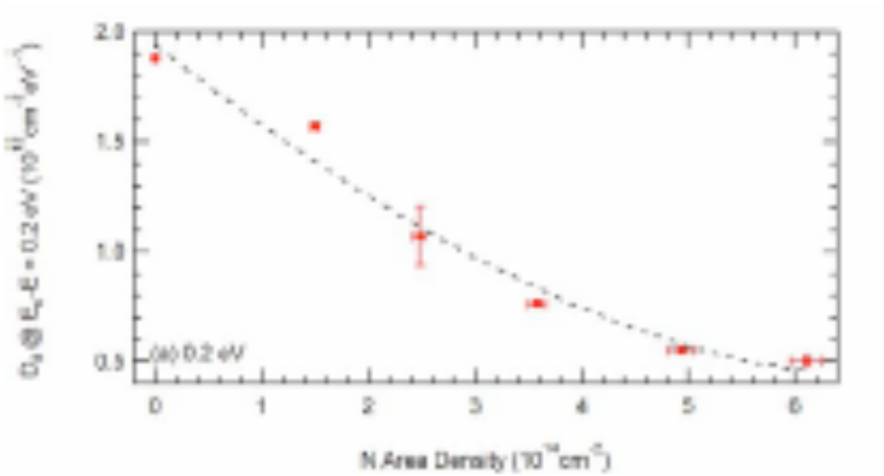

Fig. 3: Measured MOSFET characteristics

# Interface States vs. Nitrogen Content

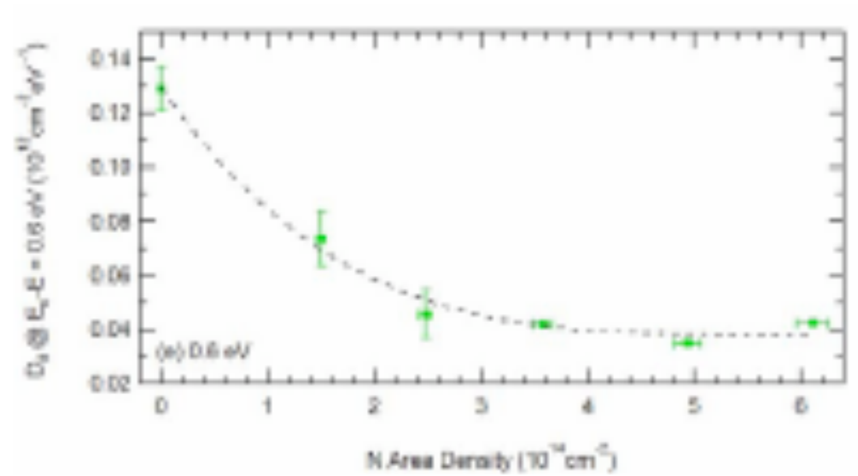


# Dit vs. Absolute N Content Near Ec and Ec-E=0.6eV

$D_{it}$ @ $E_c$-E = 0.2 eV




$D_{it}$ @ $E_c$-E = 0.6 eV




→ Deep states have a higher passivation cross-section than shallow states