

# **Total-Dose Effects on MSDRAMs**

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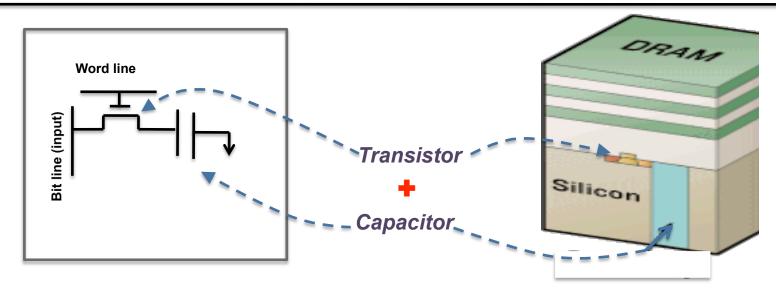


### **OUTLINE**

- ♦ Motivation
- ♦ ZRAM / MSDRAMs
- ♦ MSDRAM operations
- ♦ Total ionizing dose (TID) effects on MSDRAM
  - → TID effects on the memory window
  - → Retention time response to TID
  - → Impact of TID on the state "1"
- ♦ Conclusion



### **MOTIVATION**



- → The difficulty of the capacitor miniaturization in DRAM memory cells prevents the scaling of DRAM cells.
- → Capacitor-less DRAM as ZRAM and MSDRAM have been successfully investigated to replace standard DRAM cells.



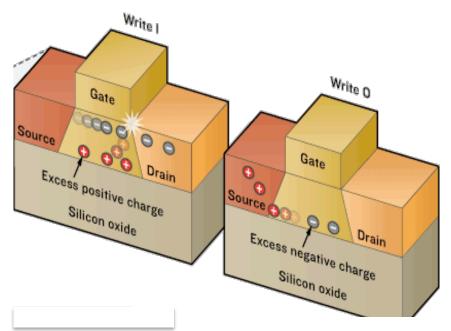
In this work we focus on investigating the TID effects on MSDRAM cells



## ZRAM

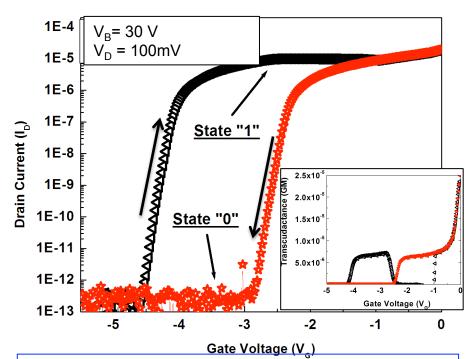
### VS.

# **MSDRAM**



http://spectrum.ieee.org/images/jan07/images/wsemif1.gif

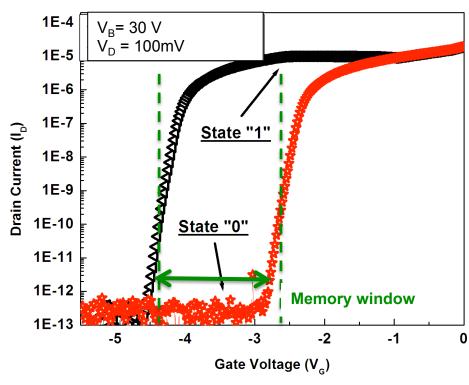
- ♦ Impact ionization is the primary mechanism in ZRAM operation.
- ♦ At the state "1": the drain current is high.
- ♦ At the state "0": the drain current is low.



- ♦ MSDRAMs rely on the MSD effect.
- ♦ At the state "1": the drain current is ON
- ♦ At the state "0": the drain current is OFF.



# **MSDRAMs OPERATION (1/2)**



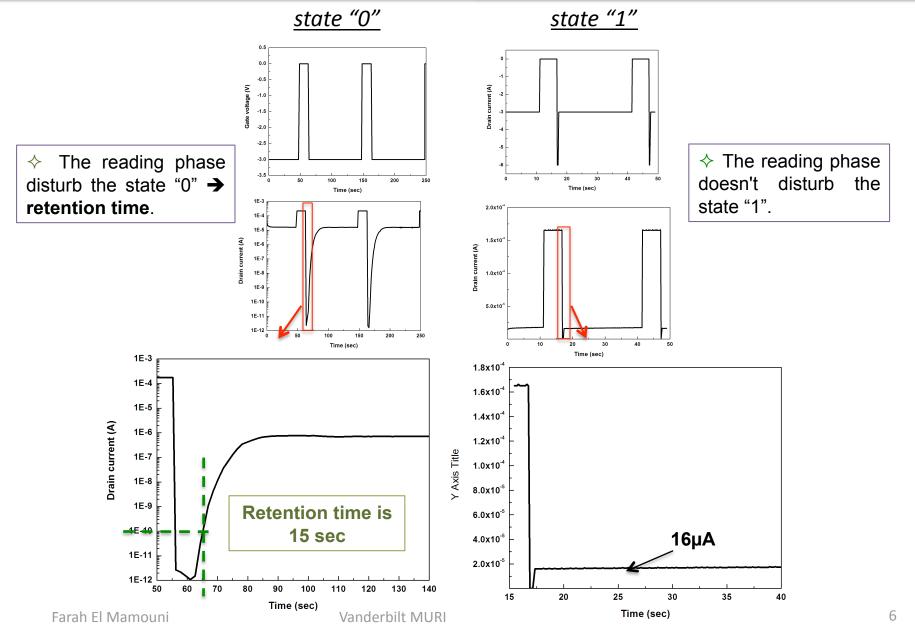
- ♦ For memory application, the MSDRAM should be operated in the memory window. i.e.,  $V_G$ =(-3 V,-4.5 V),  $V_{BG}$ =30 V,  $V_D$ =100m V and  $V_S$ =0 V.
- → The hysteresis measurements define the reading and programming voltages of the MSDRAM.

#### Example:

A gate voltage of -3 V is the minimum reading voltage for the state "0" and "1".



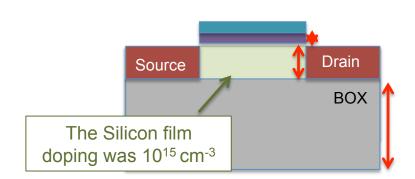
# **MSDRAM OPERATION (2/2)**



# TID EFFECTS ON MSDRAM

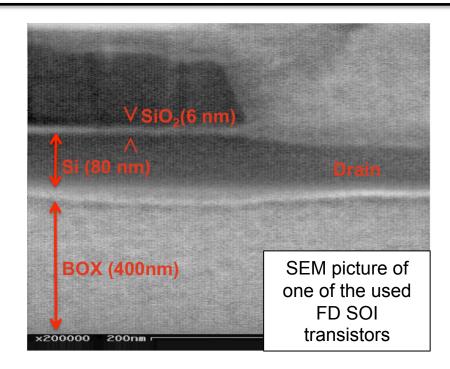


### **DEVICE AND MESEARMENT DETAILS**



- ➤ Total of 8 devices were investigated in this work.
- Devices with gate width and length of 300x300 μA were used to study the MSD response to TID effects.
- $\triangleright$  Devices with gate width and length of 100x25  $\mu$ A were used to investigate the retention time of irradiated MSDRAM.

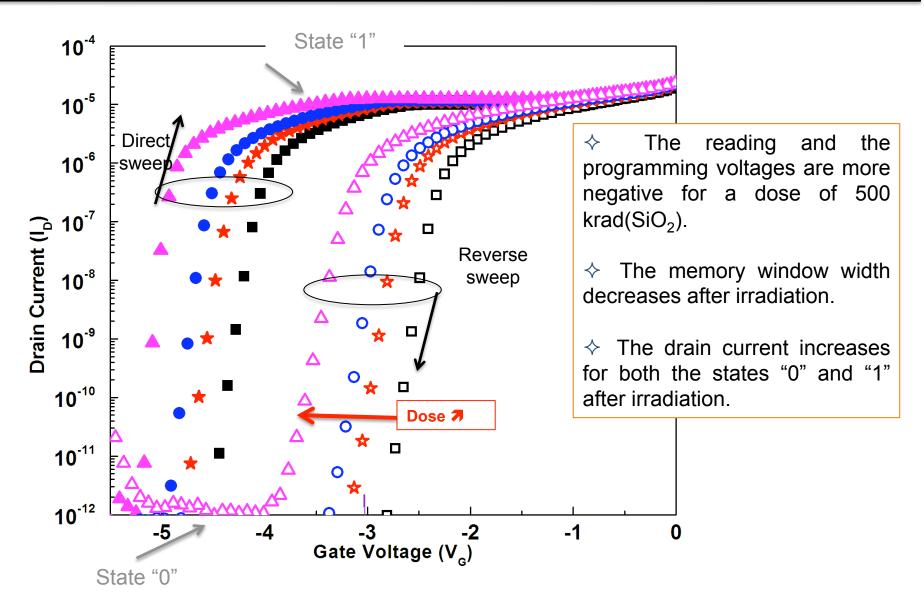
During all the pre- and post-rad measurements the drain bias was **100 mV**.



➤ The MSDRAM cells were irradiated with a drain voltage of 2.5 V, a floating body and all other terminal grounded.

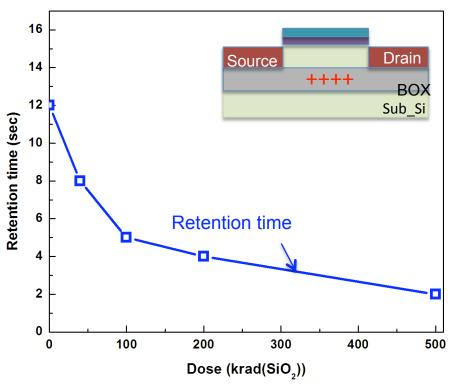


# TID EFFECTS ON THE MEMORY WINDOW OF IRRADIATED MSDRAM





### RETENTION TIME RESPONSE TO TID EFFECTS

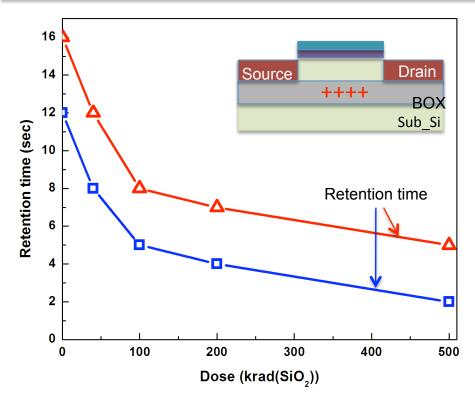


♦ After irradiation, positive charge is trapped in the BOX. It is harder to maintain the silicon film fully depleted. The state "0" is disturbed.

➤ Blue curve: the back gate was biased at 20 V and the reading voltage was -3 V.

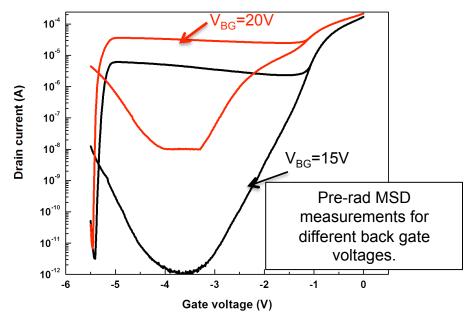


### RETENTION TIME RESPONSE TO TID EFFECTS



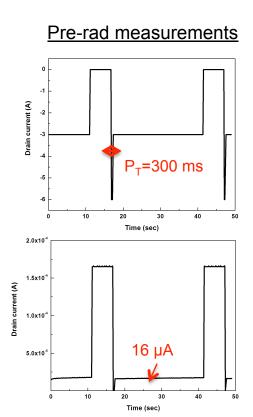
- ➤ Blue curve: the back gate was biased at 20 V and the reading voltage was -3 V.
- ➤ Red curve: the back gate was biased at 15 V and the reading voltage was -3 V.

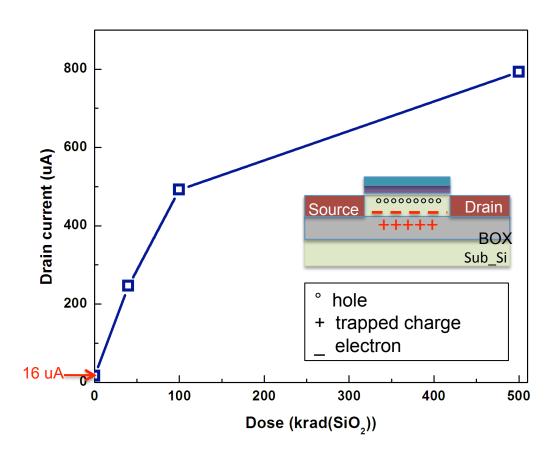
♦ An MSDRAM cell programmed with a lower back gate shows higher retention times before and after irradiation. It is easier to turn off the back side channel for lower V<sub>BG</sub>.





### TID RESPONSE OF THE STATE "1" IN IRRADATED MSDRAM





♦ The drain current at the state "1" increases for increasing dose. After irradiation, the trapped charge in the BOX, decreases the back gate threshold voltage and increases the drain current.



### CONCLUSION

- The memory window of irradiated MSDRAMs shifts toward more negative front gate voltages. This modifies the programming and the reading voltages with increasing dose.
- The memory window of irradiated MSDRAMs tends to shrink with dose, but for some devices, the memory effect is maintained even at a dose of 500 krad(SiO<sub>2</sub>).
- ➤ The retention time decreases with increasing dose in irradiated MSDRAM. This can be compensated by decreasing the back gate voltage.
- ➤ Higher drain current were obtained while reading the state "1" after irradiation. This may maintain the difference in the current level between the state "1" and "0" in irradiated MSDRAMs.



### **FUTURE WORK**

♦ The drain current at the state "1" showed to be very sensitive to the programming time. we are trying to understand the combined effect of the programming time and the total dose on irradiated MSDRAM cells.

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