Radiation Effects in SiGe Devices

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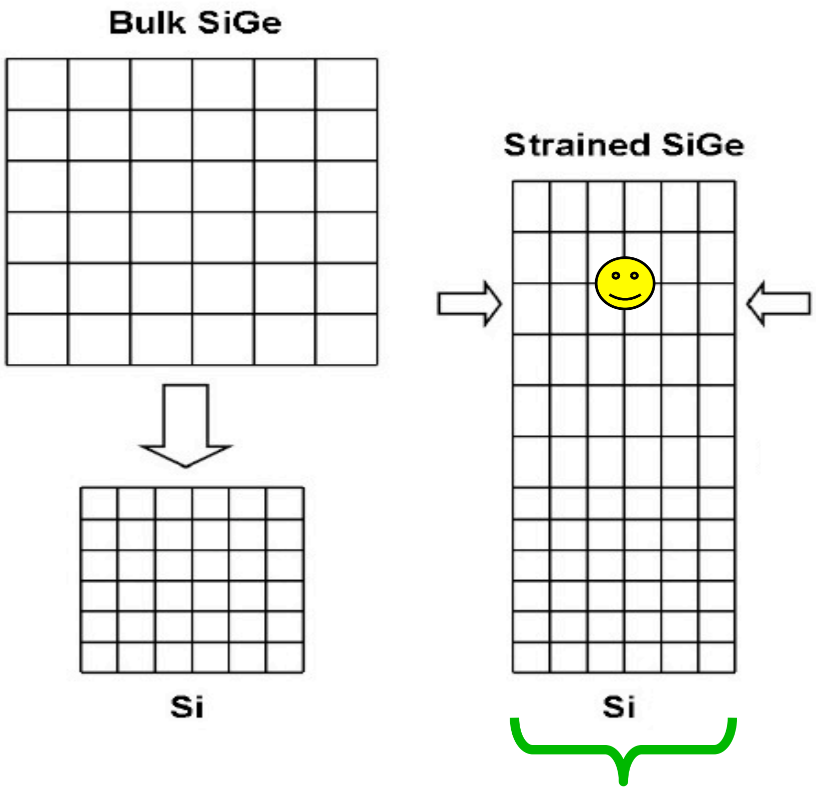
Outline

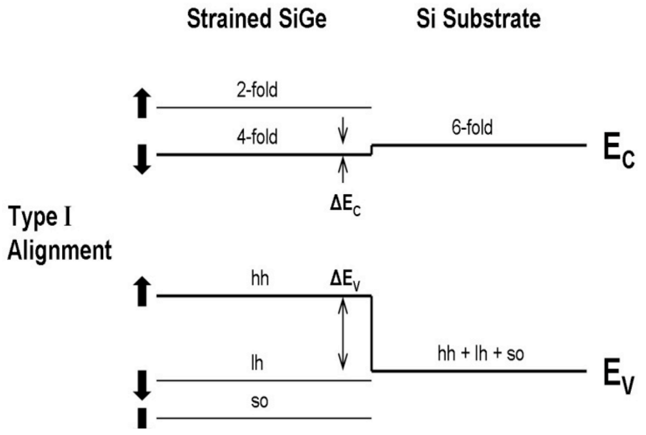
- **SiGe HBT Technology & Extreme Environment Applications**
- **Total Dose Effects on SiGe HBTs**
  - damage mechanisms, temperature dependence, scaling
- **Single Event Studies of SiGe HBTs**
  - TRIBICC vs. IBICC
- **Hardening Methodologies & 3-D Modeling**
  - “n-ring” incorporation
  - bulk vs. SOI platforms
  - inverse-mode cascode
- **Mixed-mode Modeling and Circuit Exposures**
  - BGR measurements
- **Progress & Plans**

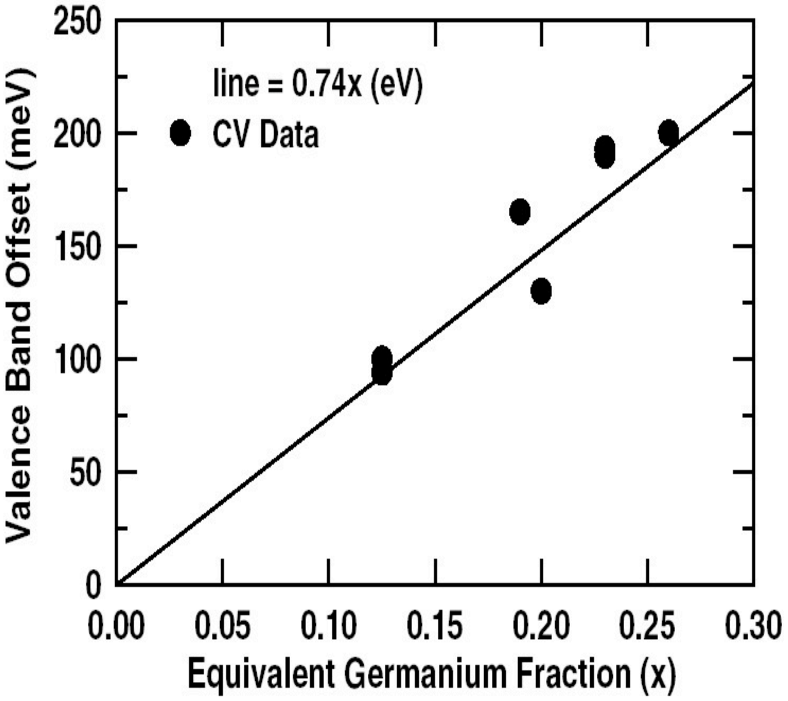
SiGe Strain Engineering

The Bright Idea!

Practice Bandgap Engineering
… but do it in Silicon!

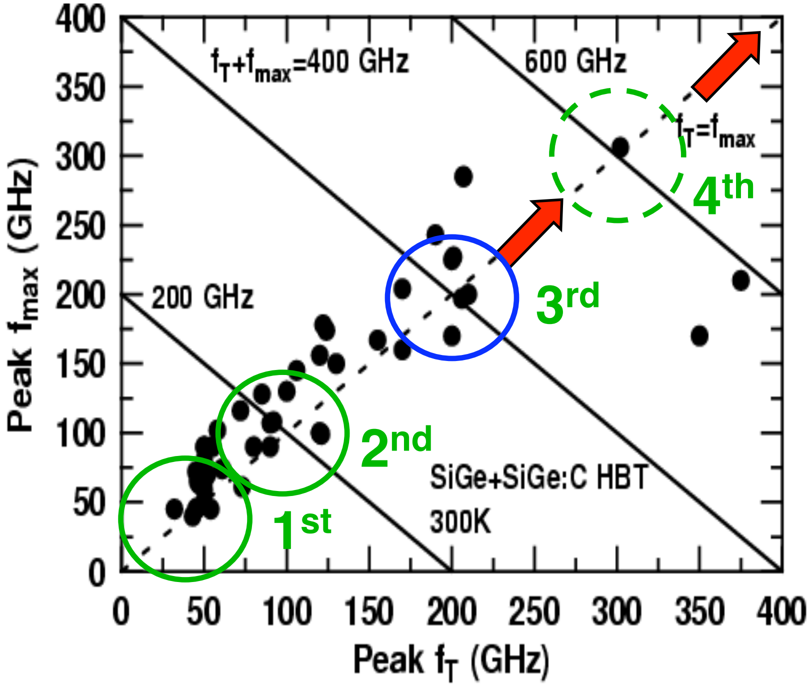


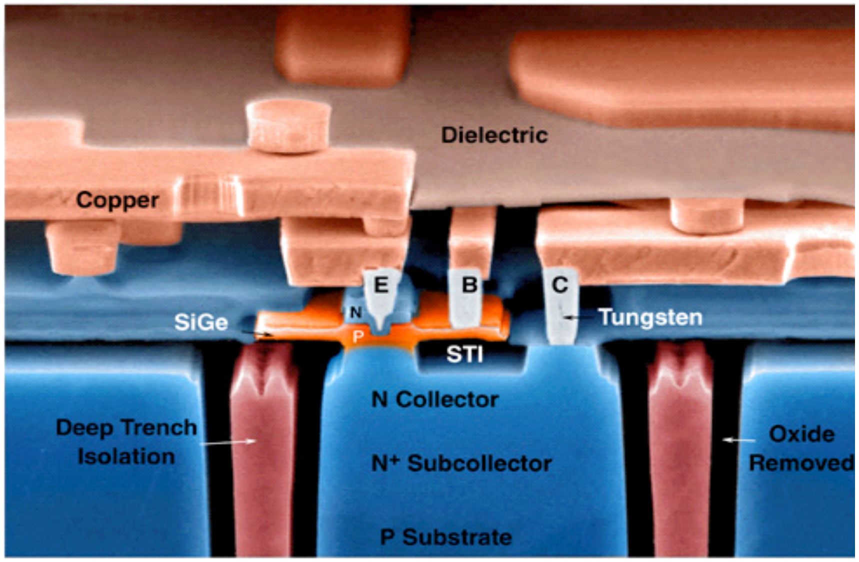


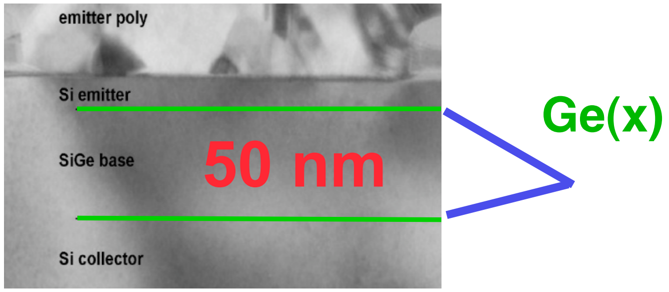


SiGe Success Story

- **Unconditionally Stable, UHV/CVD SiGe Epitaxial Base**
- **SiGe = SiGe HBT + Si CMOS for Highly Integrated Solutions**
- **100% Si Manufacturing Compatibility**
- **Rapid Generation Evolution Incorporating C-SiGe Processes**







SiGe = III-V Speed + Si Manufacturing

Win-Win!

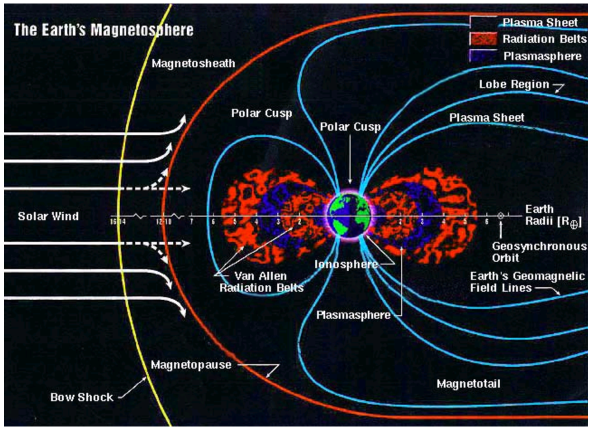
Growing Opportunities

- SiGe Radar Systems
  - **defense radar systems + automotive radar** (e.g., @ 10 GHz, 77 GHz)
  - **automotive radar** (24, 77 GHz)
- SiGe for Millimeter-wave Communications
  - **Gb/s short range wireless links** (60, 94 GHz)
  - **cognitive radio / frequency-agile WLAN / 100 Gb Ethernet**
- SiGe for THz Sensing, Imaging, and Communications
  - **imaging / radar systems, diagnostics, comm** (94 GHz, 100-300 GHz)
- SiGe for Analog Applications
  - **the emerging role of C-SiGe** (npn + pnp) + **data conversion** (ADC limits)
- SiGe for Extreme Environments
  - **extreme temperature** (4K to 300C) + **radiation** (e.g. space systems)
- SiGe for Low Power Electronics
  - **biomedical applications**

EE Electronics

Space-Based Electronics

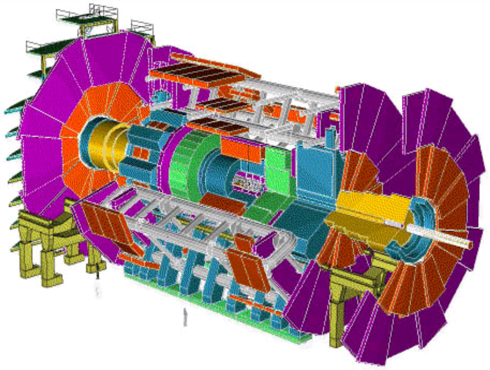
- Low-energy plasma (Van Allen)
- Galactic cosmic rays
- Solar flares
- Terrestrial cosmic rays
- Temperature -180°C to + 120°C



[1] http://see.msfc.nasa.gov/pf/pfimage/sphere8x6.jpg

High-Energy Physics Detectors

- ATLAS detector (LHC @ CERN)
- 10^9 p-p collisions/s at several TeV
- 115 days/year over 10 years
- 1 MeV neutron fluence > 10^{14} n/cm^2



[2] http://scipp.ucsc.edu/~sige/

GOAL: **On-orbit error rate reduction via mission + system design, shielding, algorithms, and *hardening by design and process***

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- **Total Dose Effects on SiGe HBTs**
  - damage mechanisms, temperature, scaling, in-beam
- Single Event Studies of SiGe HBTs
  - TRIBICC vs. IBICC
- Hardening Methodologies & 3-D Modeling
  - “n-ring” incorporation
  - bulk vs. SOI platforms
  - inverse-mode cascode
- Mixed-mode Modeling and Circuit Exposures
  - BGR measurements
- Progress & Plans

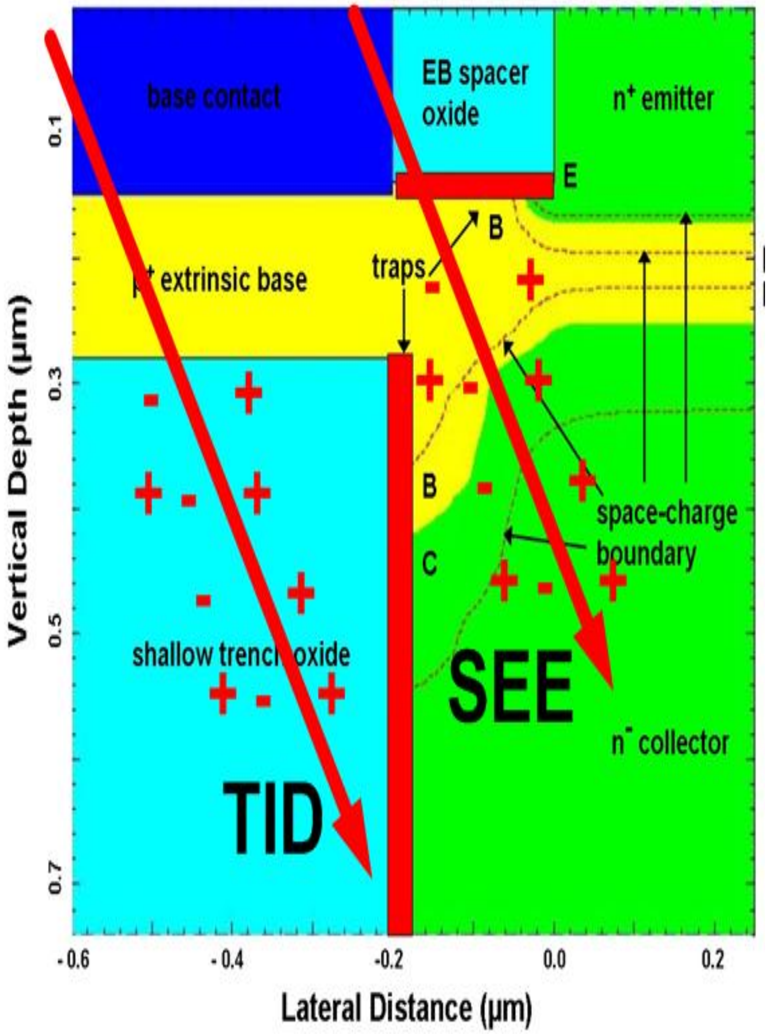
TID Damage Mechanisms

Primary Damage Source

- **Ionization Damage**
  - Charged particles + photons
  - Oxide charging + interface traps
    - EB Spacer & STI
  - FETs: V_T shifts, leakage
  - HBTs: I_B leakage, circuit bias shift

Secondary Damage Source

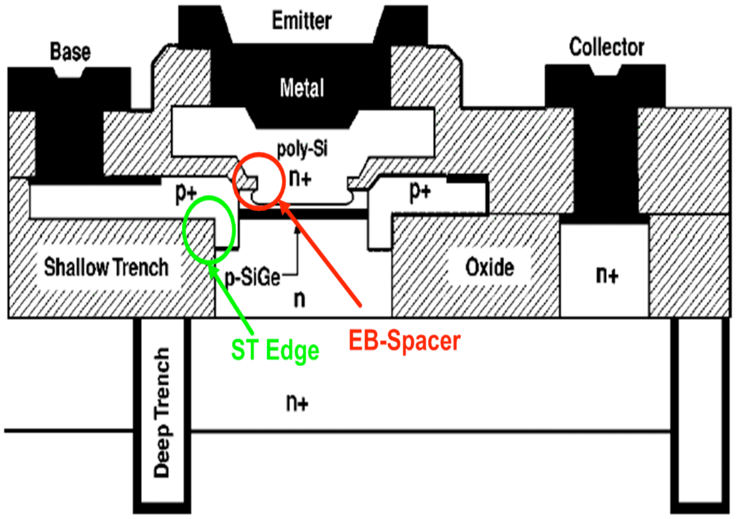
- **Displacement Damage**
  - Neutral + charged particles
  - Vacancies + interstitials
  - Dopant de-activation



IBM Technology Nodes

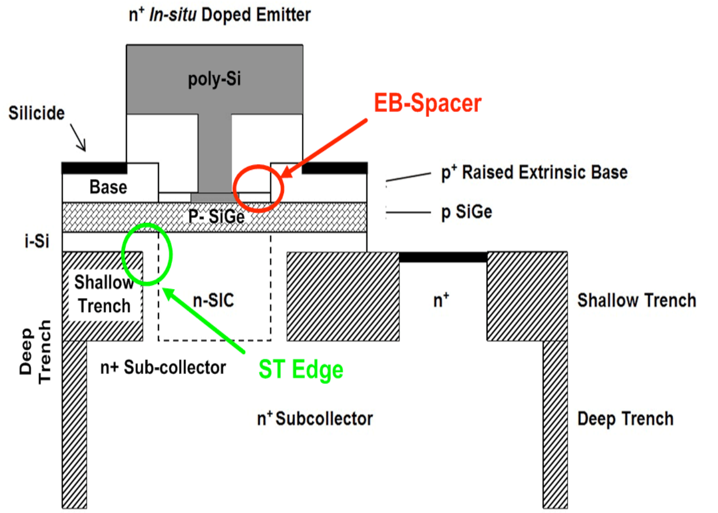
Technology Node	Peak f_T (GHz)	Peak f_{MAX} (GHz)	BV_{CEO} (V)	W_E (µm)
1st-generation (5AM)	50	70	3.3	0.5
2nd-generation (7HP)	120	100	2.5	0.2
3rd-generation (8HP)	207	285	1.7	0.12
4th-generation (9T)	350	307	1.2	0.12

5AM & 7HP



[5] D.C. Ahlgren et. al., in *Proc. IEEE BCTM* pp. 143-46, 2001.

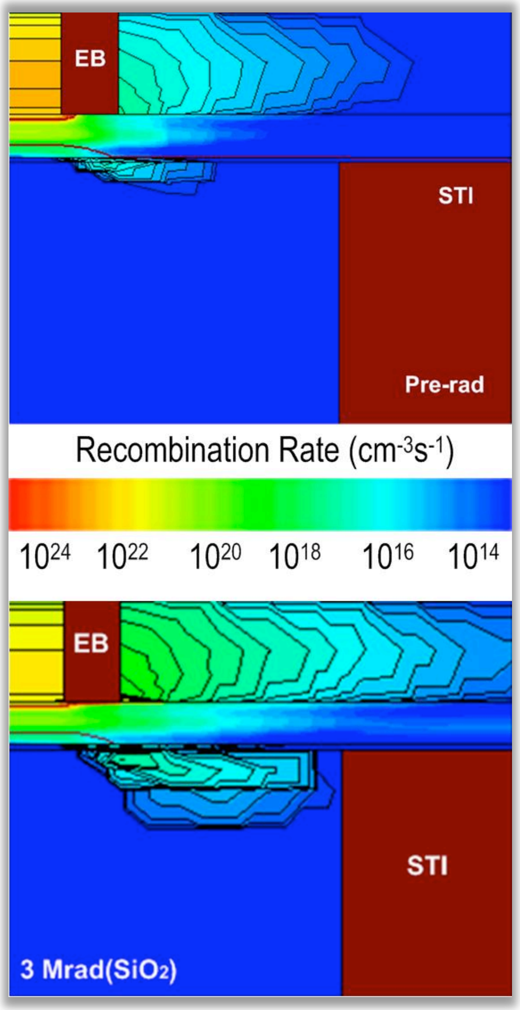
8HP & 9T

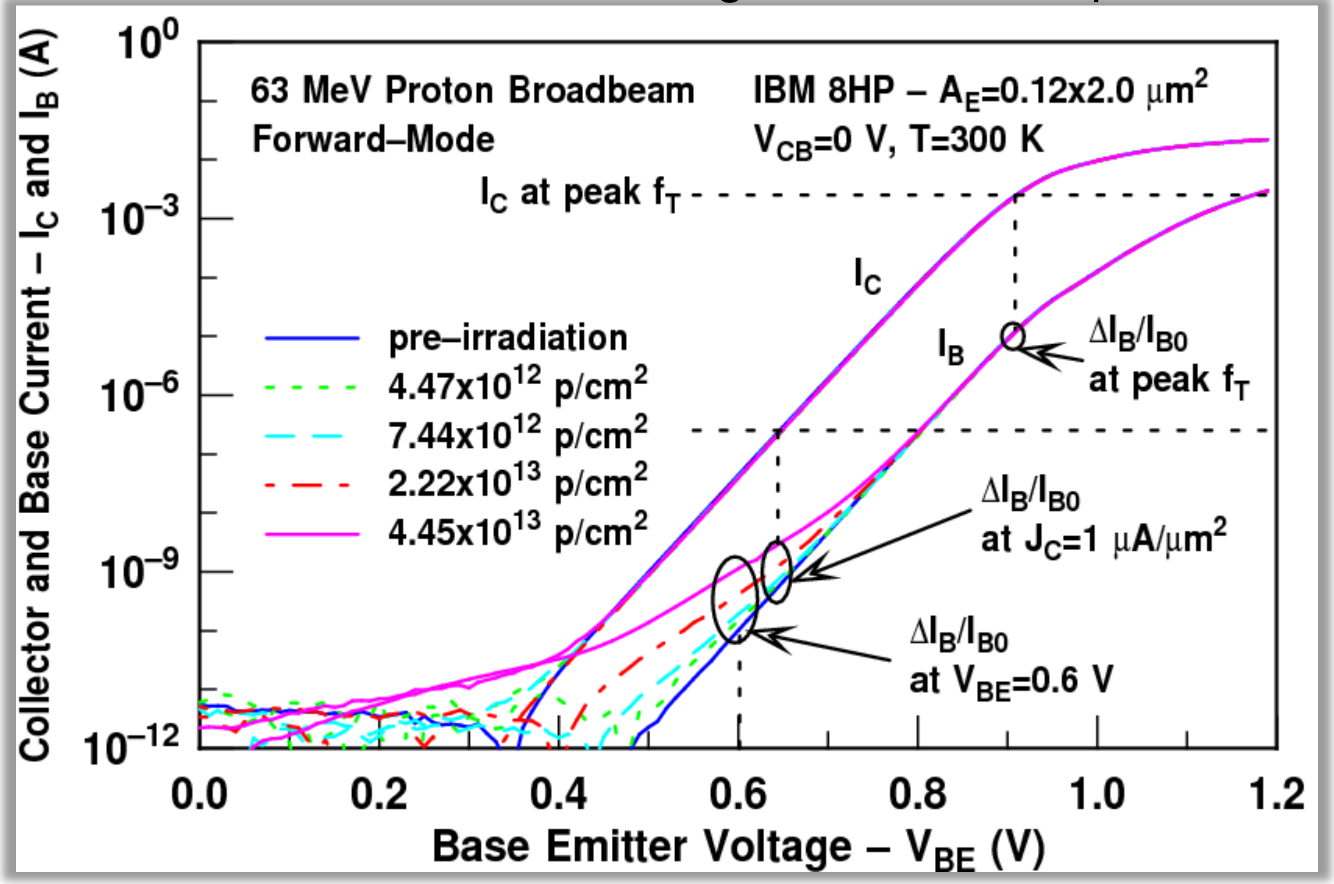


[6] B. Jagannathan et. al., IEEE EDL , vol. 23, no. 5, pp. 258-60, May 2002.

TID Damage (Forward-mode)

- G/R traps at EB-spacer → excess base current ($\Delta I_B/I_{B0}$)
- No degradation at circuit-relevant bias (J_C near peak f_T)

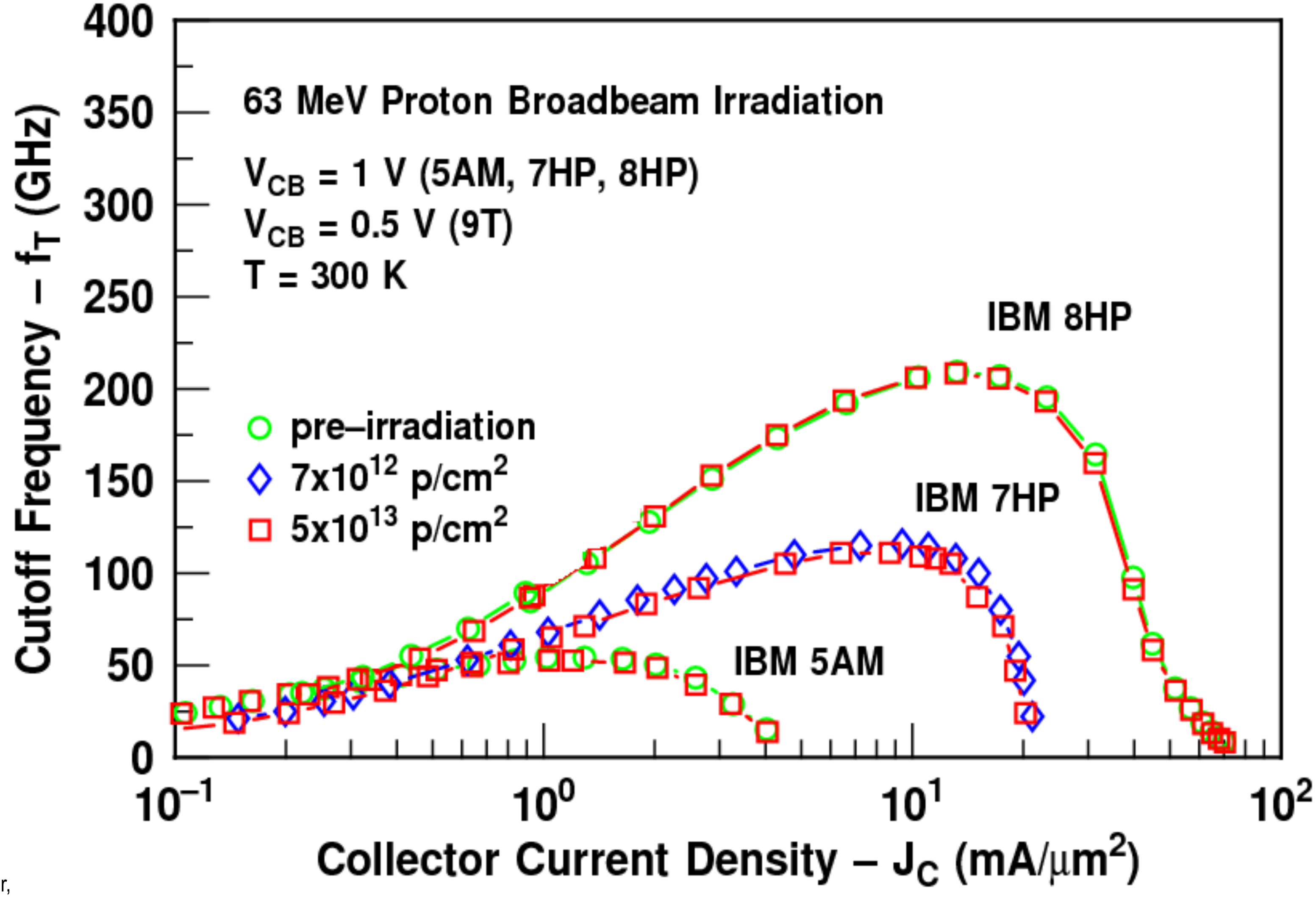




Forward-Mode $\Delta I_B/I_{B0}$ samples the EB-spacer oxide

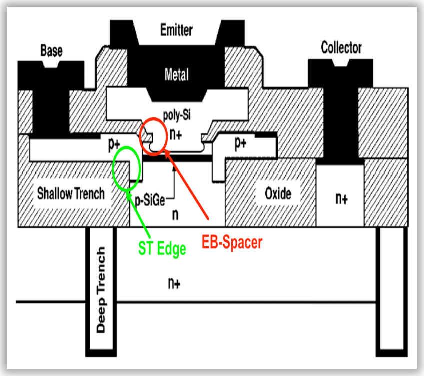
ac Performance Metrics

- No change in f_T, f_{MAX}, r_{bb}, or τ_f → lack of dopant deactivation

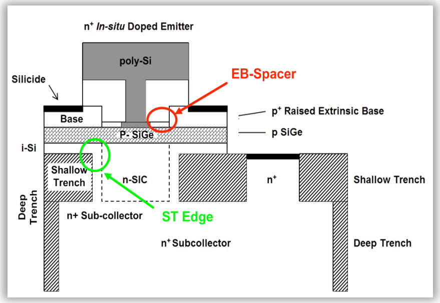


Scaling Effects

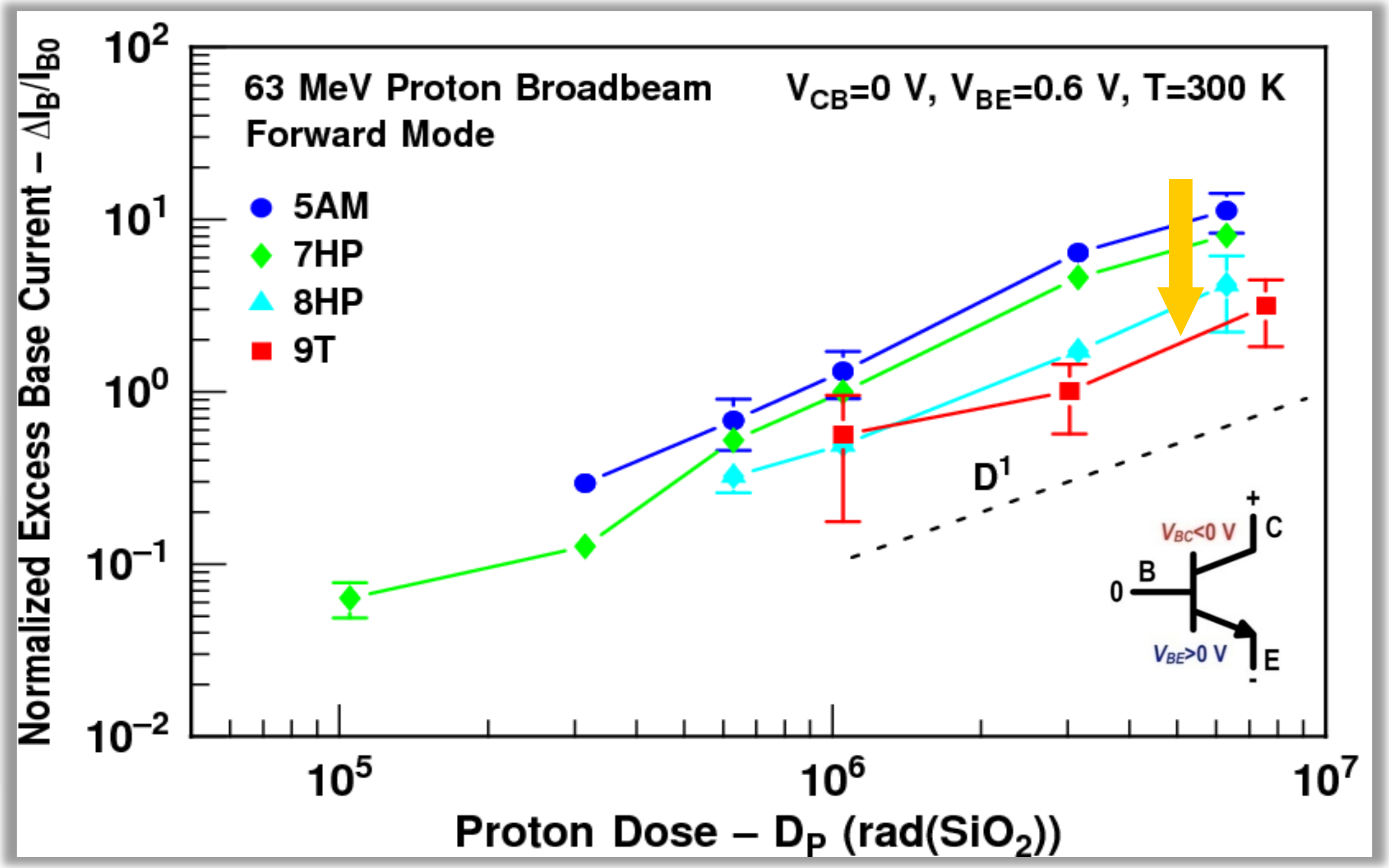
- $\Delta I_B/I_{B0}$ has a near-linear (D^1) dose dependence
- Thinner BE-spacer + raised extrinsic base → smaller $\Delta I_B/I_{B0}$
- Similar trends for $\Delta I_B/I_{B0}$ at J_C=1 μA/μm^2 and V_{BE}=0.6 V



5AM & 7HP

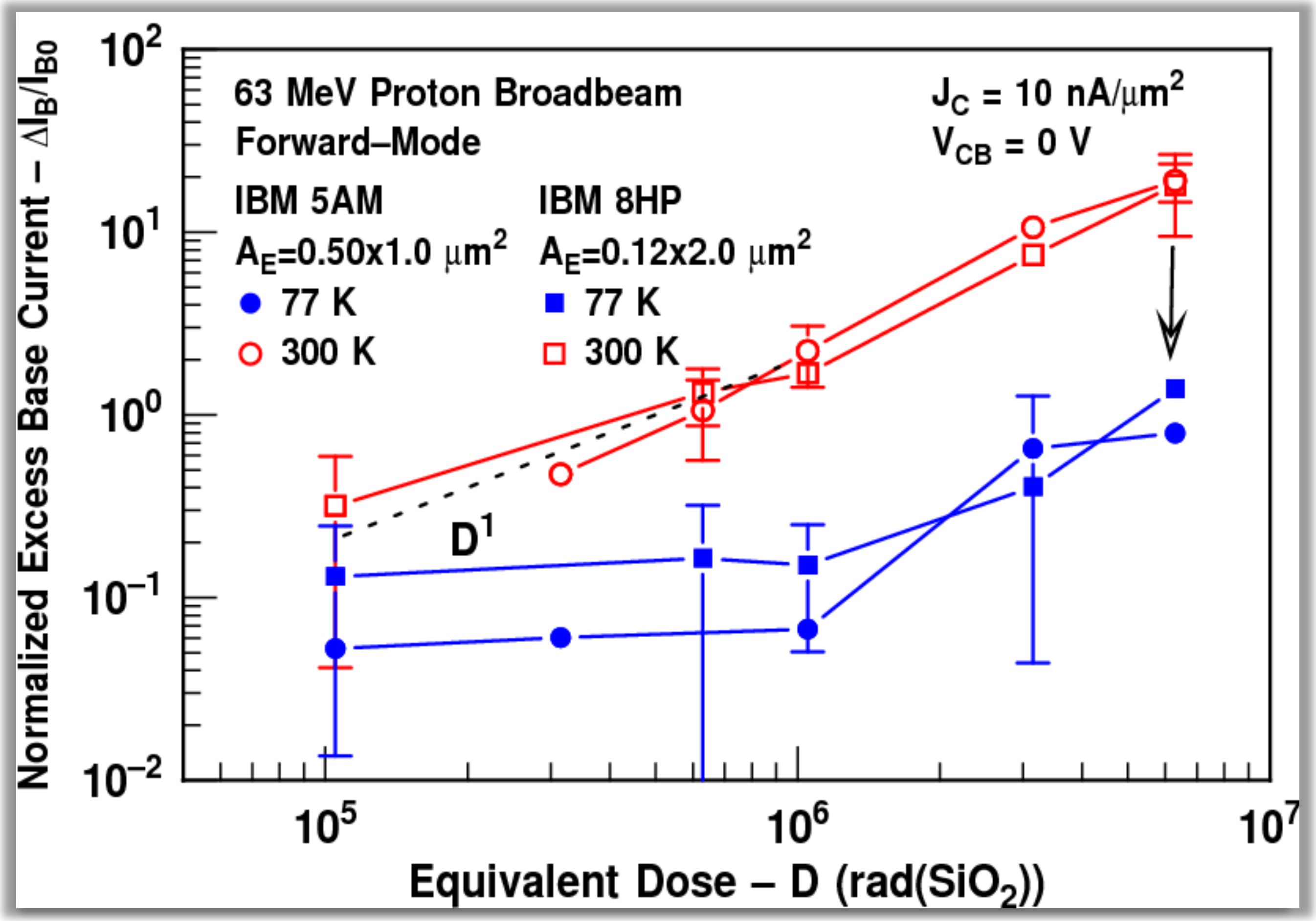


8HP & 9T



Temperature Dependence

- Hole transport slowed at 77 K → increase in self trapping
- Oxide trapped charge *increases* and interface traps *decrease*



SiGe TID Summary

- **SiGe HBTs are <u>inherently tolerant</u> to TID effects**

➡ **As Fabricated!**

- Minimal damage to <u>devices + circuits</u> (all sources, no ELDRS)
- Much more tolerant than comparable MOS technologies
- Damage dominated by low-injection SRH recombination
- No *ac* performance degradation across all SiGe generations
- TID tolerance is improved with technology scaling
- Reduced TID damage at cryogenic temperature
- SiGe HBTs function after 100+ Mrad exposure

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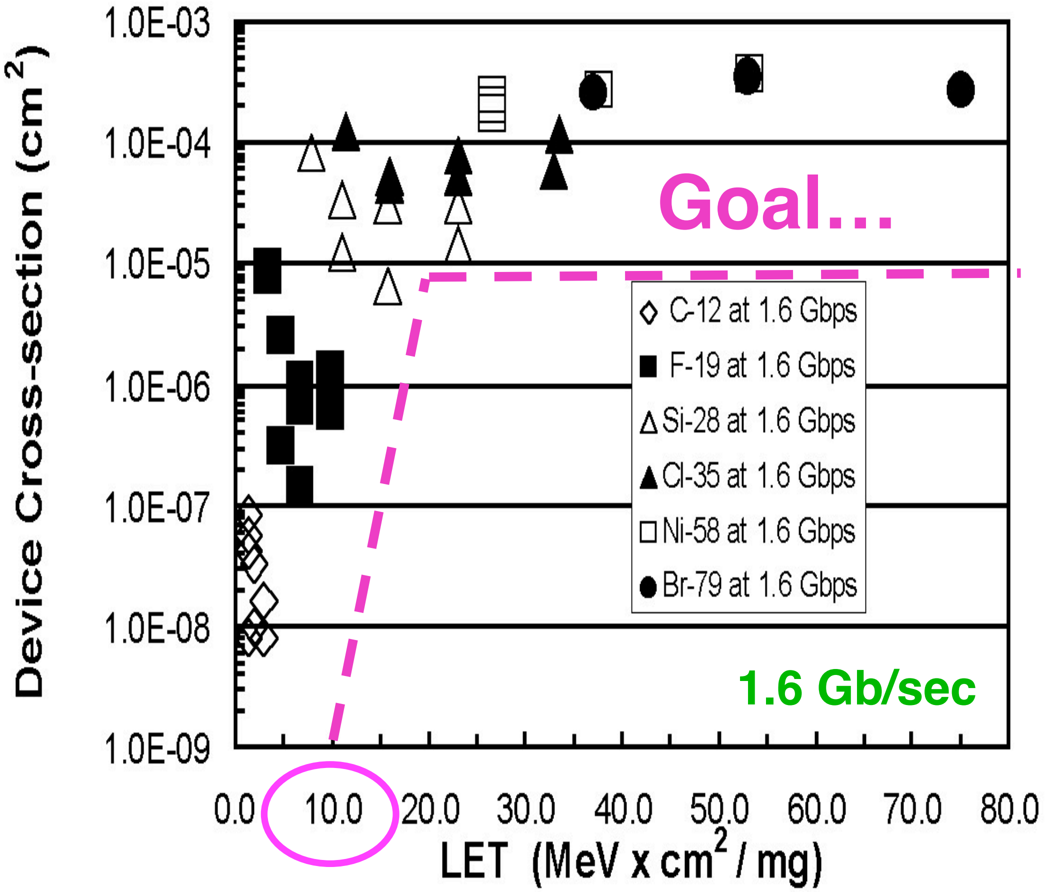
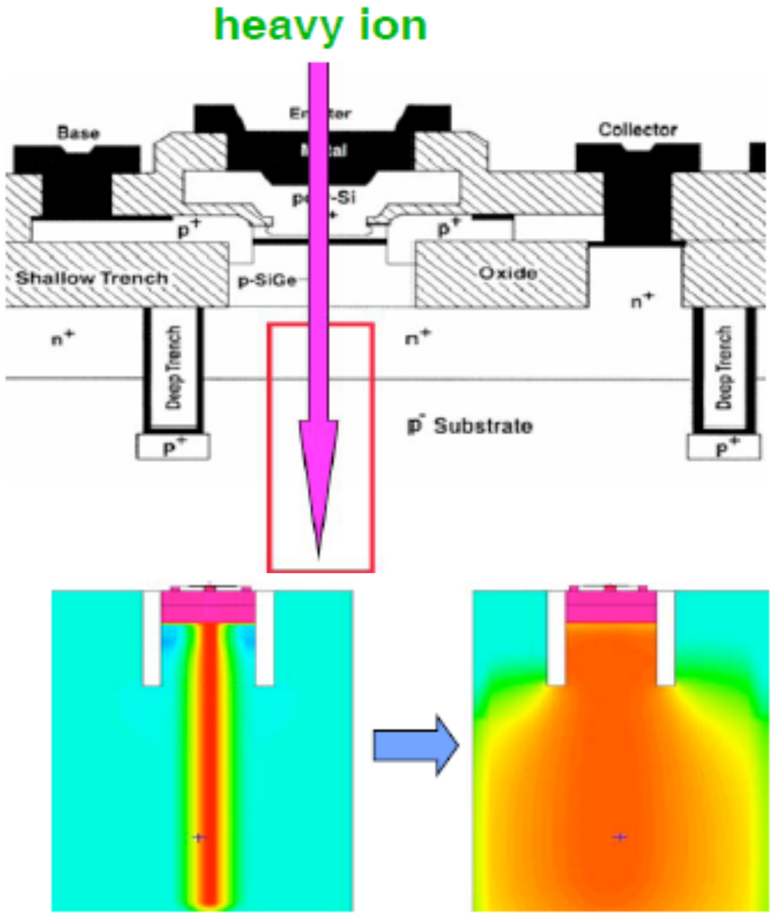
  - “n-ring” incorporation
  - bulk vs. SOI platforms
  - inverse-mode cascode
- **Mixed-mode Modeling and Circuit Exposures**
  - VCO measurements
  - BGR measurements
- **Progress & Plans**

Single Event Effects

- **Observed SEU Sensitivity in SiGe HBT Shift Registers**
  - low LET threshold + high saturated cross-section
  - TMR works, other options?

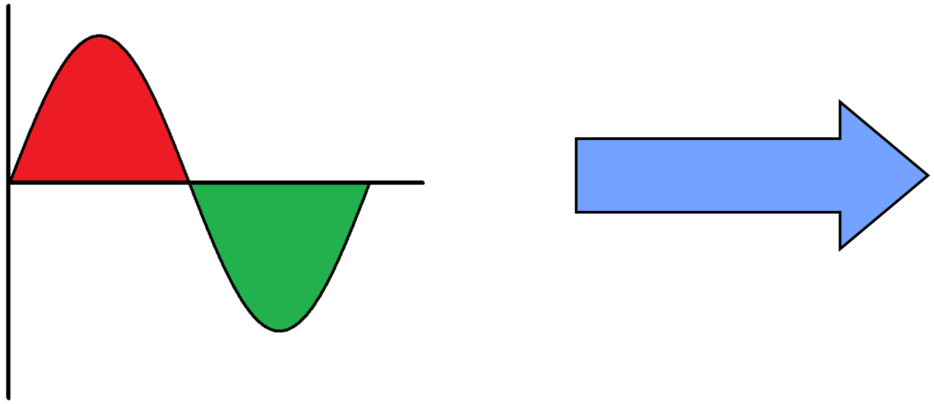




P. Marshall *et al.*, *IEEE TNS*, 47, p. 2669, 2000

SEE Experiments

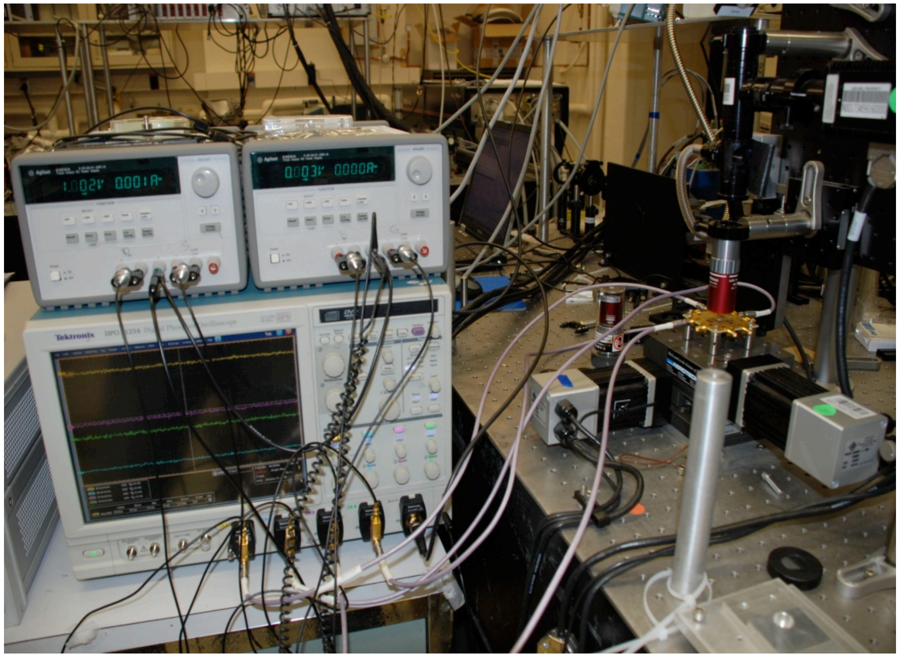
- Traditionally, IBICC is Performed for SEU
  - Measure of total nodal charge induced
  - Loss of detailed current transient
  - Less desirable for SiGe HBT logic
- Two Major Problems With IBICC Experiments
  - Rise time of charge sensitive preamp
  - Not compatible with bipolar signals
    - Possibility of charge cancellation



Complete Cancellation

TRIBICC Measurements

- Directly Capture Induced Transients on Nodes
  - Very fast (~ps) with reasonable duration (~ns)
- Difficult Measurement to Perform
  - Packaging to minimize parasitics
    - Die on board solutions

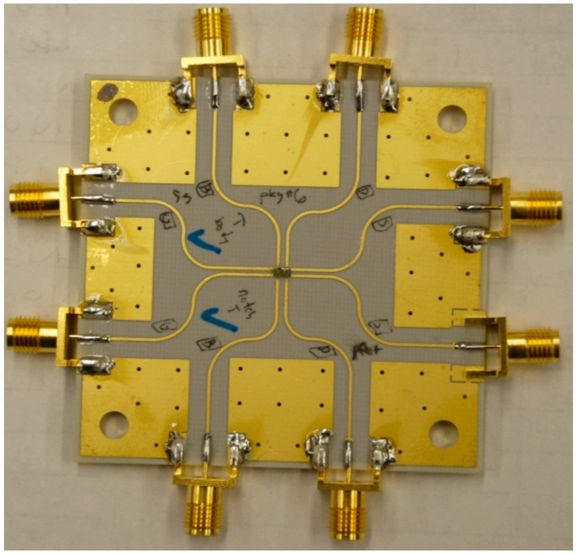


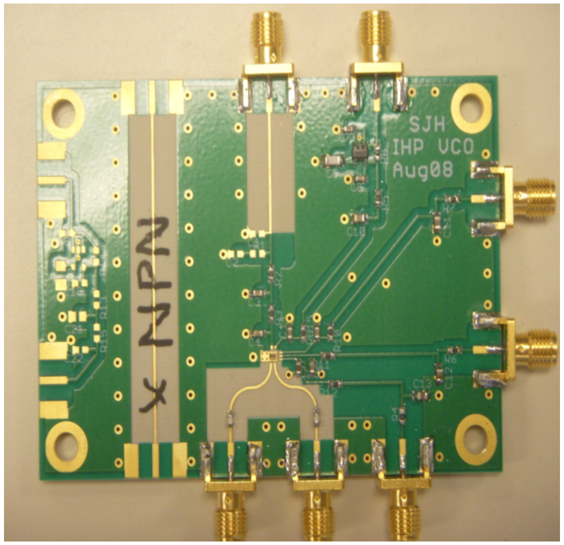
- Hardware Limitations
  - Oscope bandwidth
    - 12.5 GHz
  - Sampling rate
    - 50 GS/second

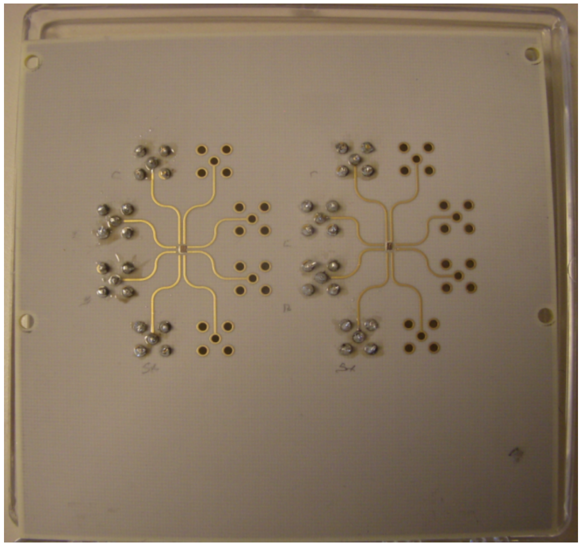
TRIBICC Board Designs

- **Board Design Dependent on Facility**
  - Back-side laser vs. Front-side heavy-ion
- **50-ohm Microstrip Lines**
  - Rogers 4003C dielectric
  - Characterized using HFSS

Simulations show functionality up to 30 GHz







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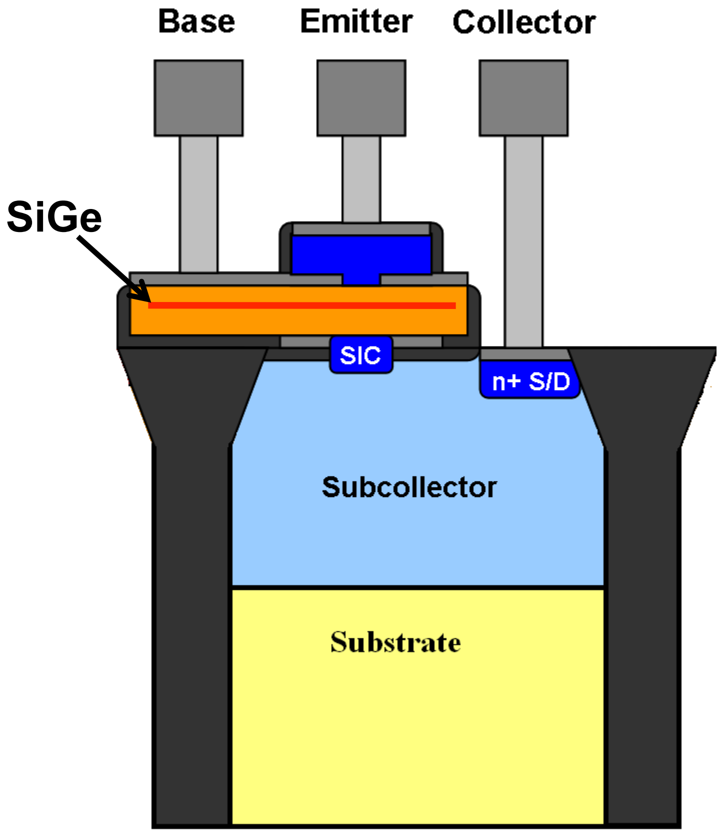
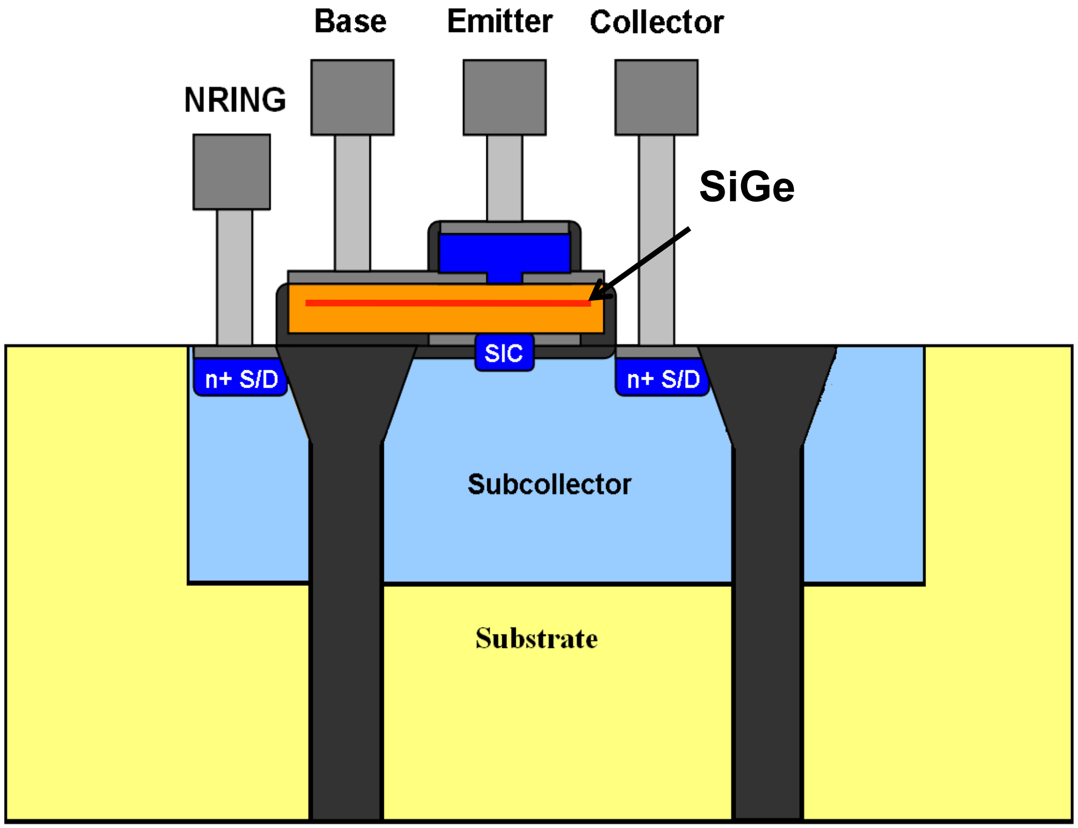
N-Ring SiGe HBTs

- **Competing N+ Junction External to Device**
  - **Shunt path for charge → reduce collector charge**



Standard HBT

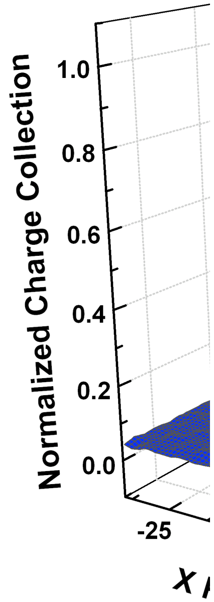


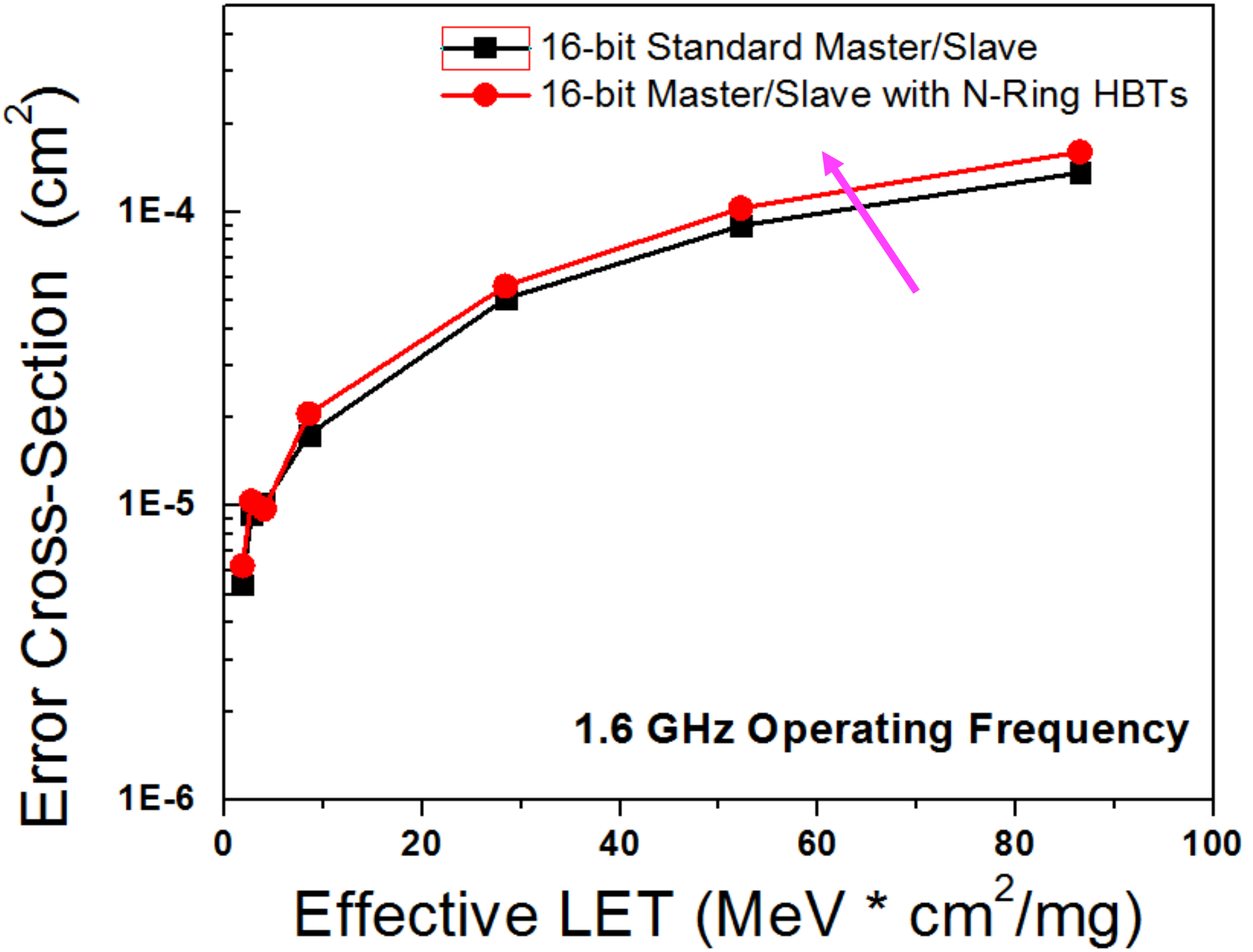
NRING HBT

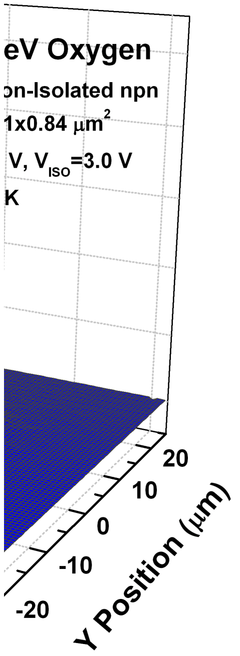
NRING IBICC Results

- **Charg**
  - sigr nsitive area)

T







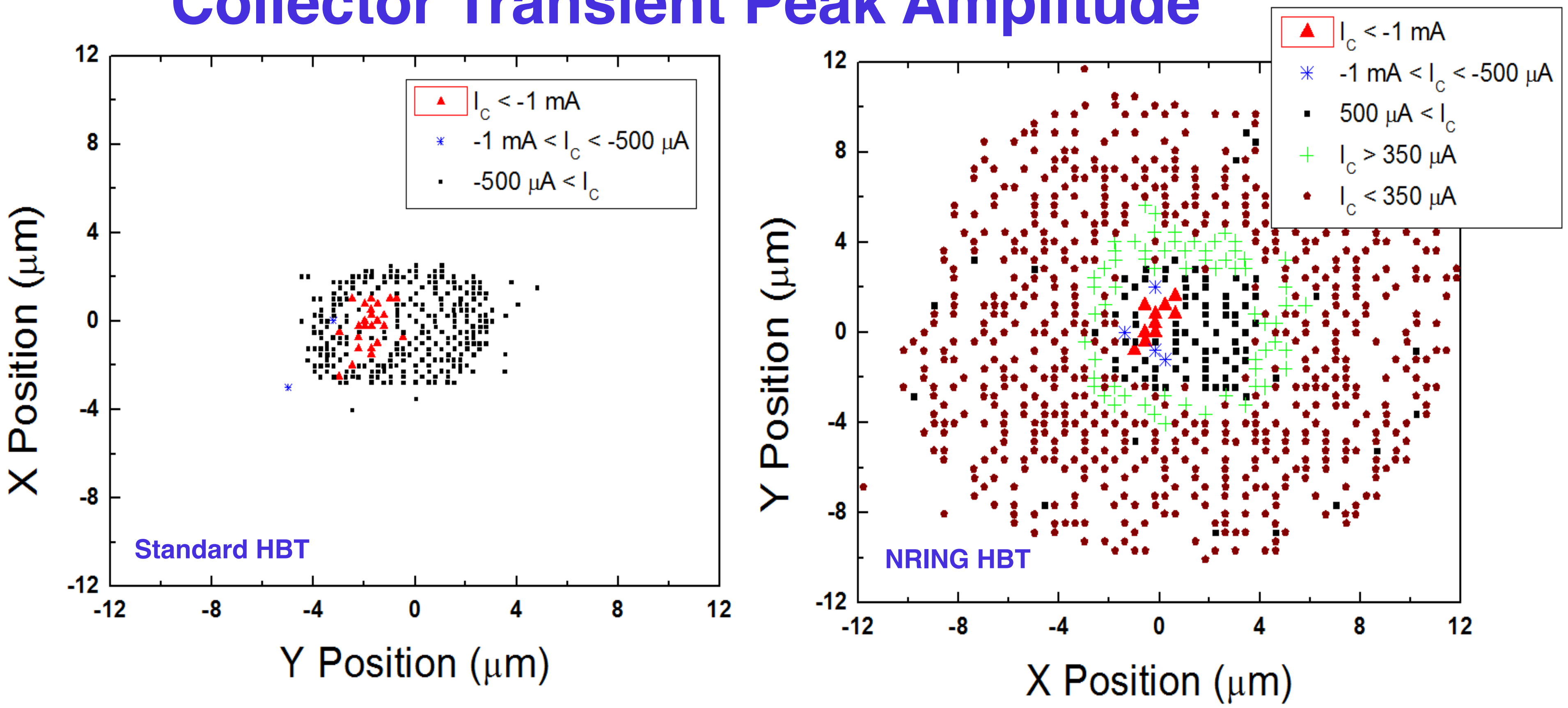
Q: Are the IBICC results real?

John D. Cressler, 5/25/10

NRING TRIBICC Results

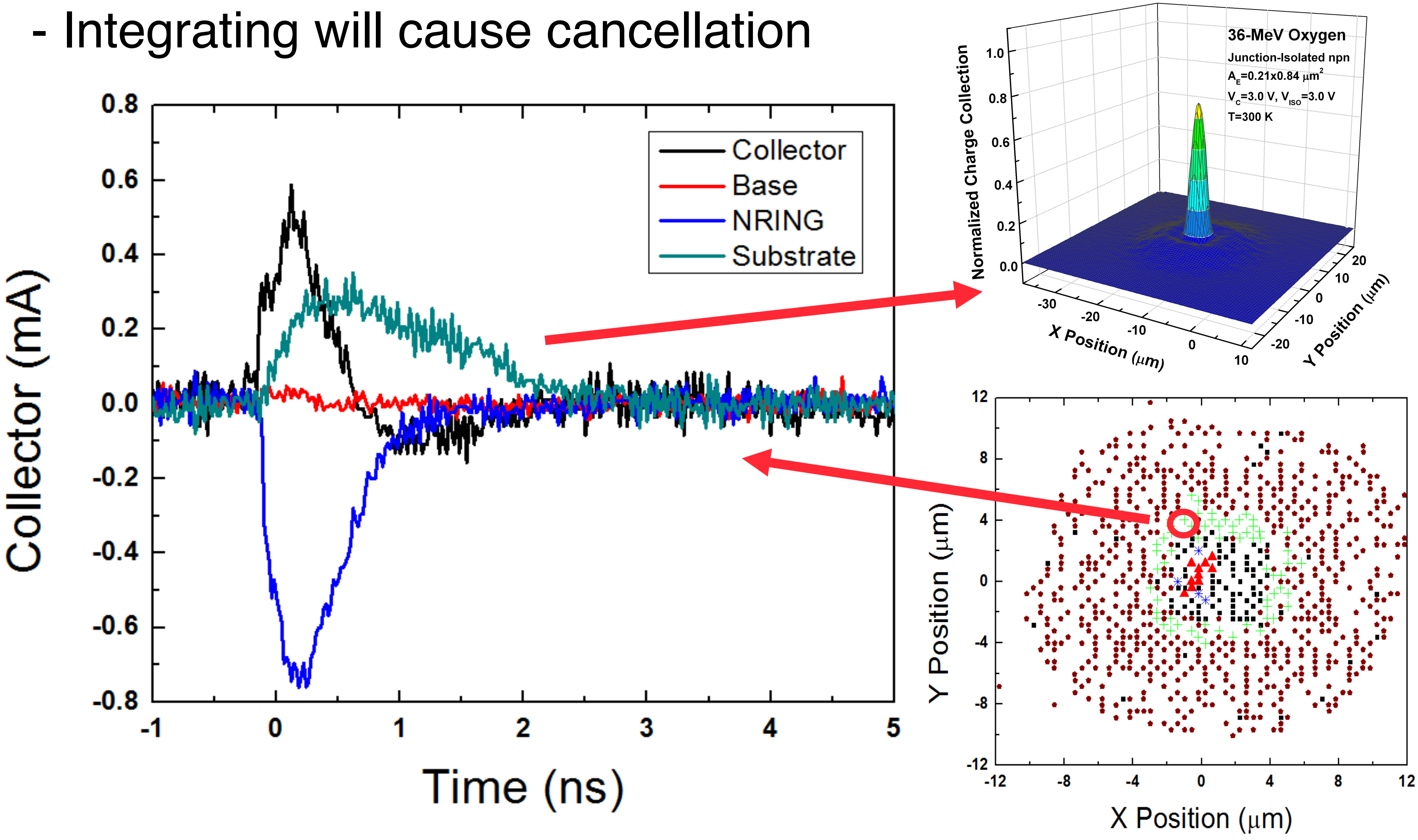
- **TRIBICC Shows Strikingly Different Results**
  - NRING device has **large** increase in sensitive area
  - Positive transients exist outside the deep trench

Collector Transient Peak Amplitude



Exterior Transients

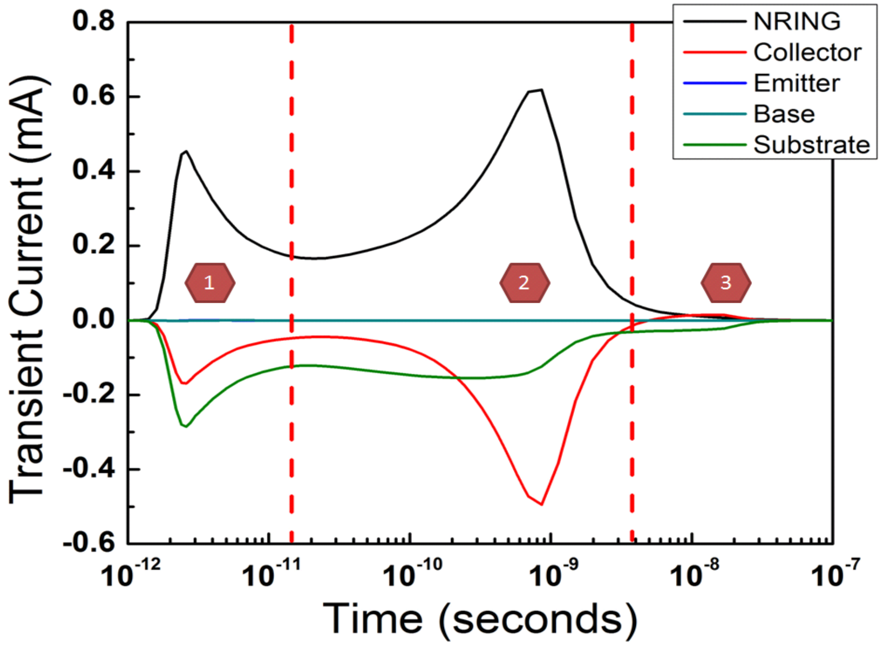
- **Transients Induced Outside the Deep Trench Are Bipolar**
  - Integrating will cause cancellation



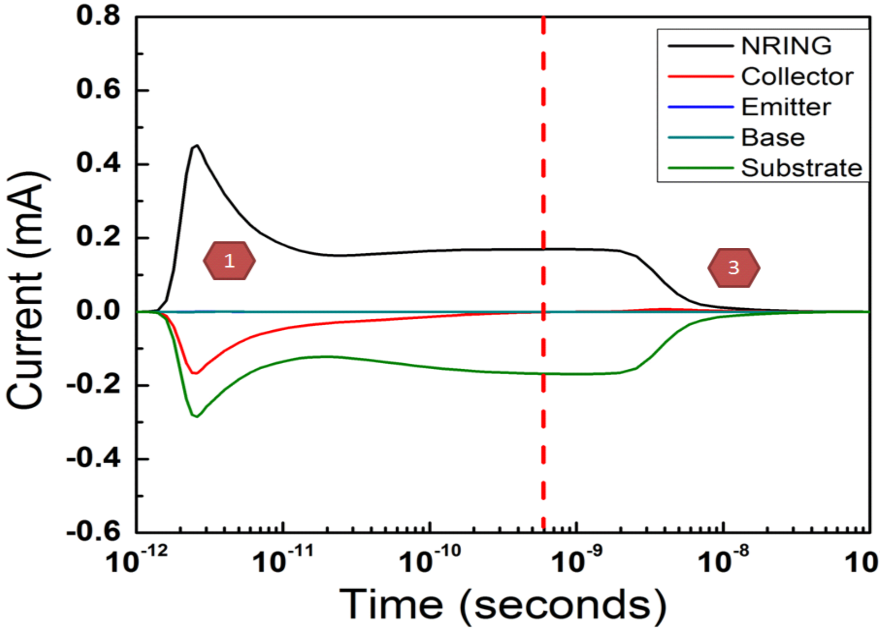
3-D TCAD Simulations

- **Transient current waveform strongly dependent on bias**
  - Worst case for collector at lowest potential
    - Parasitic NPN turning on (nring-substrate-subcollector)
  - Response broken into three regions

V_{NR} = 3 V, all others 0 V

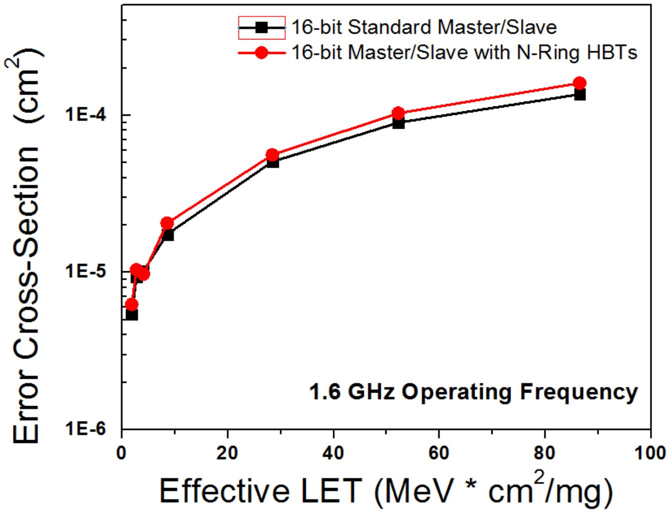


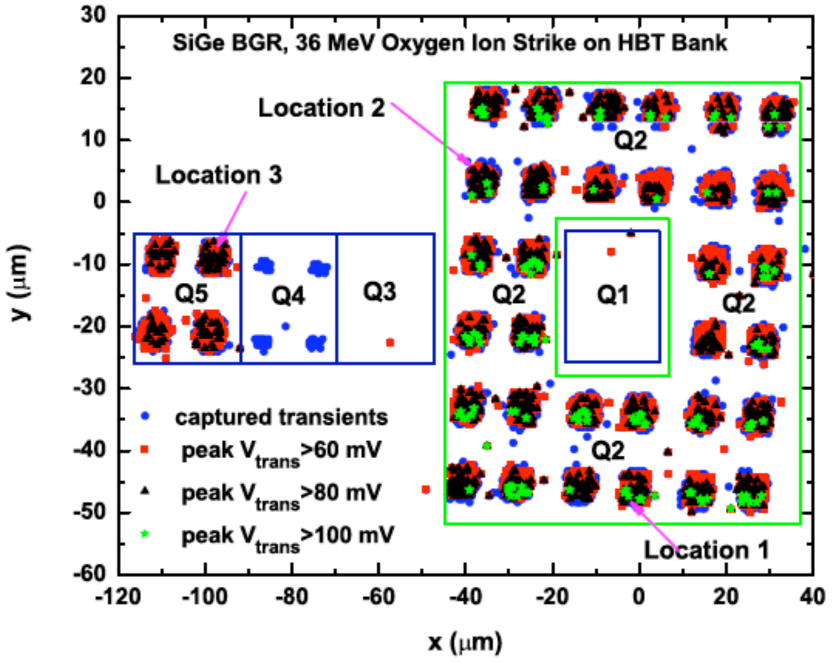
V_C, V_{NR} = 3 V, all others 0 V

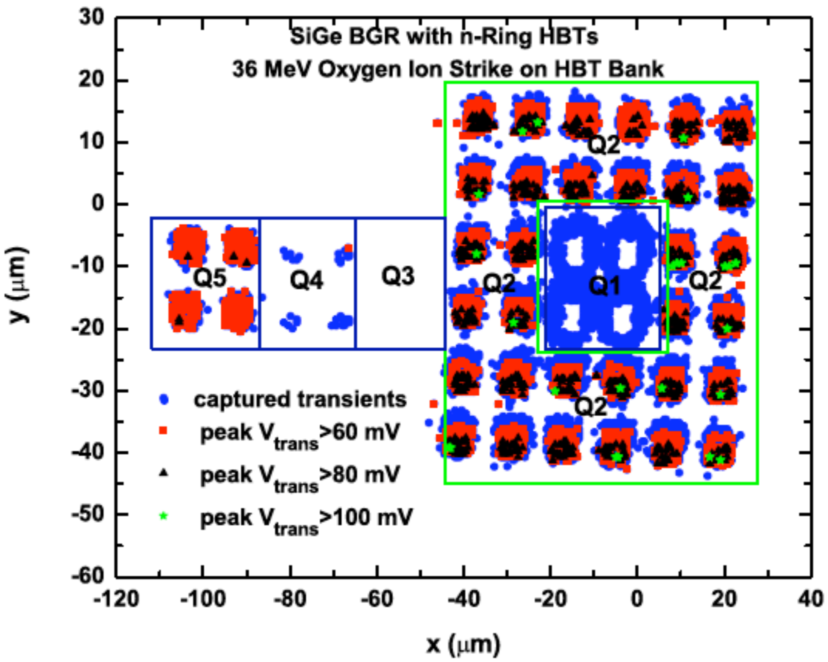


Circuit Implications

- **Digital vs. Analog**
  - Application specific answer!

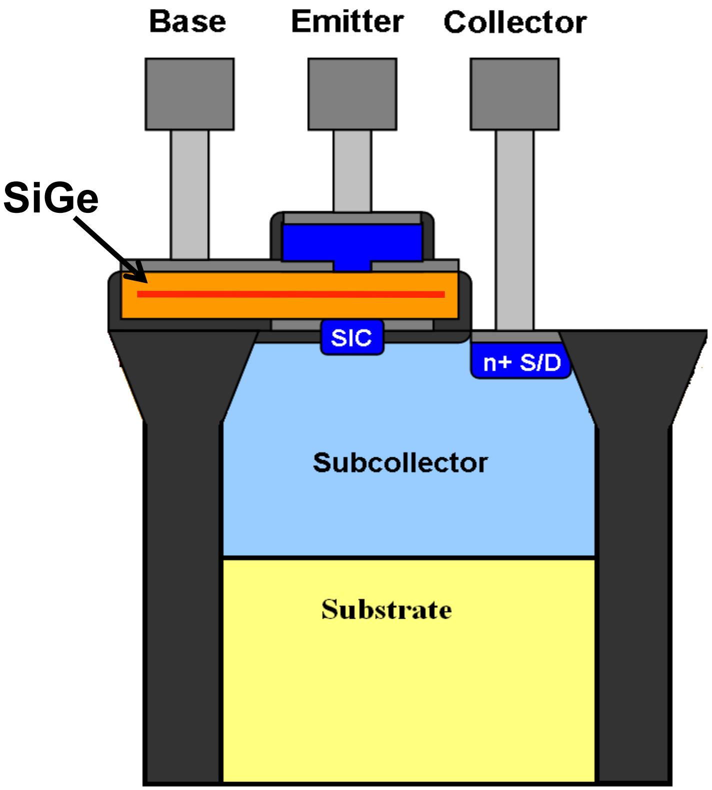


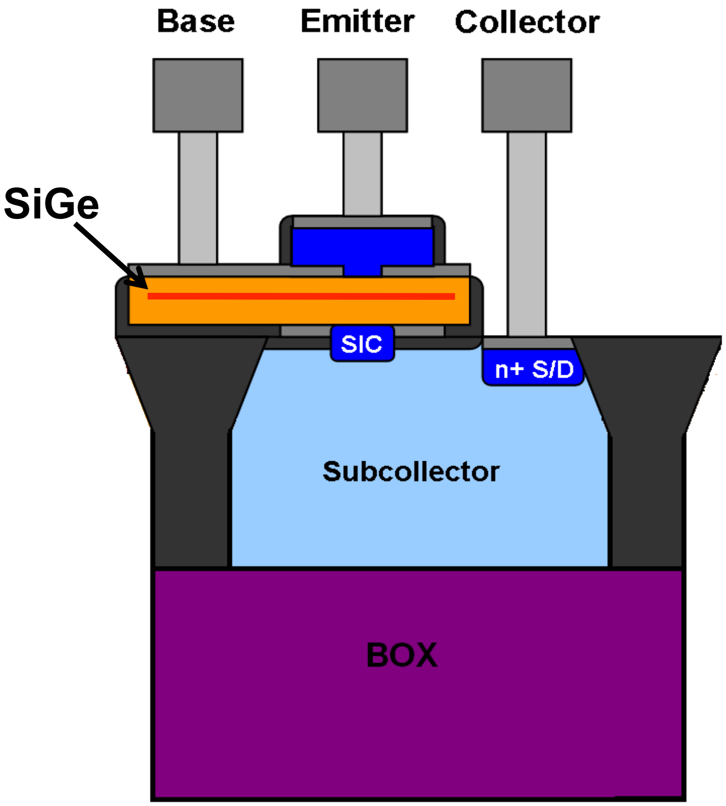




SOI vs. Bulk Platforms

- **SOI (Buried Oxide) vs. Bulk Platforms (NPNs)**
  - less charge deposited in the sensitive volume
  - expected to decrease "diffusion charge"



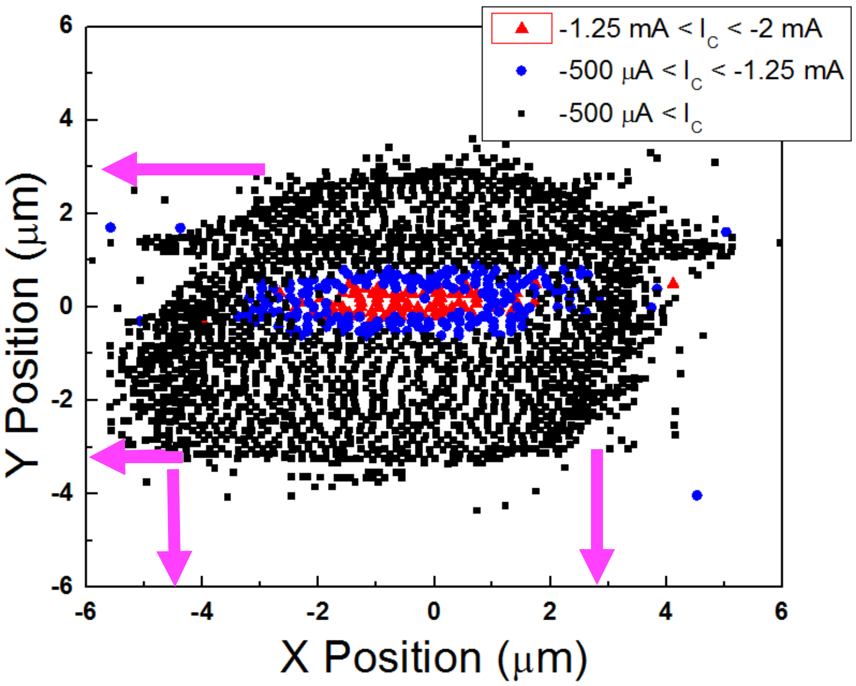


Microbeam Results

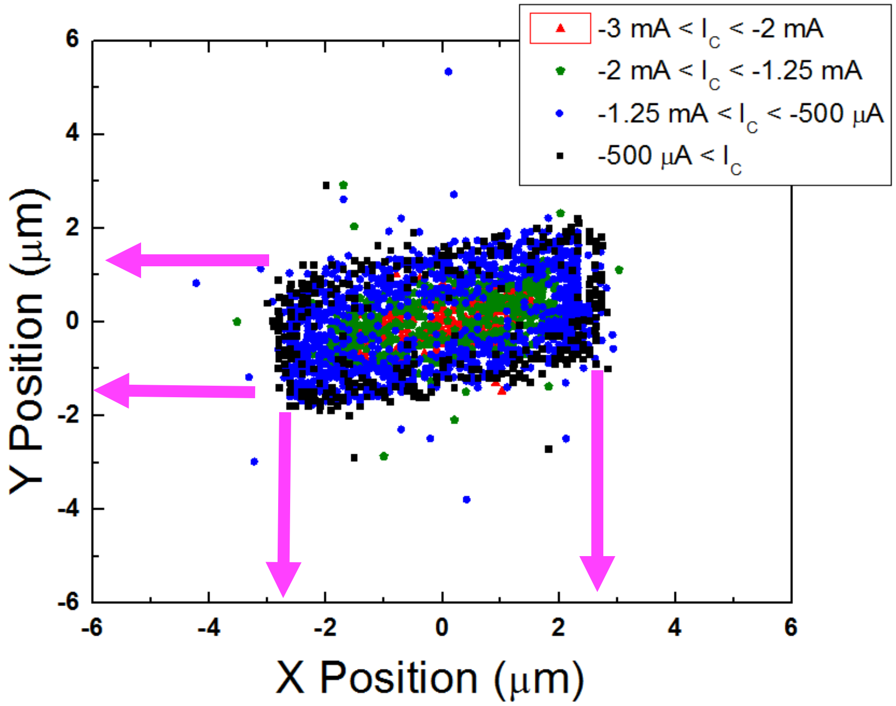
- **Two Distinguishing Differences Between Platforms**
  - **(1)** Reduction in sensitive area for SOI platform

45 um^2 → 7.5 um^2

Collector Transient Peak Amplitude

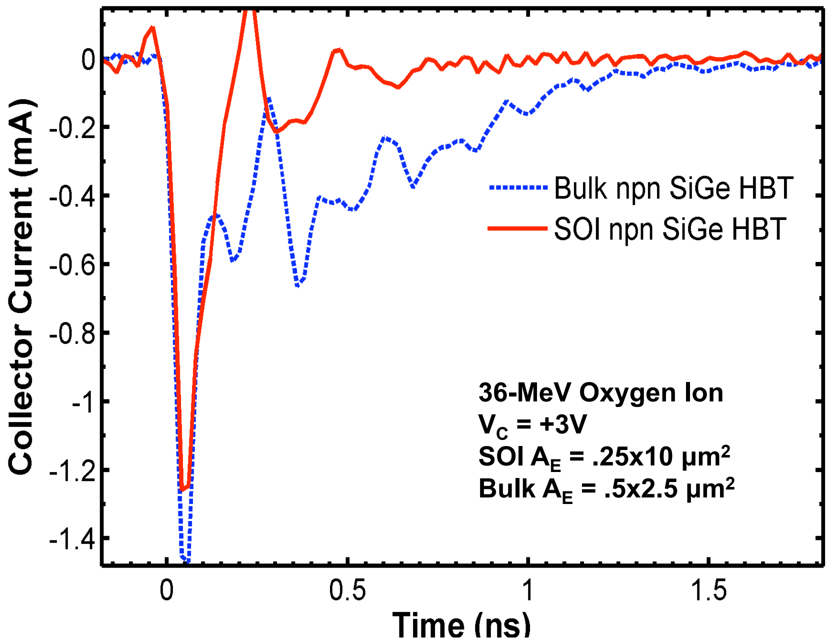


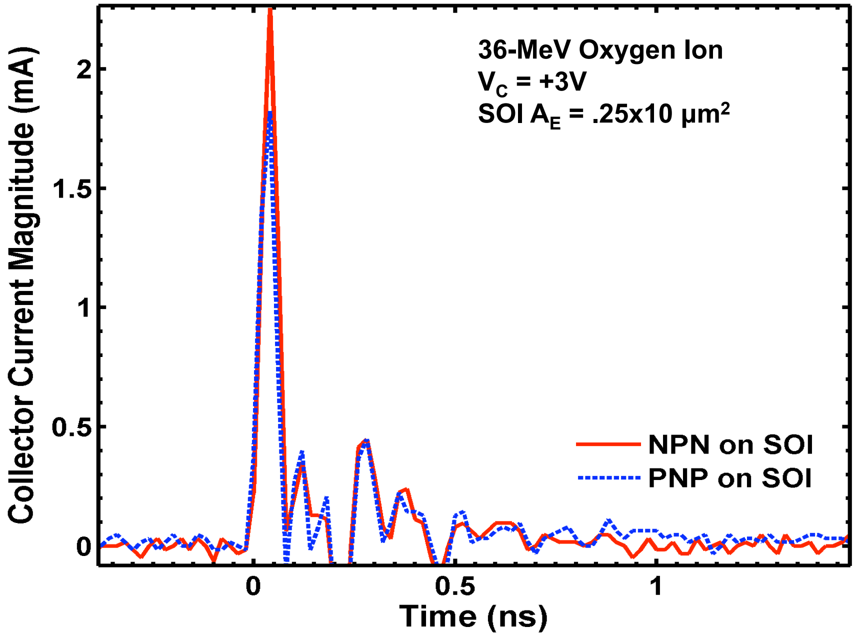
Bulk



SOI

TRIBICC Measurements





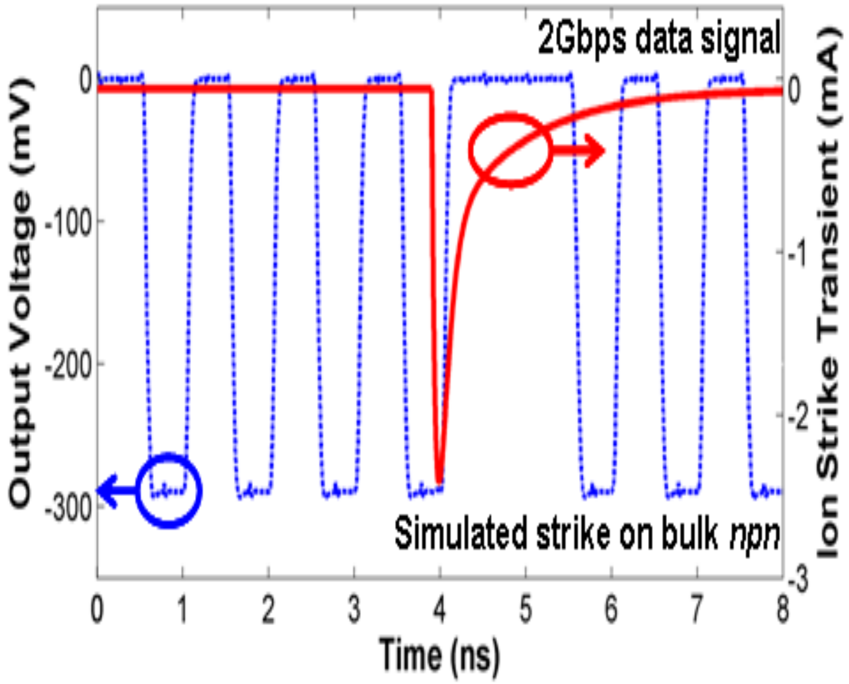
(2) Significant reduction in transient duration

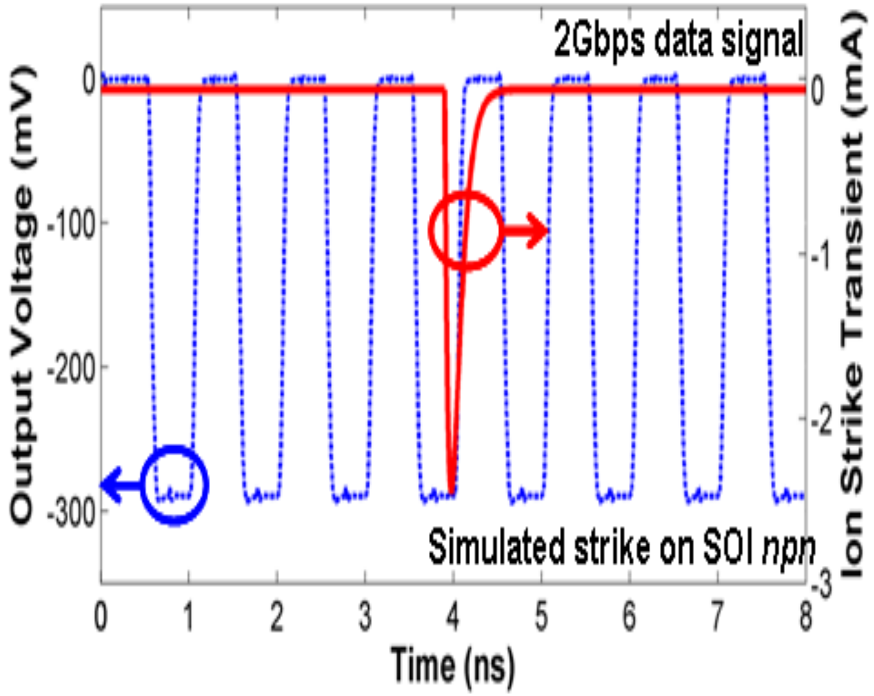
~ 1.5 ns → ~ 0.5 ns

- **Similar response between NPN & PNP SOI devices**
- **Peak amplitudes are similar between platforms**

Shift Register Simulations

- **Modeled current pulses from transient data**
- **Inject transient currents in spectre simulations**
  - Injected just prior to clock edge (maximizes sensitivity)
- **Upsets seen only for register built with bulk devices**



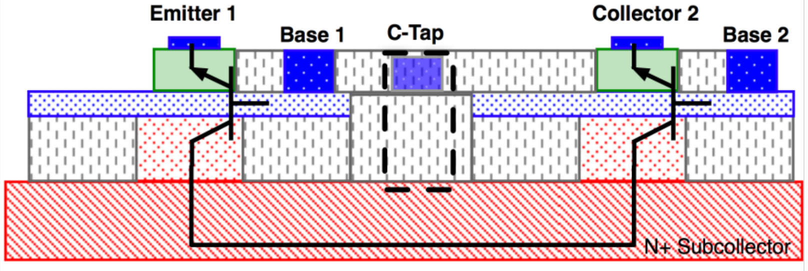


Inverse-Mode Cascode

De-couple sensitive junction from circuit output

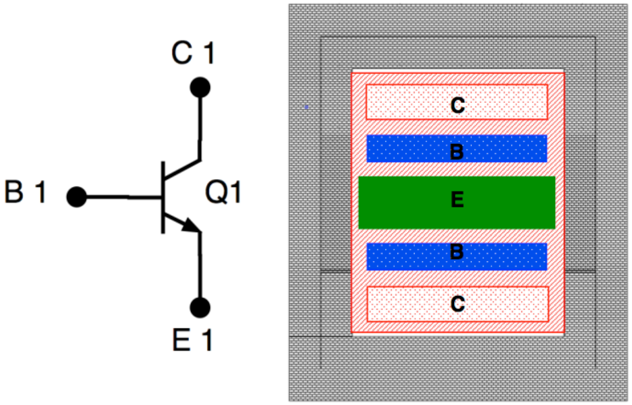
- **two transistors operating as one (“cascoded pair”)**
- **top device inverse-mode, bottom device forward-mode**
- **need coupling C-Tap to rail for radiation tolerance**

➔ Inverse-Mode Cascode (IMC)

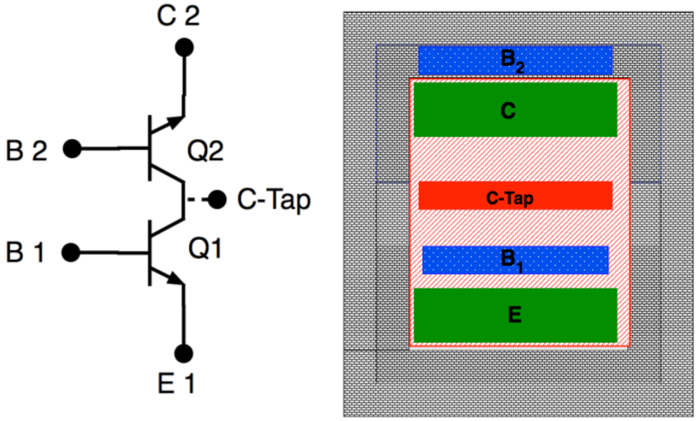


Cross-section of modified device

Industry



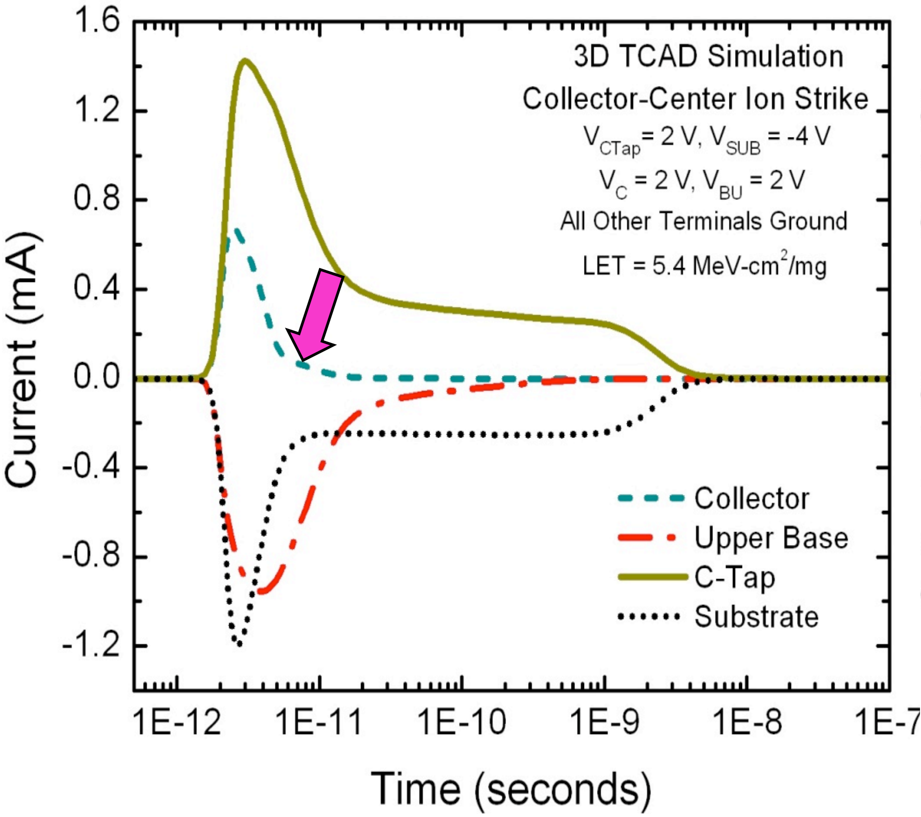
Our Solution

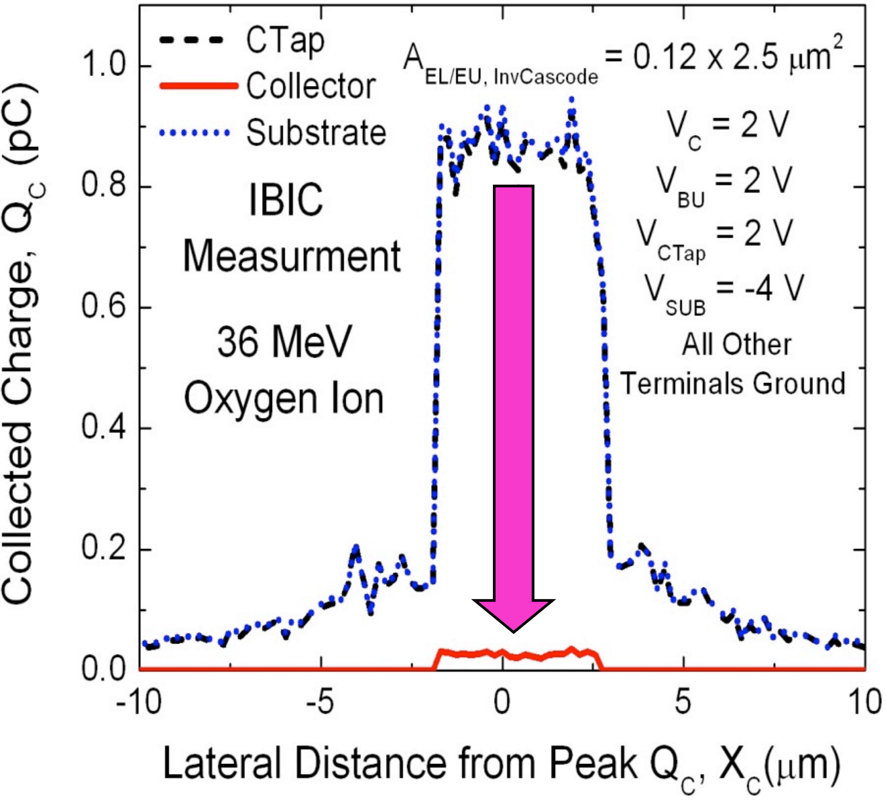


Modeling & Measurement

- IMC with C-Tap → Only Deposited Collector-base Charge
- Collector Terminal Shielded from Bulk Charges
- For Simulations C-Tap Tied to DC Potential

Q: How do we dynamically bias the buried subcollector?





Biasing the C-Tap

Solution: Capacitive Coupling

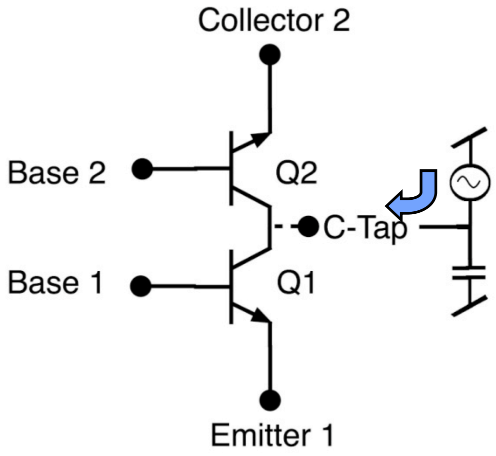
- filter high frequency components
- will decrease speed of IMC

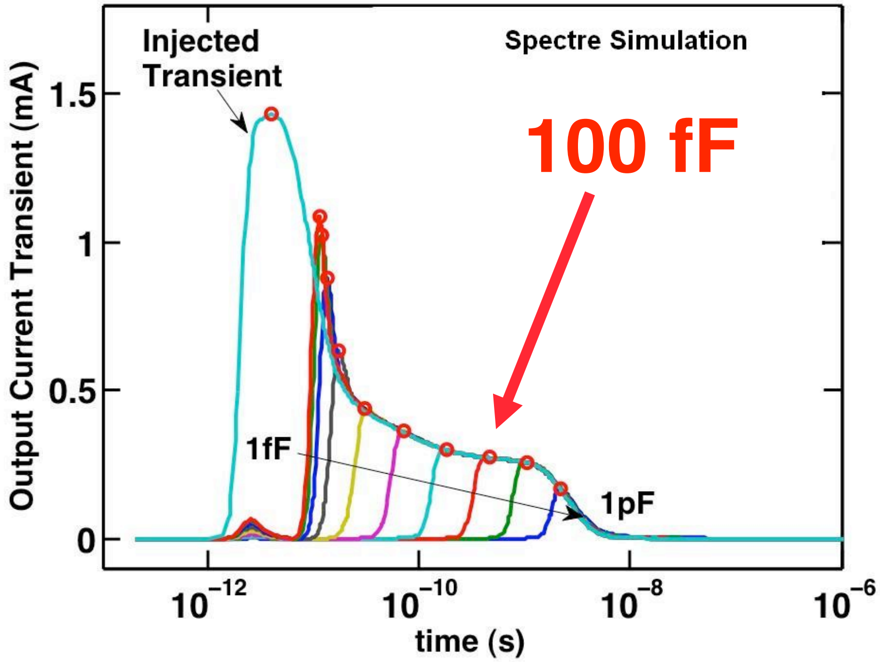
- **Spectre Simulations**
  - transient current injected at C-Tap
  - varying capacitor values
  - monitor collector transient

NET

Significant Transient Mitigation Without Large Decrease of Device Speed

Multi Gbit/s Enabled!

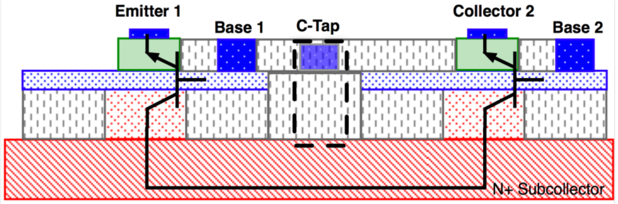




Digital Circuits

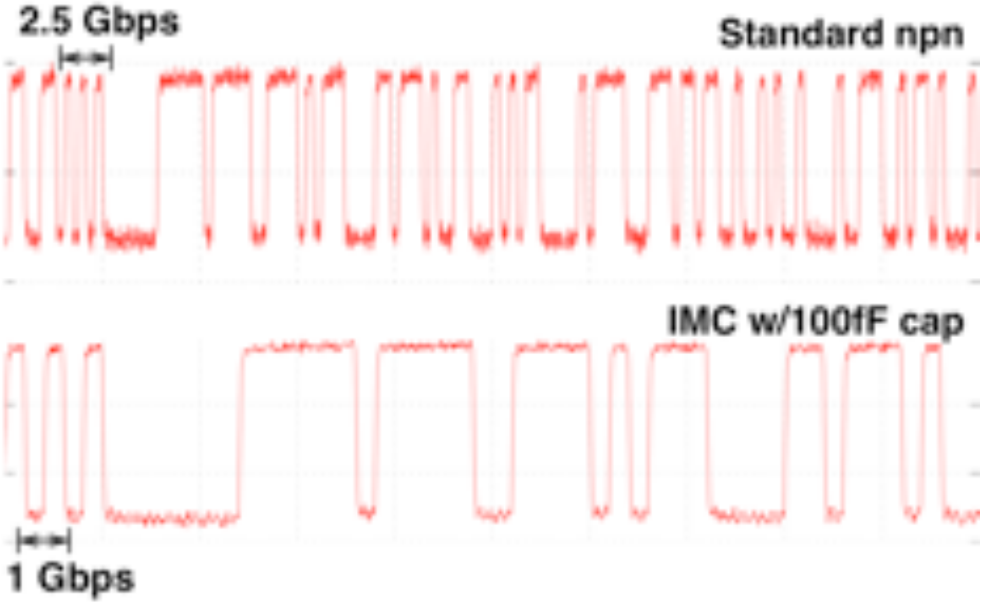
Simple device modification

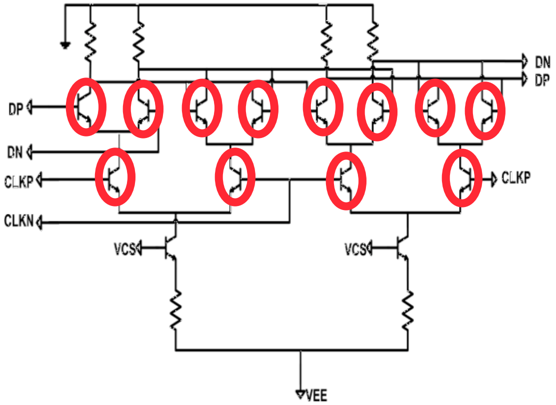
✓No increase in device area
✓Trivial to integrate into digital logic



Measured Performance of 1st generation IMC shift register with CTAP capacitive loading

IMC SR w/cap > 1 Gbps





Ready for Broadbeam!

Outline

- **SiGe HBT Technology & Extreme Environment Applications**
- **Total Dose Effects on SiGe HBTs**
  - damage mechanisms, temperature dependence, scaling
- **Single Event Studies of SiGe HBTs**
  - TRIBICC vs. IBICC
- **Hardening Methodologies & 3-D Modeling**
  - “n-ring” incorporation
  - bulk vs. SOI platforms
  - inverse-mode cascode
- **Mixed-mode Modeling and Circuit Exposures**
  - BGR measurements
- **Progress & Plans**

Circuit SET Modeling

- **Approaches to simulating circuit SET:**
  1. Inject analytical double exponential transient
  2. Inject computed 3D TCAD transients at “worst-case” biases
  3. Inject computed 3D TCAD transients at circuit nodal biases
  4. Full mixed-mode simulation (3D TCAD within Spectre)

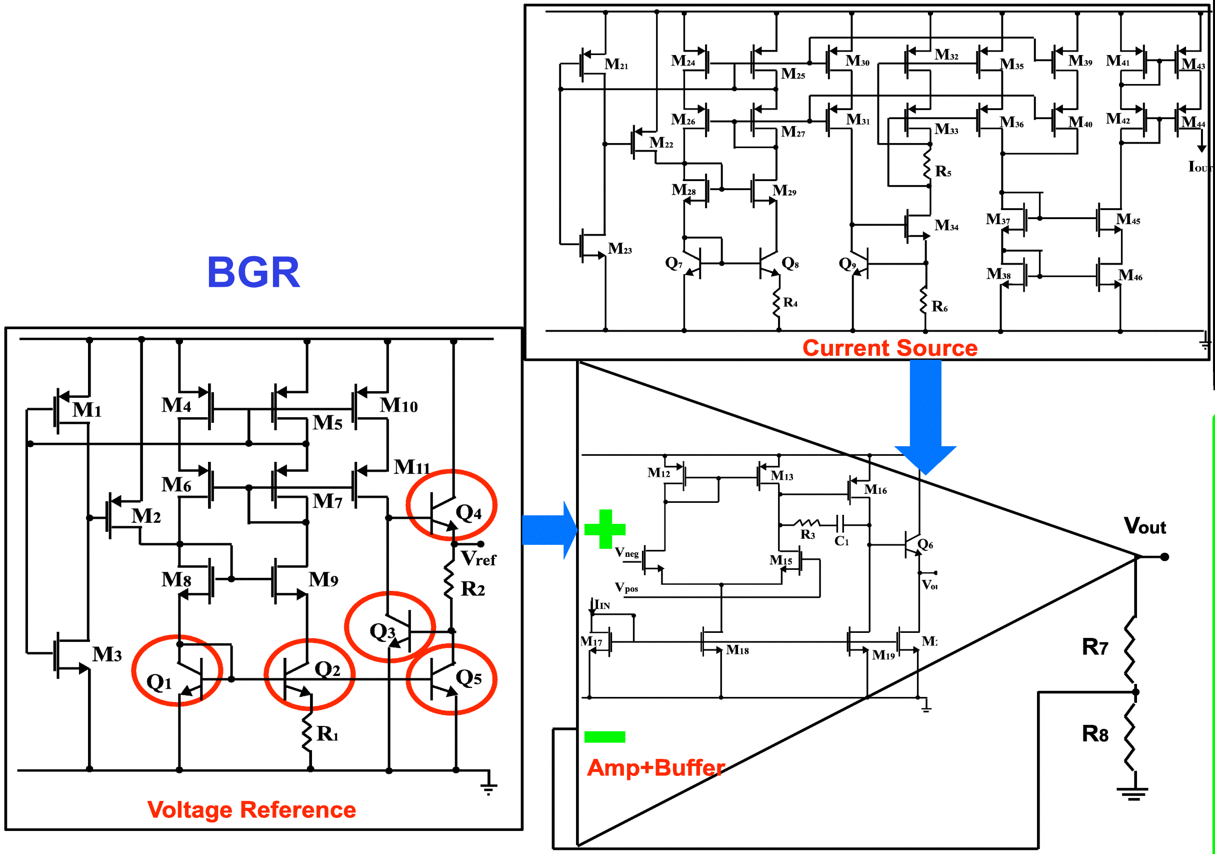
- **Under what conditions will these diverge?**
  - Spectre-only simulations will not always capture real SET
  - Full mixed-mode can capture feedback effects
  - Depends on temp., bias, circuit topology, analog vs. RF…

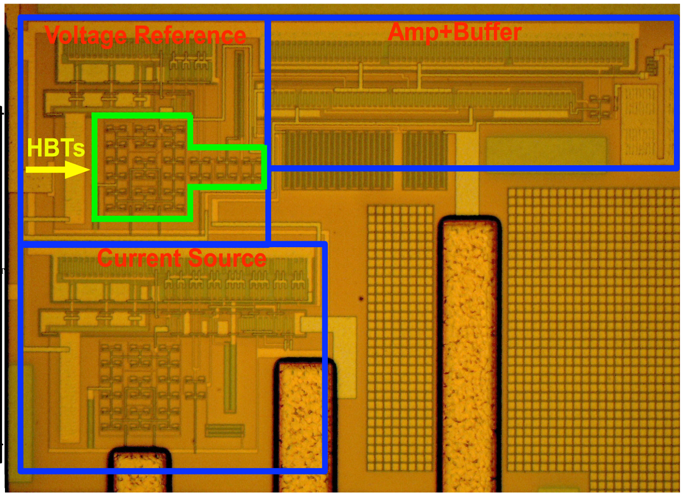
Key: Need to validate simulations against measured data

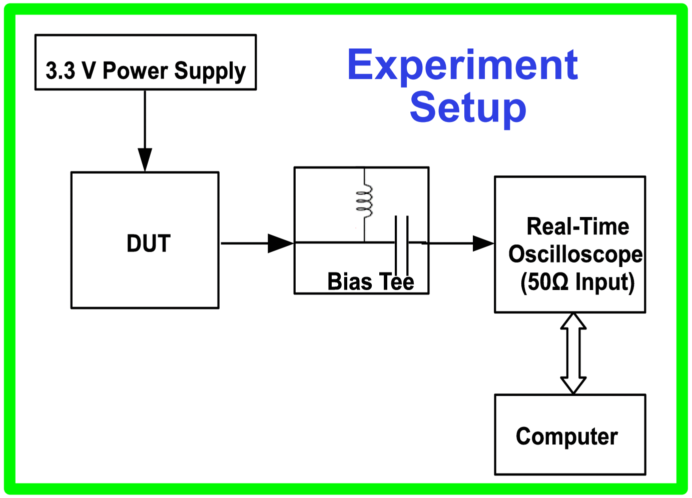
SET in a SiGe BGR

- Bandgap voltage reference used inside a regulator circuit
- SiGe HBTs in BGR were bombarded by 36 MeV oxygen ions

BGR







Experiment Setup

3.3 V Power Supply

DUT

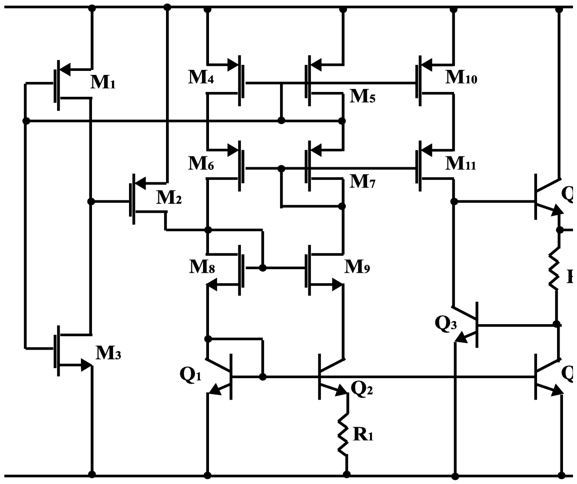
Bias Tee

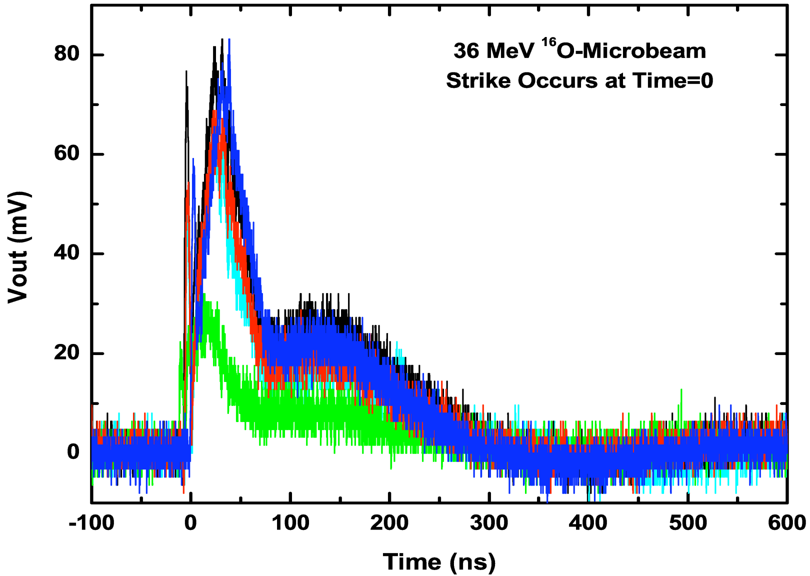
Real-Time Oscilloscope (50Ω Input)

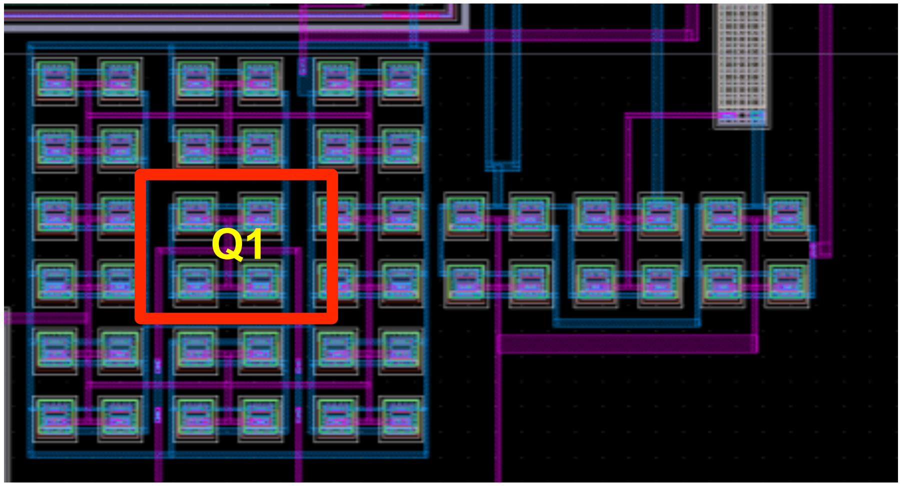
Computer

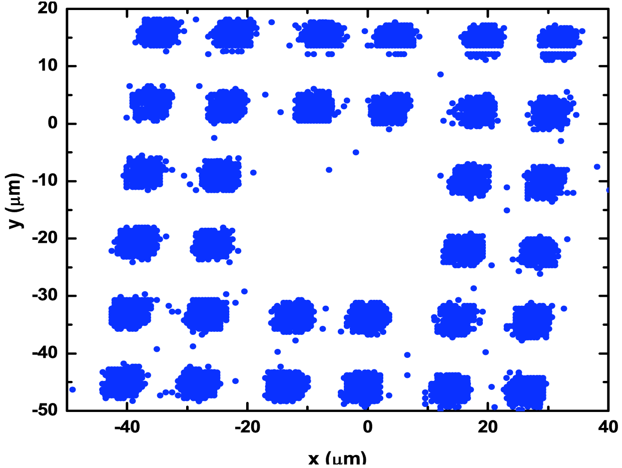
SET in a SiGe BGR

- Transient response depends on the location of the strike
- Transients on Q2 in the PTAT branch show worst-case response



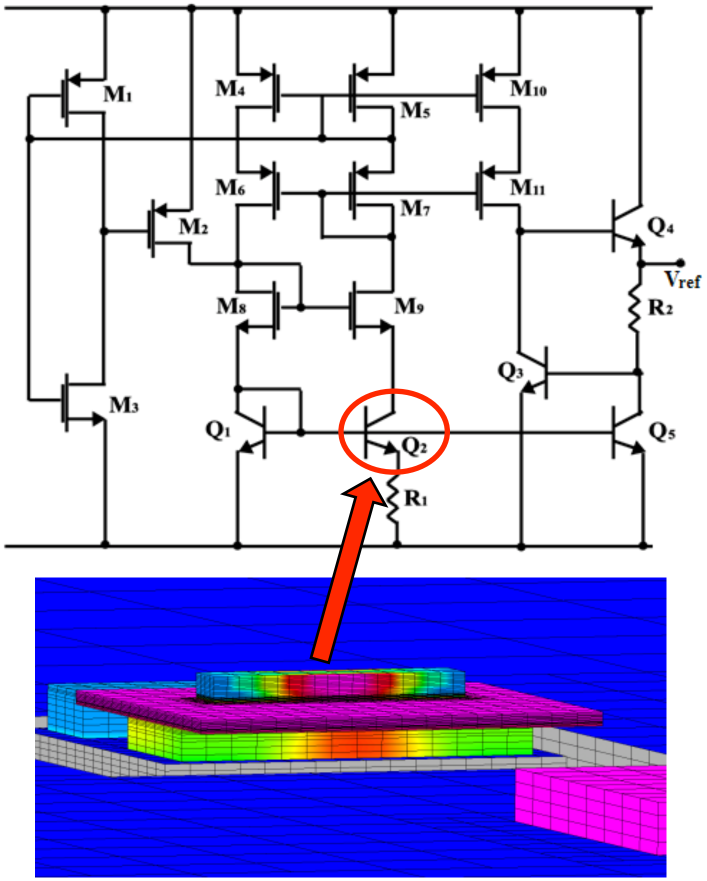

36 MeV ^{16}O-Microbeam
Strike Occurs at Time=0

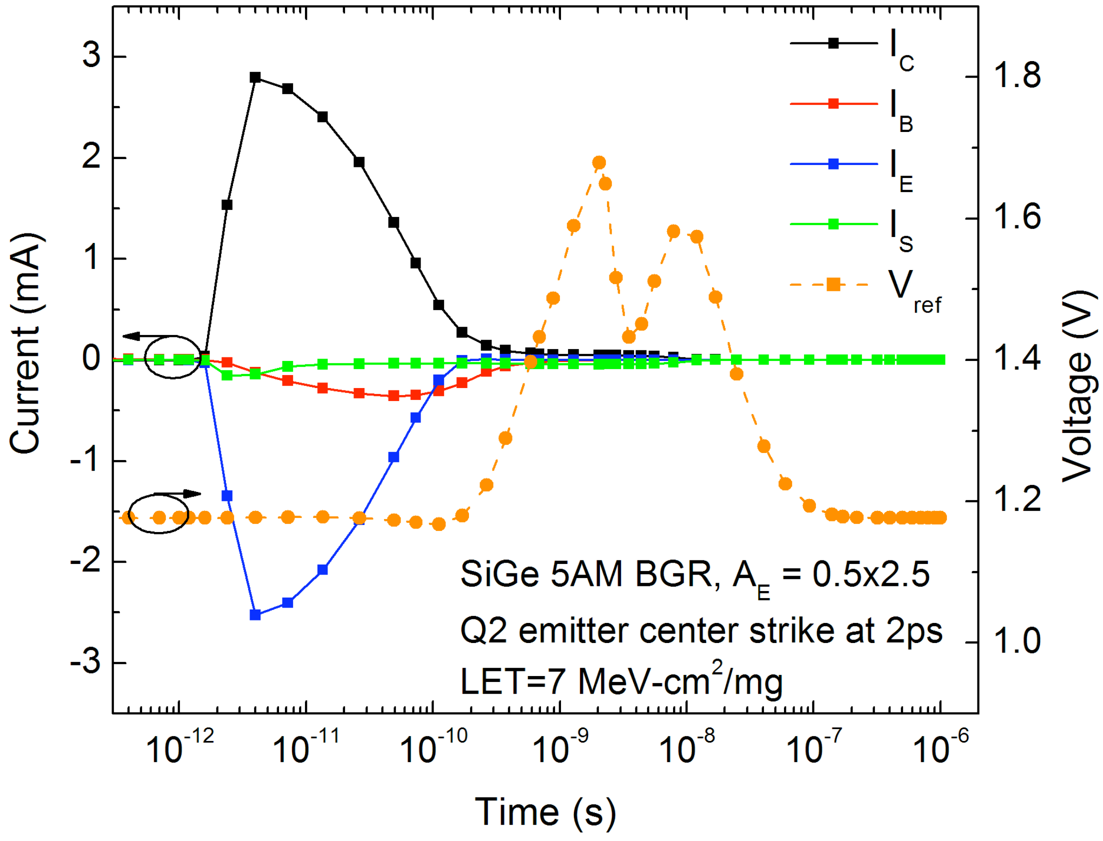




True Mixed-mode SET

- **CFDRC MixCad (Spectre + 3D NanoTCAD) used to simulate SET**
- **SiGe HBT response in BGR not equal to standalone SiGe HBT**
- **Mixed-mode SET shows long output transient (as measured!)**

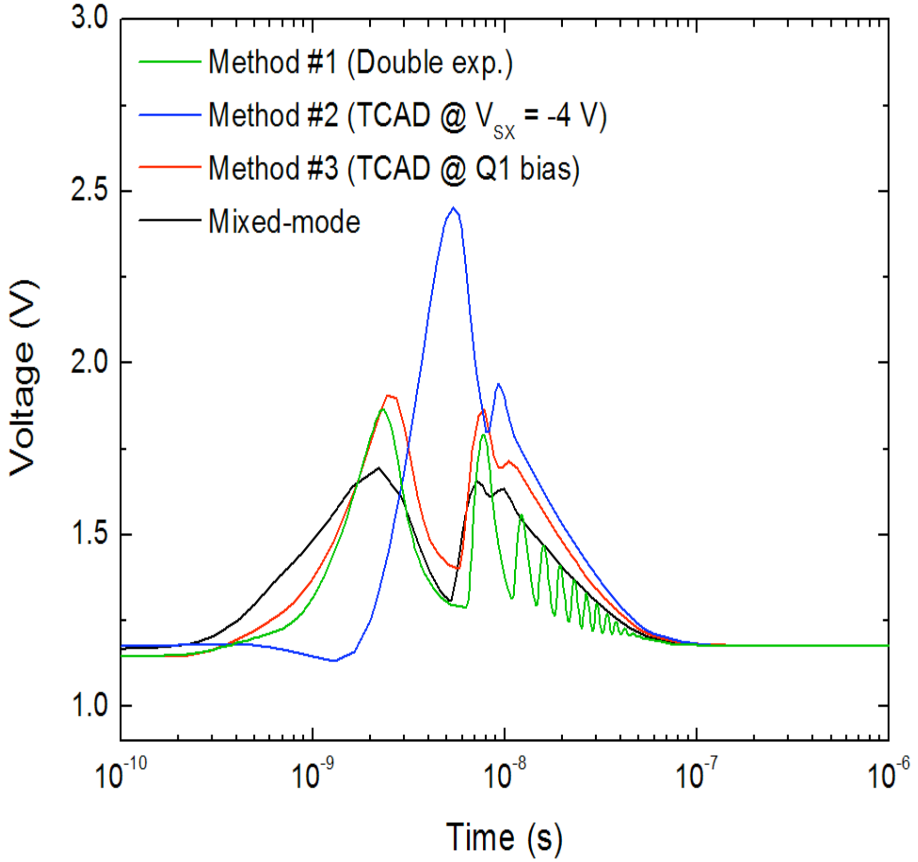




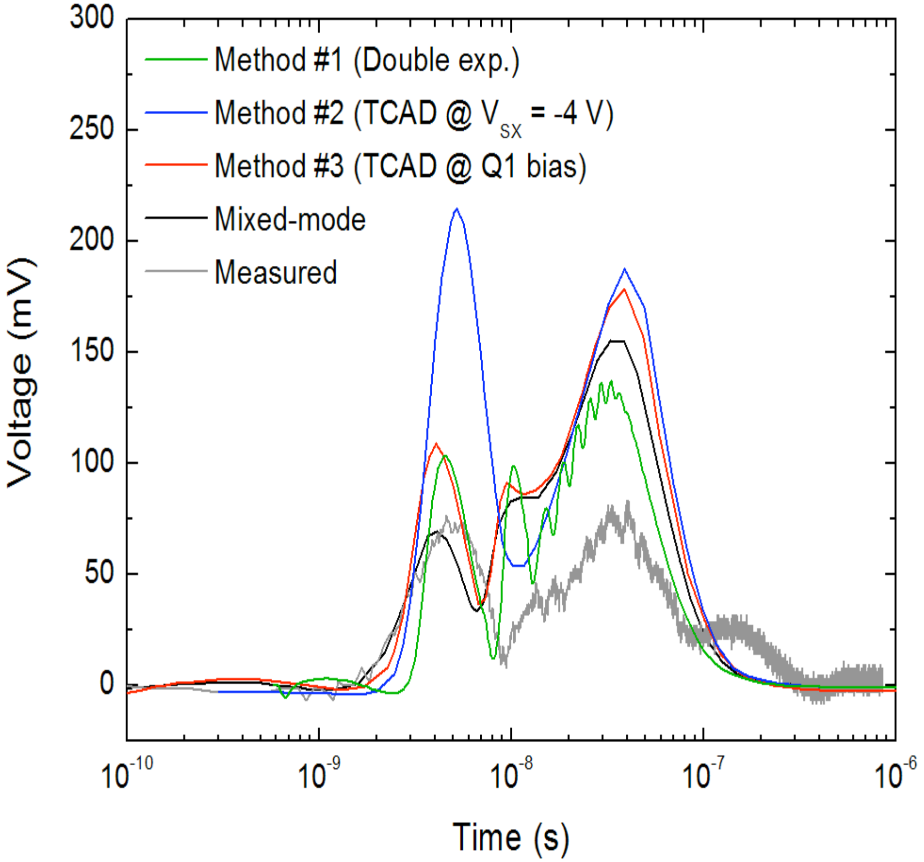
Mixed-mode vs. Spectre

- **Schematic modified to emulate measurement setup**
  - Include all parasitic elements (bias tees, cabling, scope, etc..)

Transients at BGR output



Transients at oscilloscope



Progress & Plans

No-cost Extension Granted to 8/31/10

Continue Our Exploration of Device-level SiGe Hardening

- Near-term broadbeam heavy ion experiment planned
  - Inverse-mode cascode shift registers
  - SiGe on SOI shift registers
- Characterization of self-heating effects in SiGe on SOI
  - new Agilent pulse-mode measurement system will support this
- Continue to investigate device-circuit interactions (mixed-signal)
- Continue to hone TCAD for addressing circuit response

Much Learned! ….. Much to be Done Still!

Wish List – a follow-on MURI – hint, hint!

Publications

2009 Papers

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[8] R.M. Diestelhorst, S. Phillips, A. Appaswamy, A.K. Sutton, J.D. Cressler, J.A. Pellish, R.A. Reed, G. Vizkelethy, P.W. Marshall, H. Gustat, B. Heinemann, G.G. Fischer, D. Knoll, and B. Tillack, “Using Junction Isolation to Single-Event Radiation Harden a 200 GHz SiGe:C HBT Technology Containing No Deep Trenches,” *IEEE Transactions on Nuclear Science,* vol. 56, pp. 3402-3407, 2009.

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[17] R.M. Diestelhorst, S. Finn, L. Najafizadeh, D. Ma, P. Xi, C. Ulaganathan, J.D. Cressler, B. Blalock, F. Dai, A. Mantooth, L. Del Castillo, M. Mojarradi, and R. Berger, "A Monolithic, Wide-Temperature, Charge Amplification Channel for Piezoelectric Sensing Applications in Extreme Environments," *Proceedings of the 2010 IEEE Aerospace Conference*, pp. 1-9 (on CD ROM), 2010.

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[20] S. J. Horst, S. D. Phillips, P. Saha, J. D. Cressler, D. McMorrow, P. Marshall, H. Gustat, B. Heinemann, G. G. Fisher, D. Knoll, and B. Tillack, “An Investigation of Single-Event Transients in Complementary SiGe BiCMOS Resonant Tank Oscillators,” *IEEE Nuclear and Space Radiation Effects Conference* July 2010, accepted.

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