Radiation Effects in SiGe Devices

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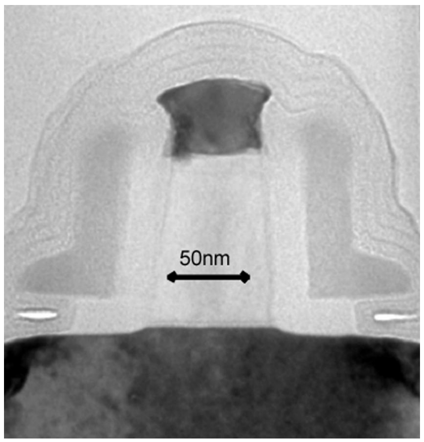
MURI Review: Vanderbilt University, Nashville, TN
June 10-11, 2009

Outline

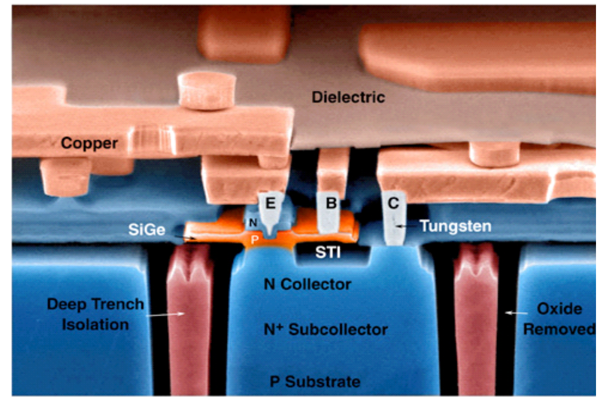
- Some Reminders from the SiGe World
- Some New TID Effects in SiGe
- Progress in SEE for Bulk SiGe HBT Platforms
  - device vs. circuit level RHBD
  - impact of deep trench isolation on SEE
  - some new RHBD approaches
  - the path to understanding device-level transients
  - new results on circuit-level transient phenomena
- Radiation Effects in Advanced Si/SiGe FETs
  - p-channel SiGe MODFETs
- Progress / Plans

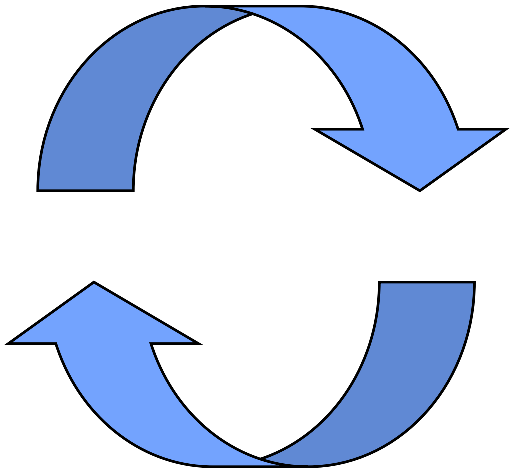
Strain Engineering in Si

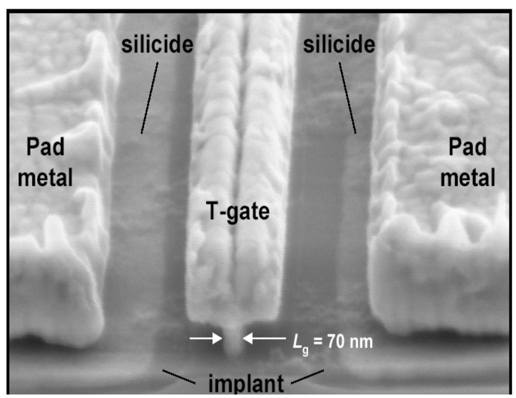
Strained Si CMOS



SiGe HBTs







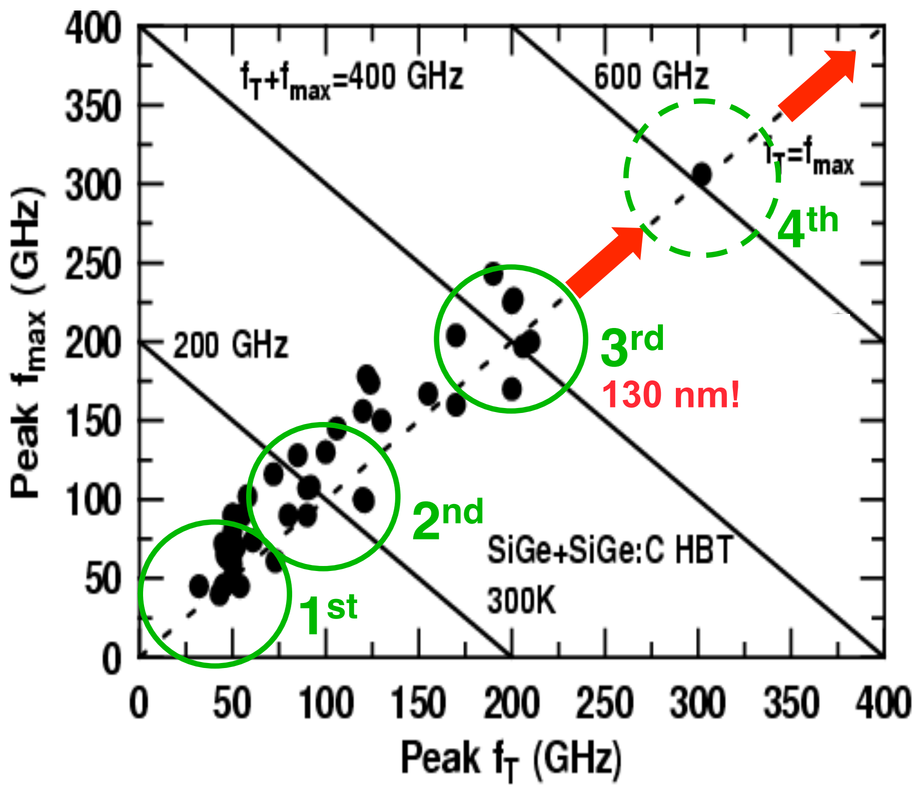
SiGe MODFETs

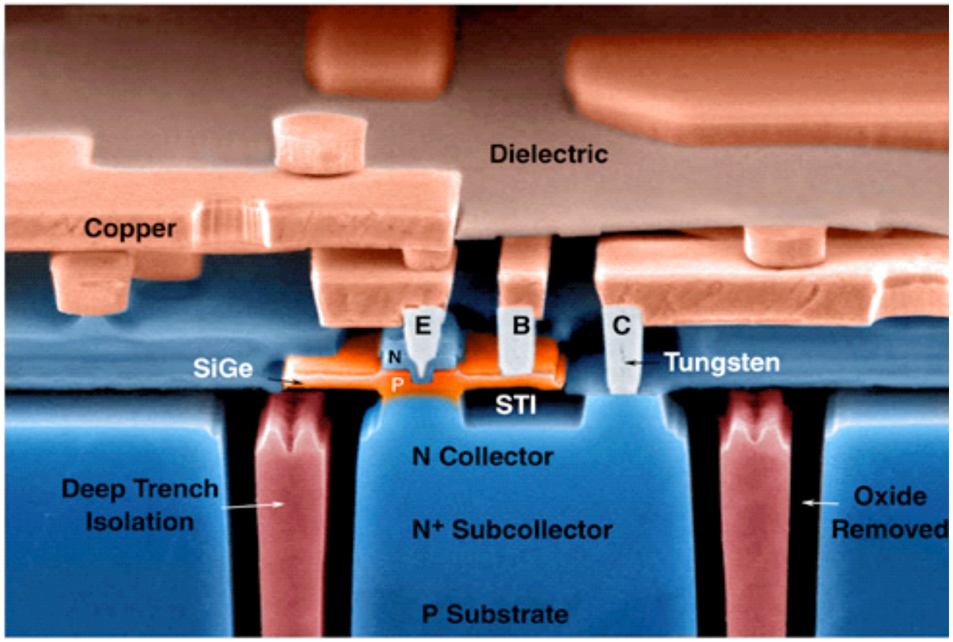
All Are:
Strain-Enhanced
Si-based Transistors

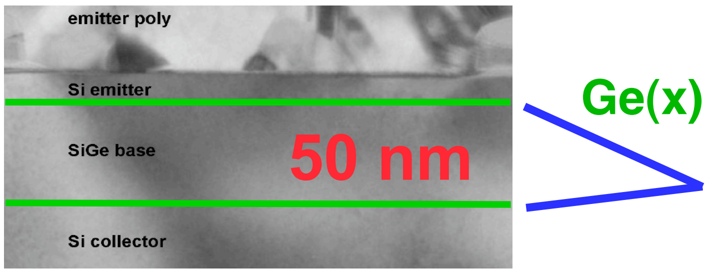
Close Cousins!

SiGe Success Story

- SiGe = SiGe HBT + Si CMOS for Highly Integrated Solutions
- Rapid Generational Evolution (full SiGe BiCMOS)
- Significant In-roads in High-speed Communications ICs







SiGe = III-V Speed + Si Manufacturing

Win-Win!

New SiGe Opportunities

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- **SiGe for Radar Systems**

  - single chip T/R for pha

  arrays, space-based radar (2-10 GHz & up)

  - automotive radar (24, 77 GHz)

- **SiGe for Millimeter-wave Communications**

  - Gb/s short range wireless links (60, 94 GHz)

  - cognitive radio / frequency-agile WLAN / 100 Gb Ethernet

- **SiGe for THz Sensing, Imaging, and Communications**

  - imaging / radar systems, diagnostics, comm (94 GHz, 100-300 GHz)

- **SiGe for Analog Applications**

  - the emerging role of C-SiGe (npn + pnp) + **data conversion** (ADC limits)

- **SiGe for Extreme Environment Electronics**

  - extreme temperatures (4K to 300C) + **radiation** (e.g., space systems)

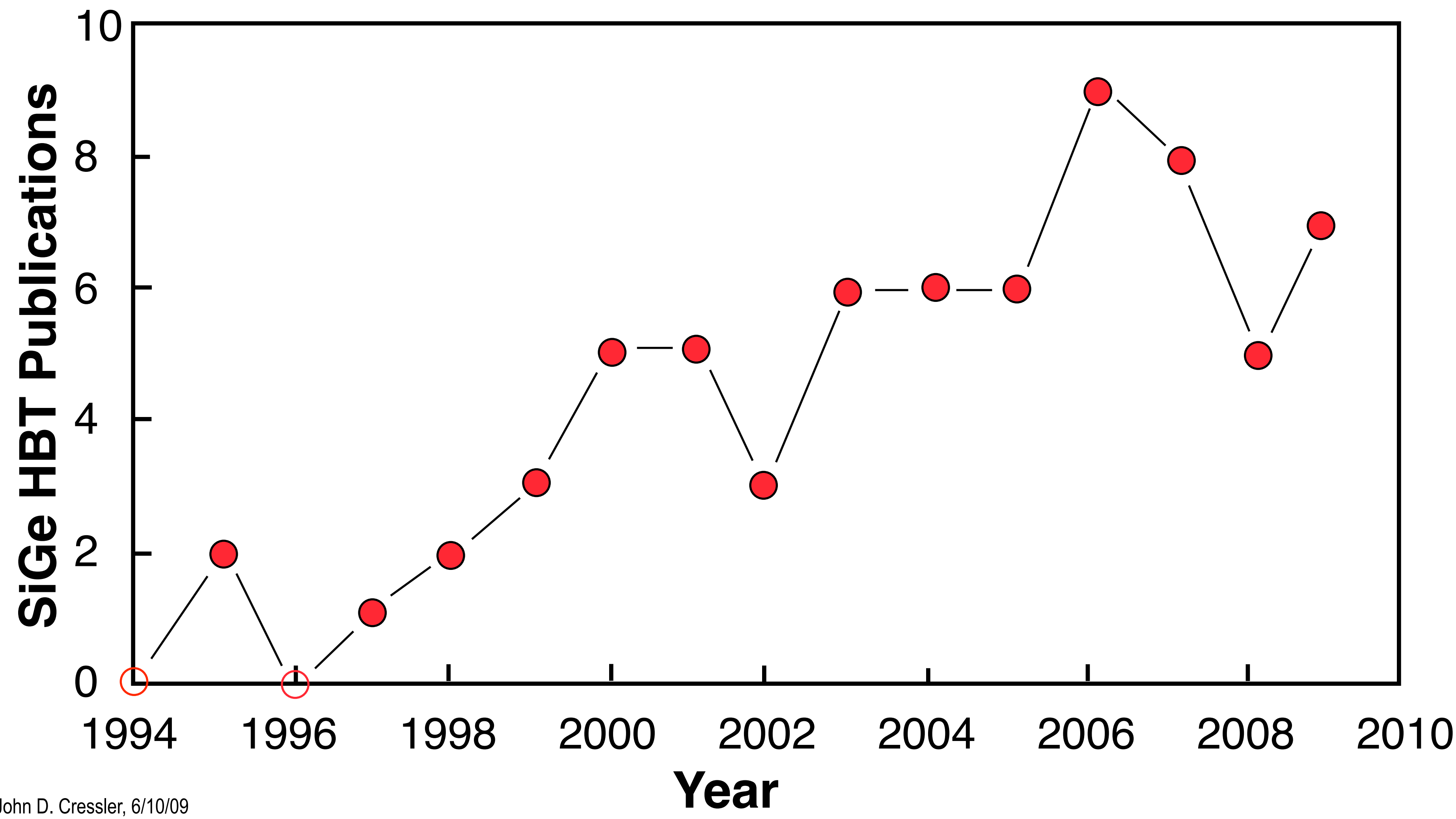
- **SiGe for Electronic Warfare**

  - extreme wideband transceivers (20 MHz – 20 GHz)

  - dynamic range enhanced receivers

SiGe HBTs at NSREC

Total SiGe HBT Papers @ NSREC:
1995-2009 = 68



TID Effects: Summary

SiGe HBTs are Inherently Tolerant to TID
… as Fabricated!

- **Minimal damage to <u>devices + circuits</u>** (all sources; no ELDRS)
- **Typically multi-Mrad capability, <u>as built</u>**
- **TID-induced damage improves with SiGe technology scaling**
- **No *ac* performance degradation across all SiGe generations**
- **SiGe HBTs much less sensitive to bias effects than CMOS**
- **SiGe HBTs function after 100+ Mrad exposure**
- **Reduced TID damage at cryogenic temperatures**

Lots of Interesting Physics …

The Story is <u>NOT</u> Over …

TID Test Protocols

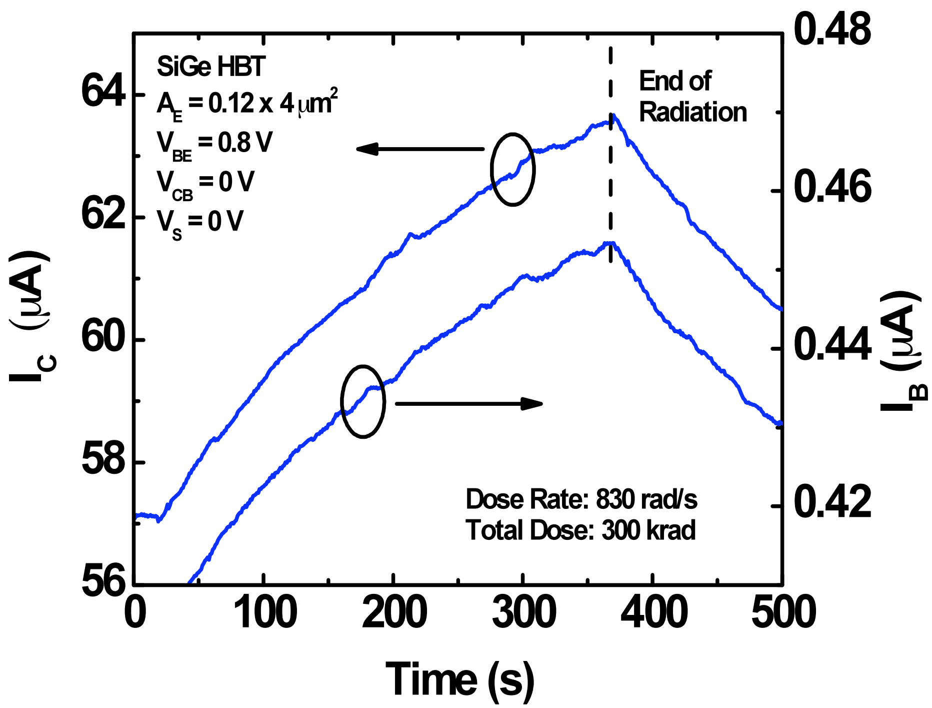
- **Standard TID Test Path:**

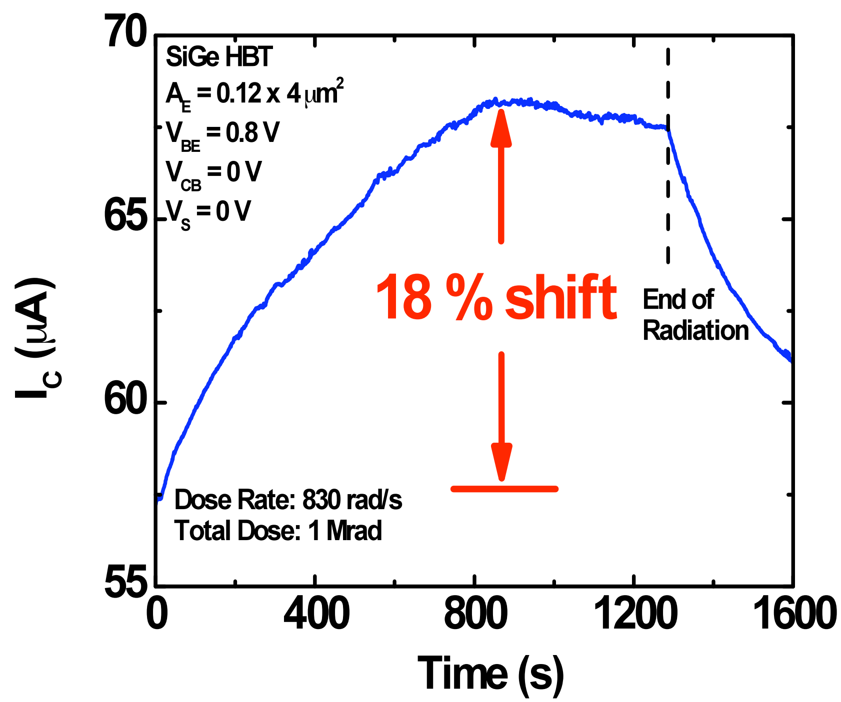
  1) measure pre-rad ⇨ 2) expose to TID ⇨ 3) remeasure, repeat

  Q: What happens to the devices between steps 2 and 3?

- **I_C and I_B Bias Shift Observed as a Function of Irradiation Time**

  Q: Impact on analog & RF circuits? Impact on reliability?





Outline

- Some Reminders from the SiGe World
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- **Progress in SEE for Bulk SiGe HBT Platforms**
  - transistor-level vs. circuit-level RHBD
  - impact of deep trench isolation on SEE
  - some new RHBD approaches
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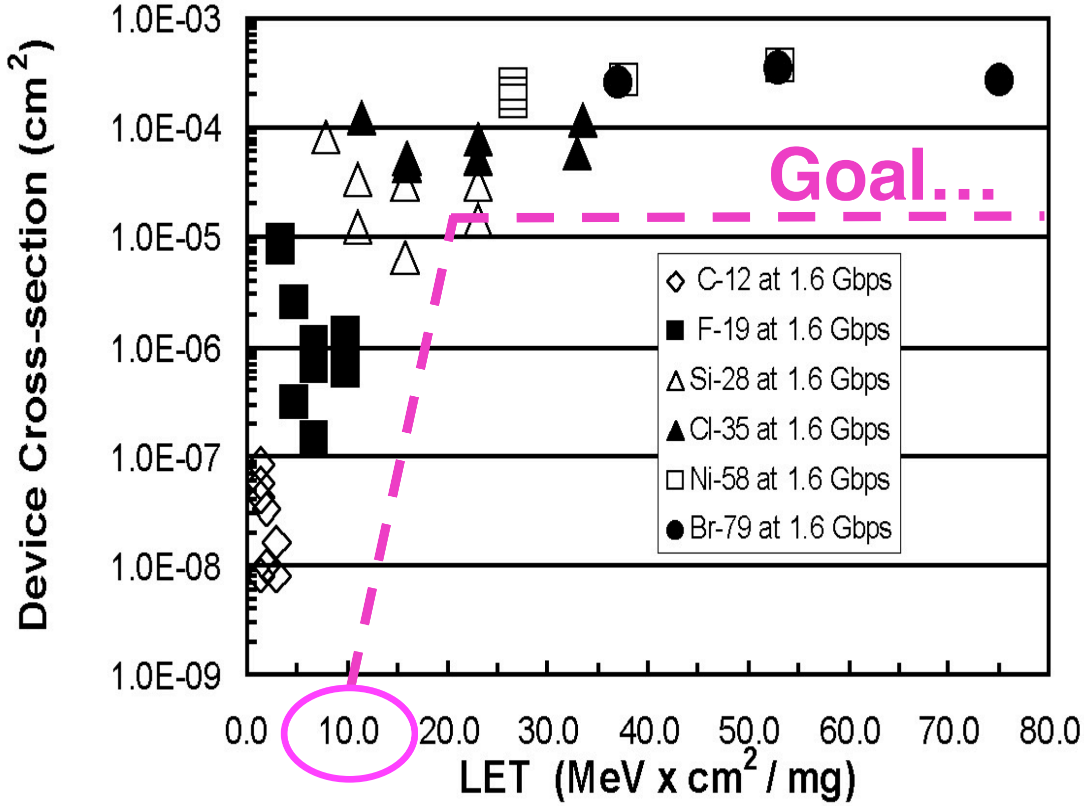
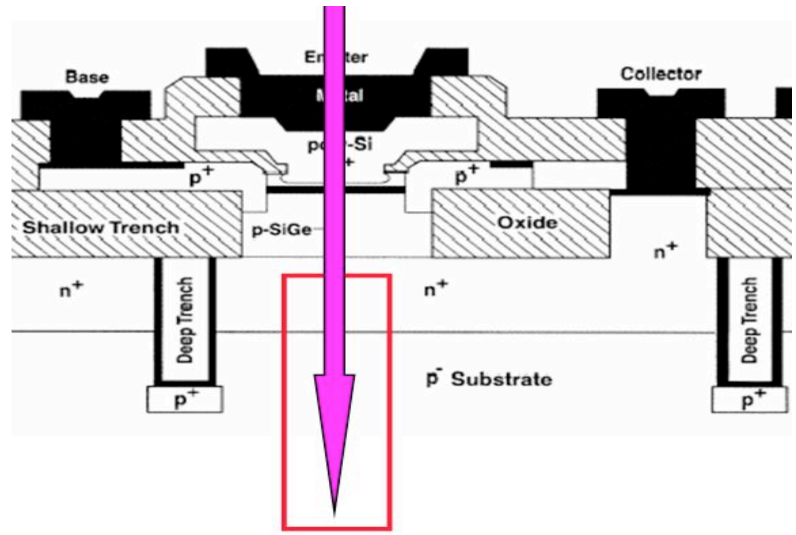
Single Event Effects

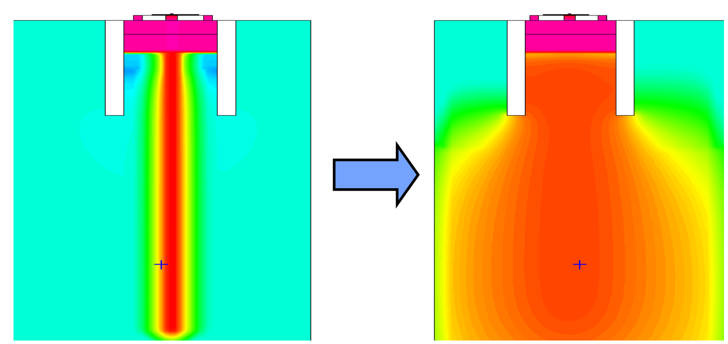
- **Observed SEU Sensitivity in SiGe HBT Shift Registers**
  - low LET threshold + high saturated cross-section **(bad news!)**



P. Marshall *et al.*, *IEEE TNS*, 47, p. 2669, 2000

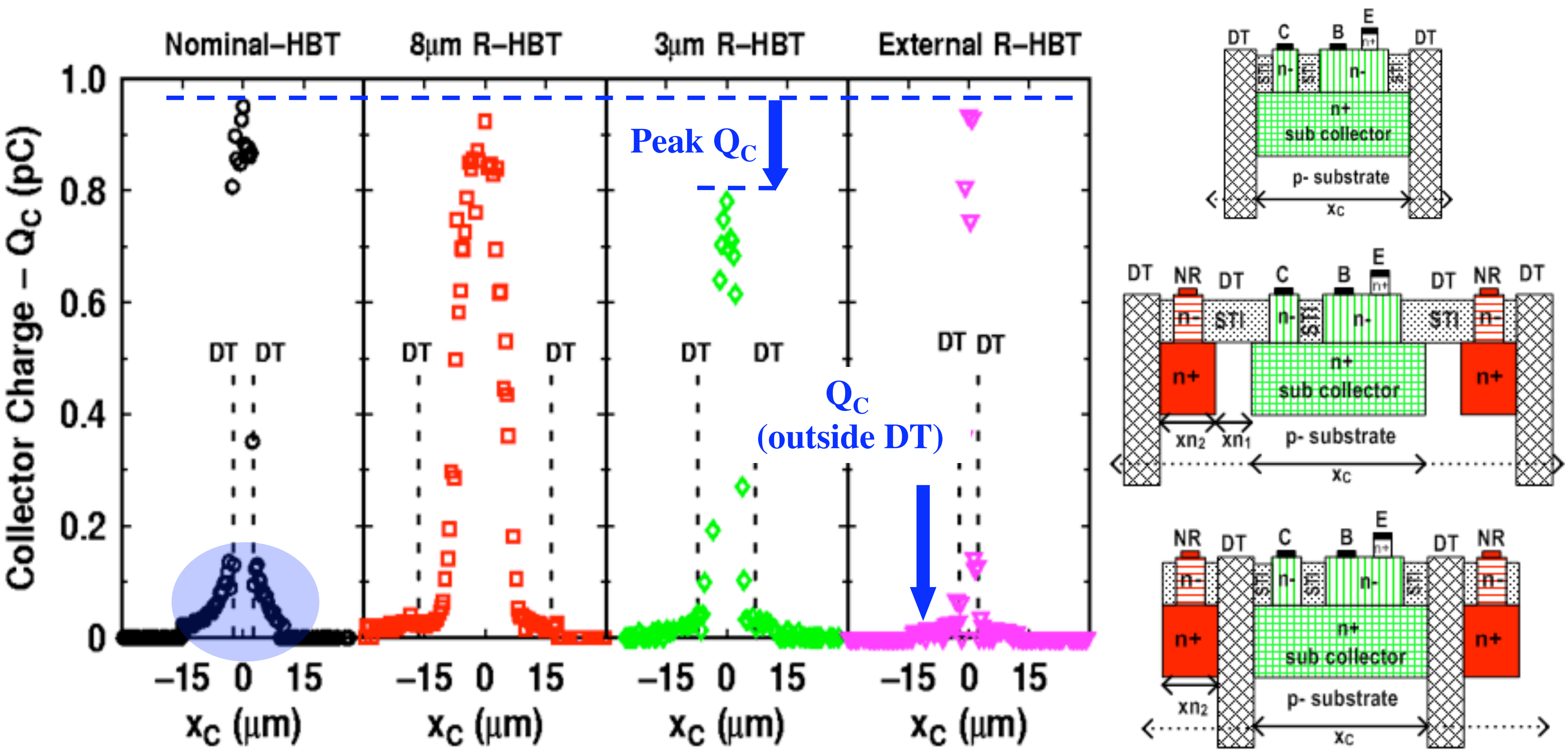
heavy ion





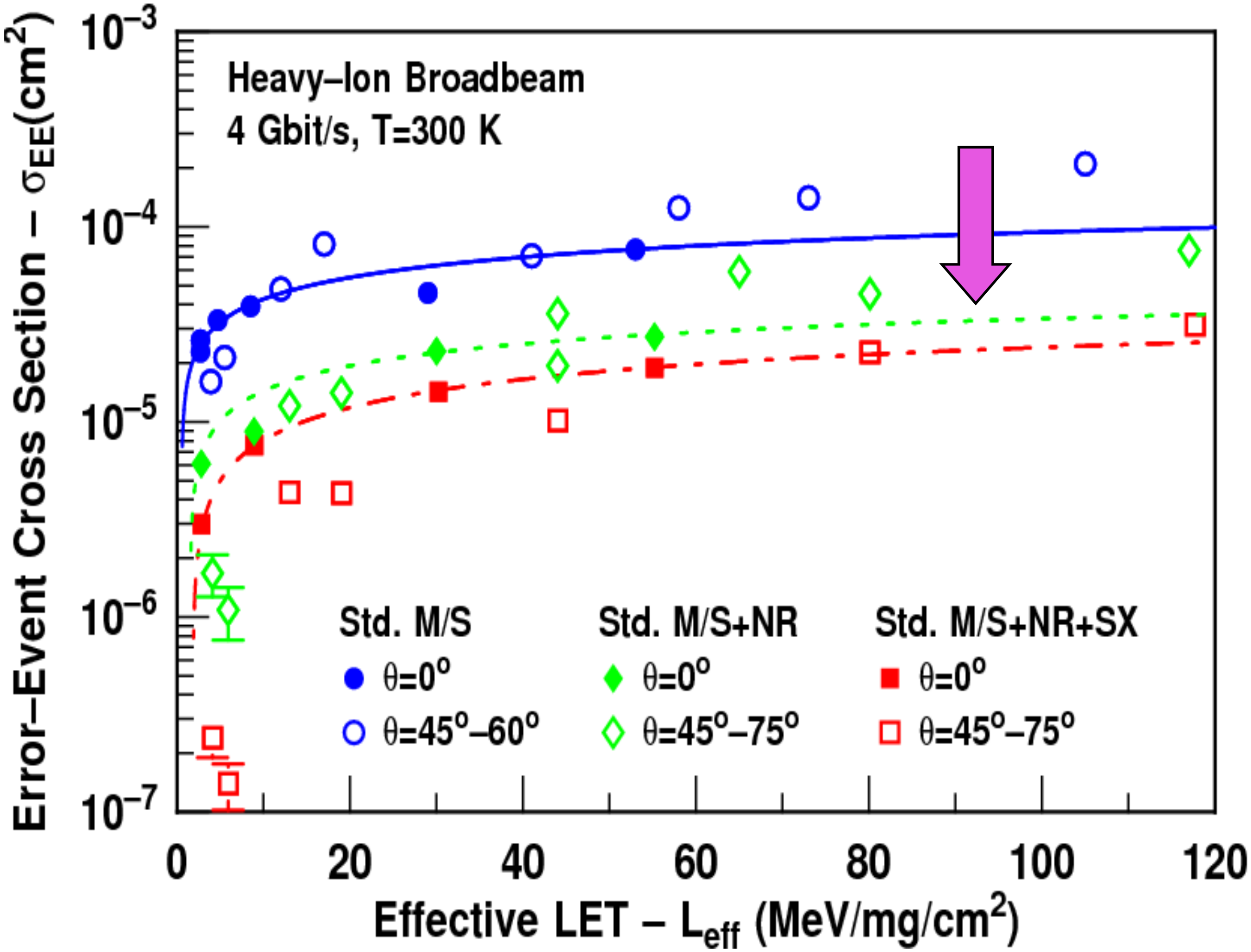
Tx-level RHBD Games

- **5-probe IBICC Measurement** (Sandia National Lab)
  - 36 MeV O_2 ions, LET= 7 MeV-cm^2/mg, 25 μm Si range
  - 100 μm^2 scan, V_C=V_B=V_E=0 V, V_{SX} = -4 V, V_{NR} = 0 - 4V



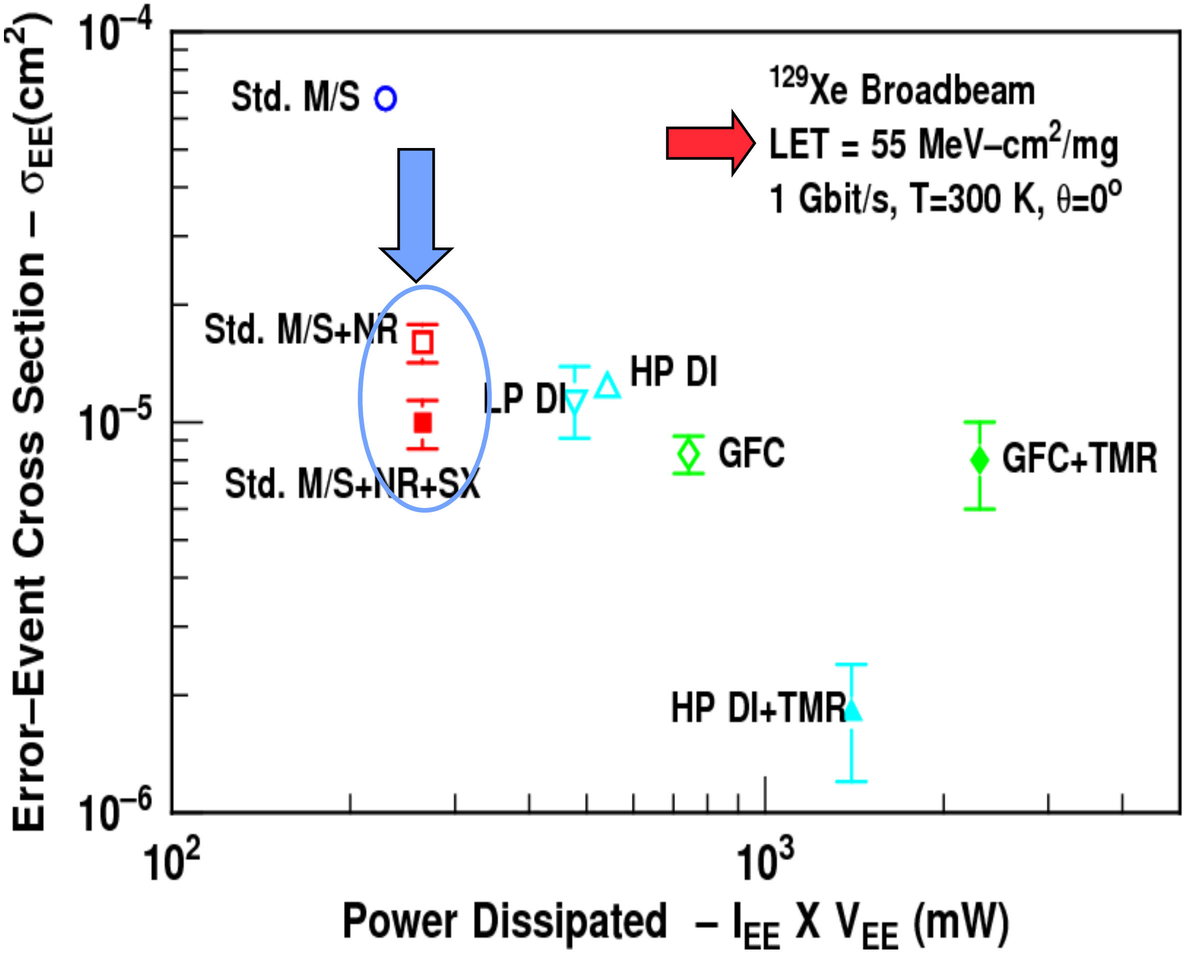
Impact of Tx RHBD

- N-ring Gives Reduction in σ_{SAT} but no Change in L_{TH}
- Substrate Contact Placement Seems to Matter



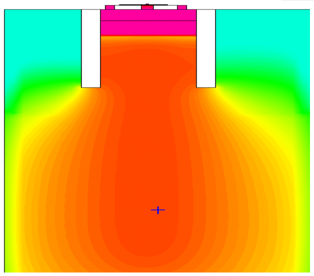
Transistor vs. Circuit RHBD

- Tx-level RHBD Offers Similar Reduction in σ_{SAT} *vs.* Circuit RHBD
- Minimal Increase in Circuit Area and Power Dissipation
- Circuit-level TMR Techniques Still Offer the Largest Mitigation

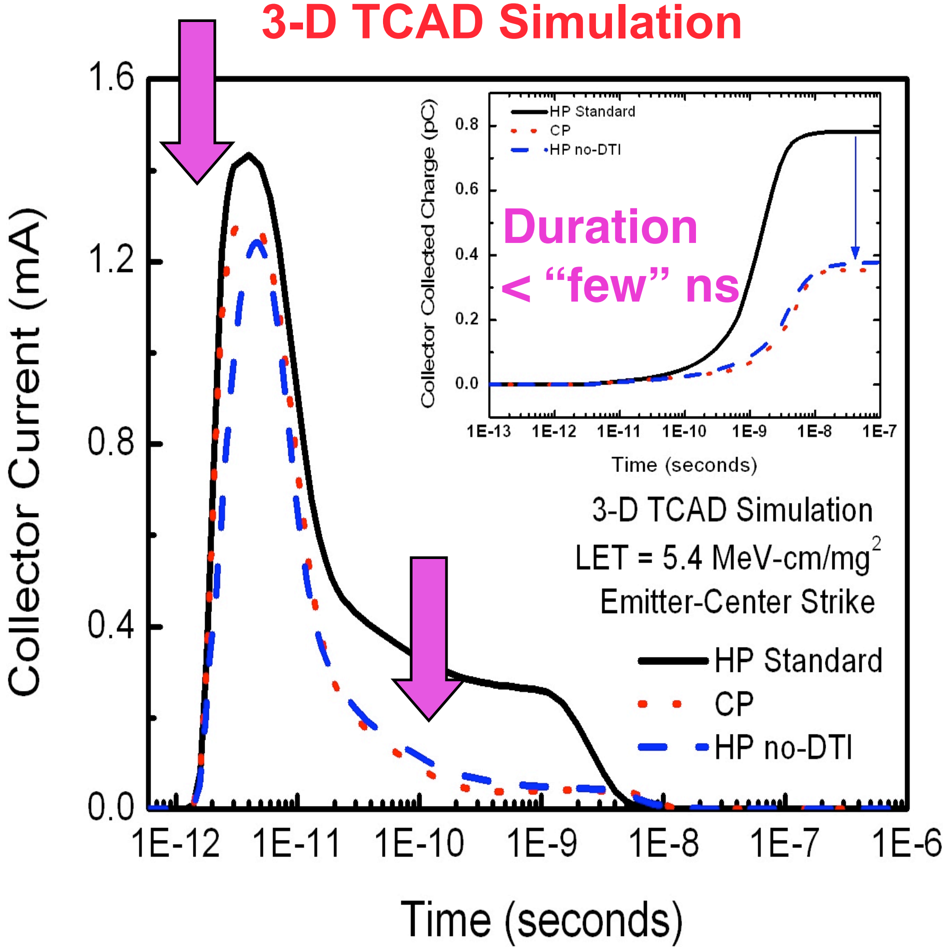


Deep Trench Effects

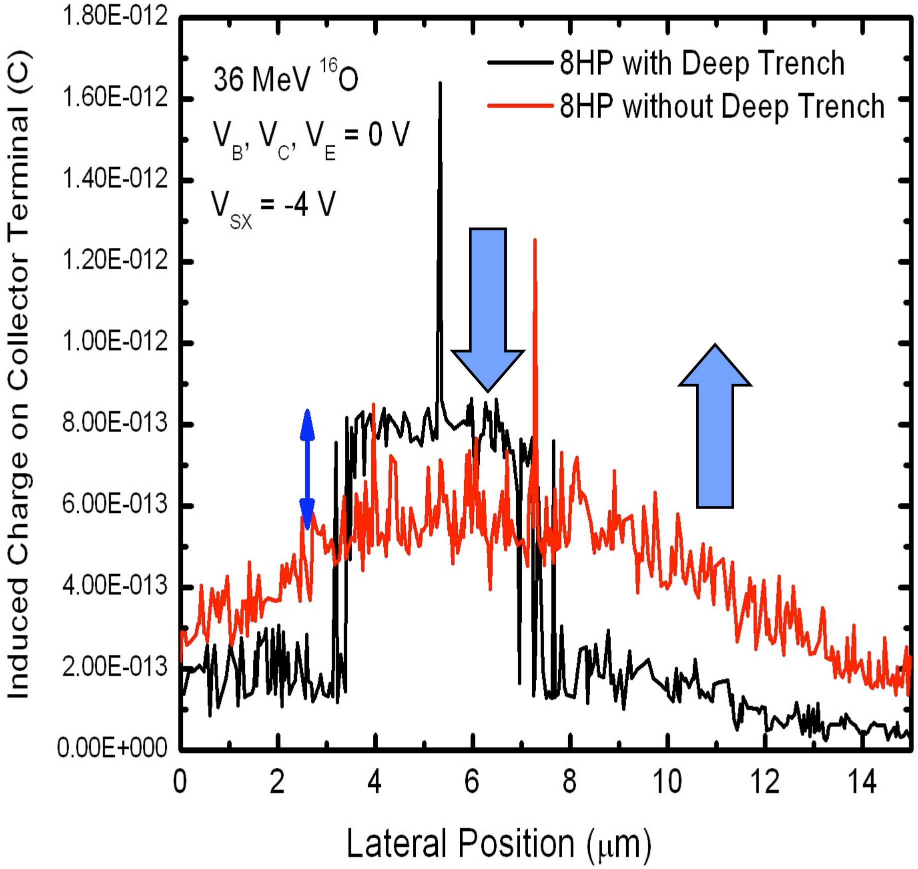
Q: Does Deep Trench Impact SEE Response?
Q: Can We Exploit This for Hardening?



3-D TCAD Simulation

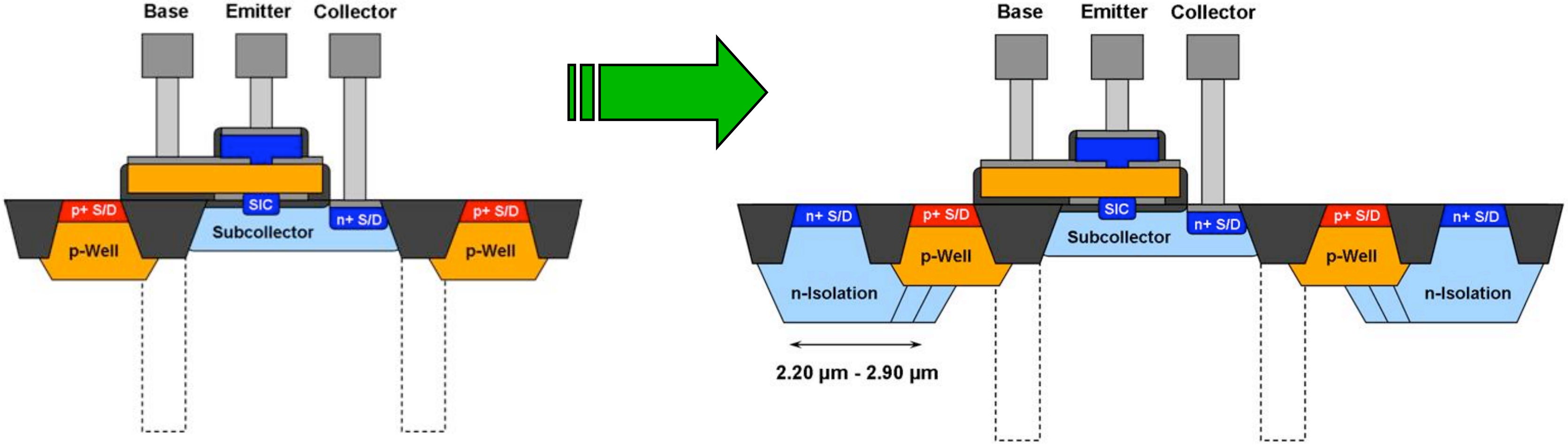


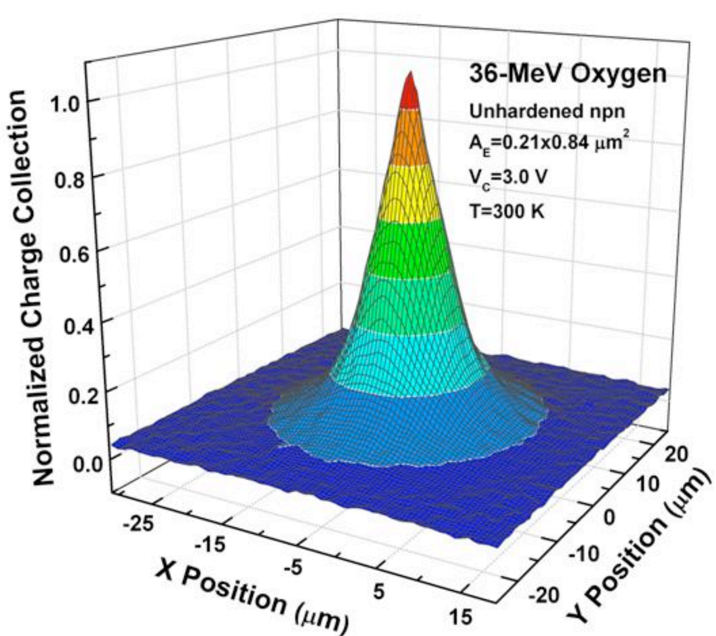
Microbeam Data

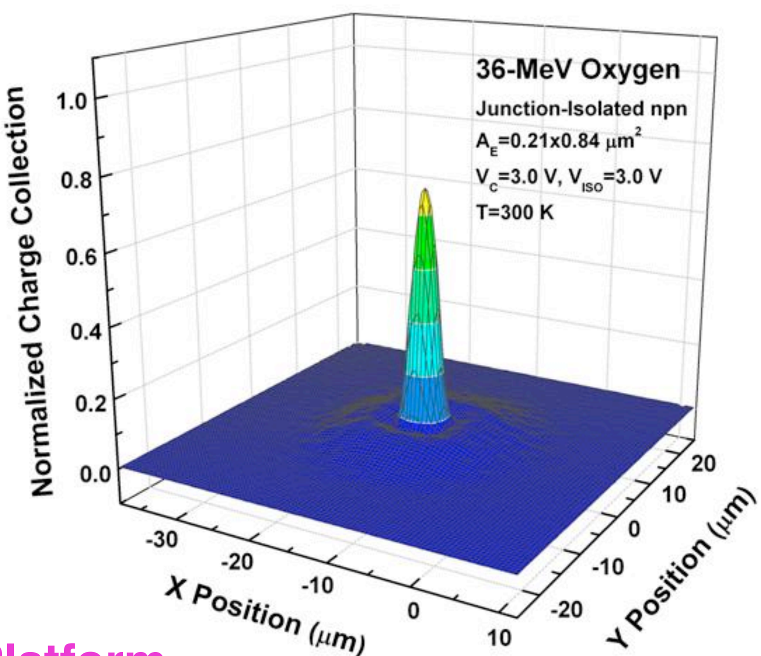


John D. Cressler, 6/10/09

Junction-Based RHBD

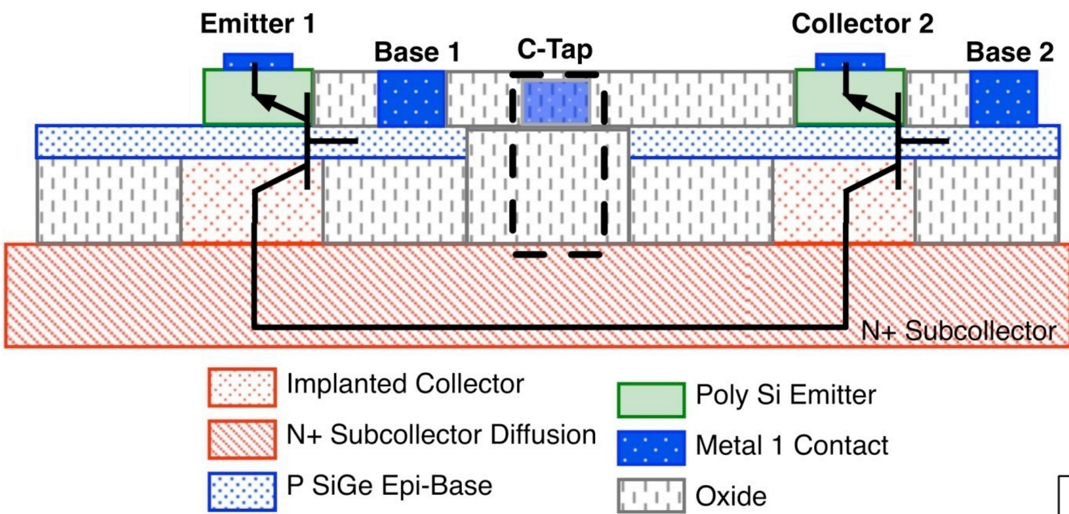


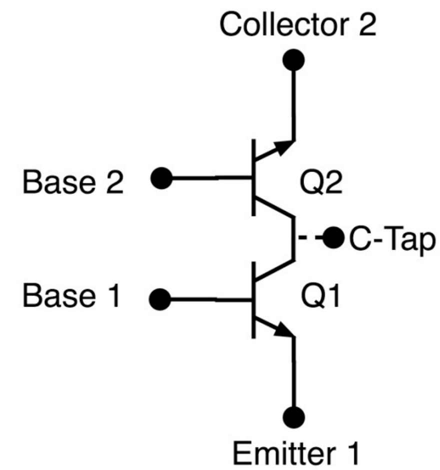


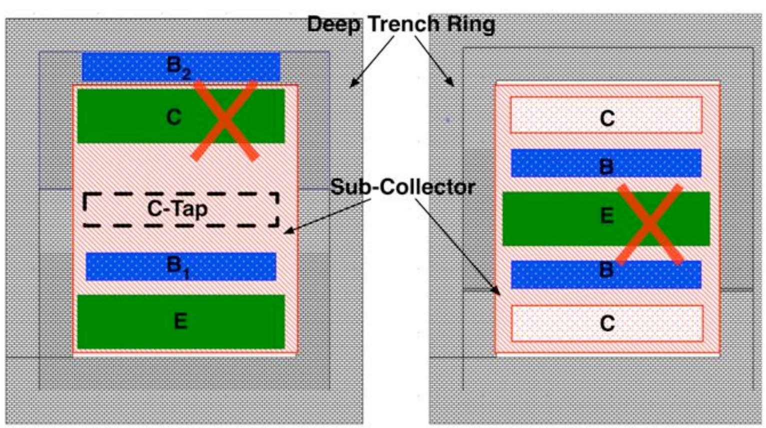


IHP SiGe Platform

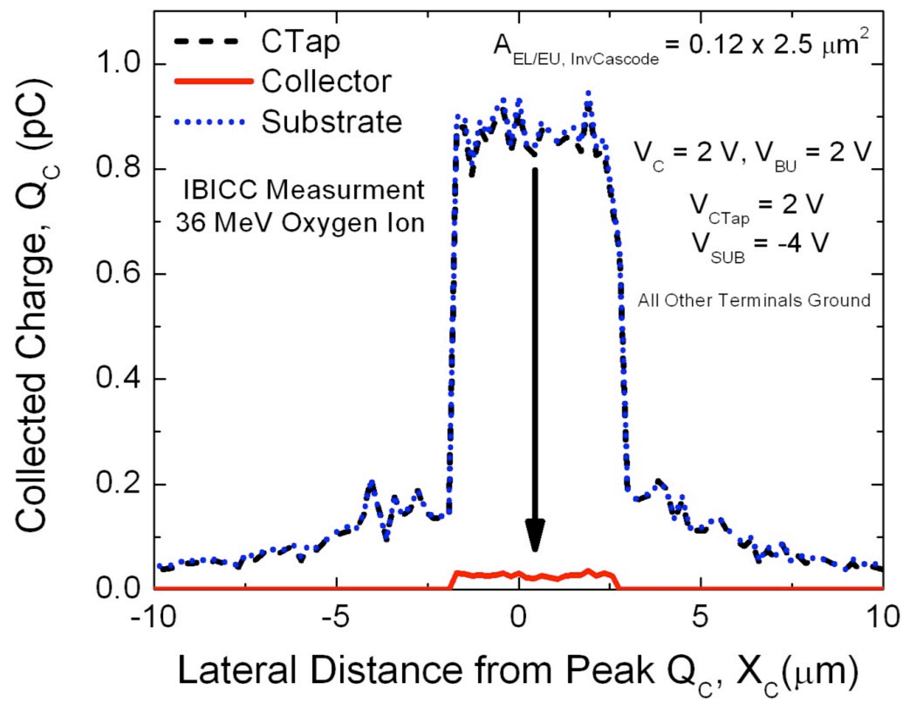
Inverse Cascode HBT



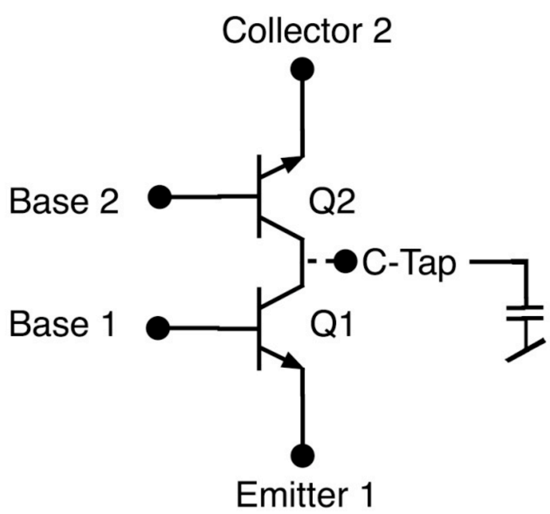


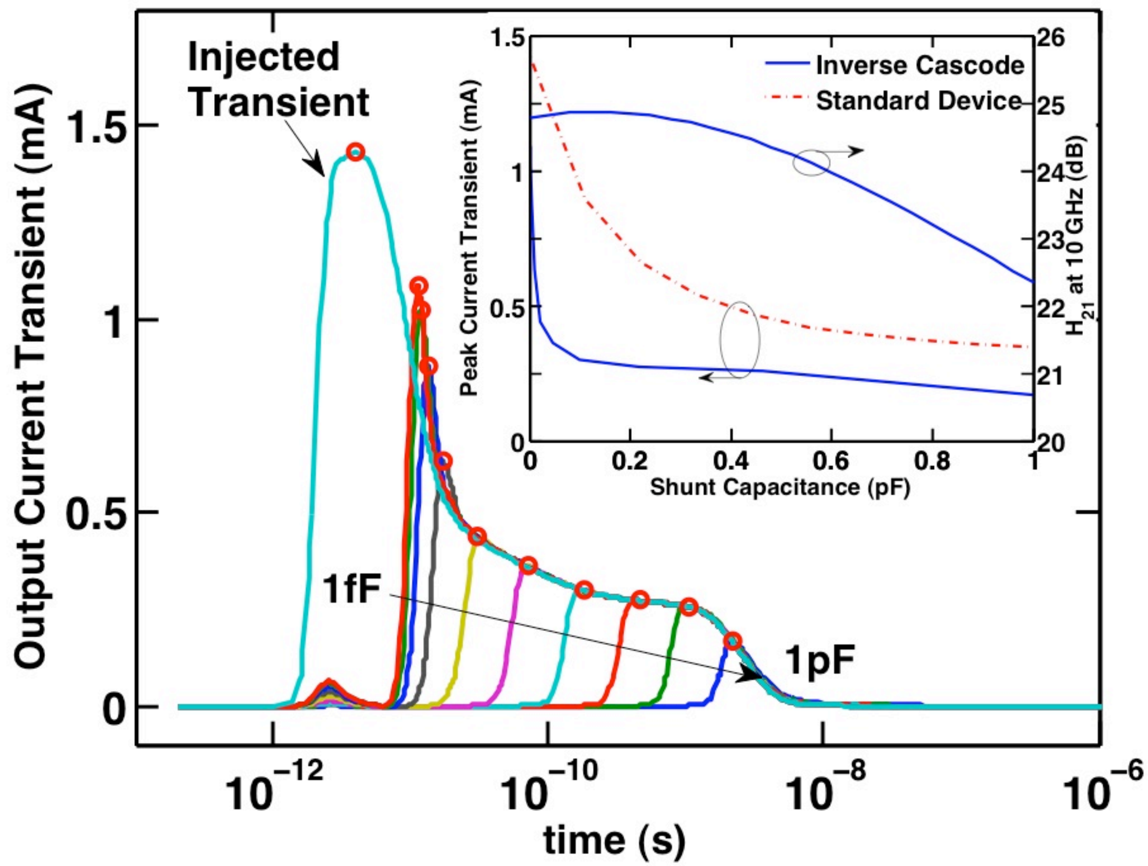


(a) Cascoded Inverse SiGe HBT (b) Standard SiGe HBT



Optimized Structure





- **Cadence Simulations of Capacitive Shunt on C-Tap Node**
  - **- larger SEE mitigation with larger capacitance**
  - **- acceptable losses for amount of mitigation achieved (multi-Gb/s)**

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Georgia Institute of Technology

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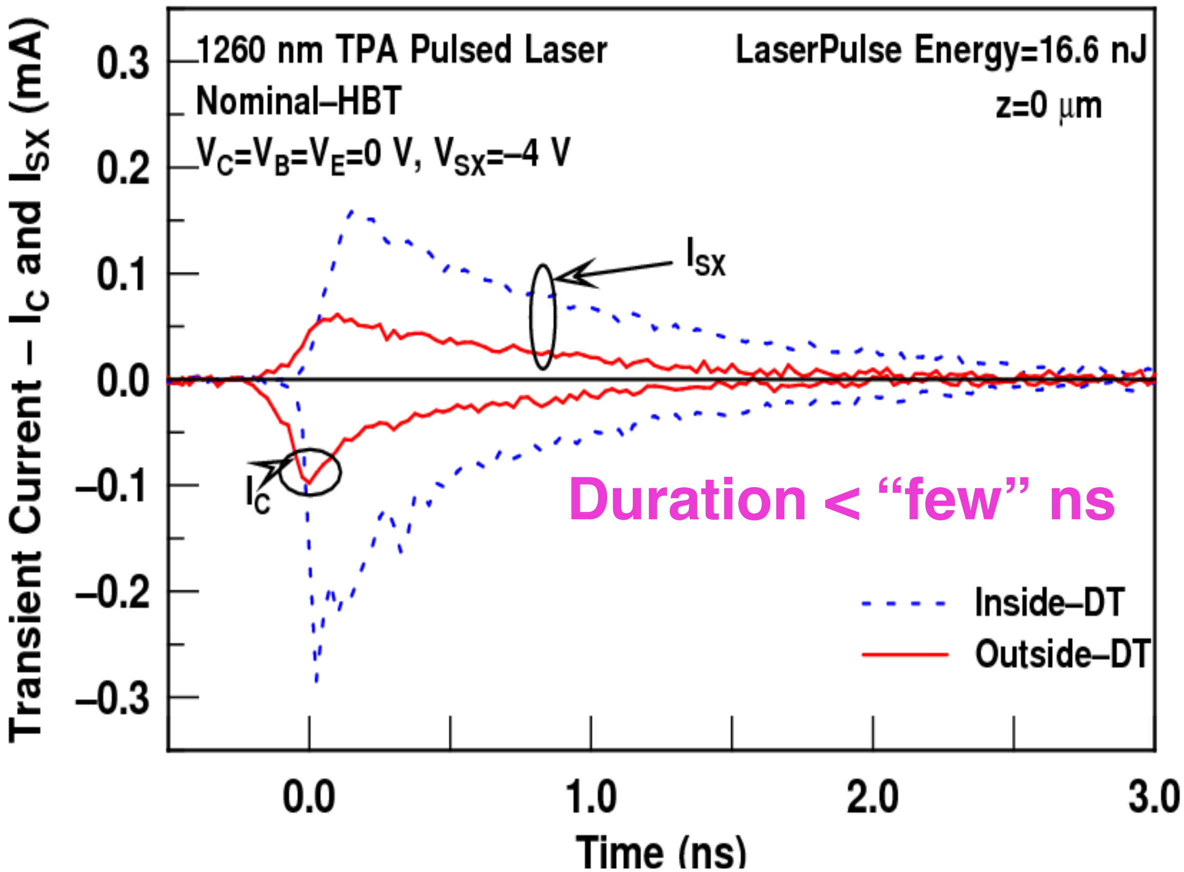
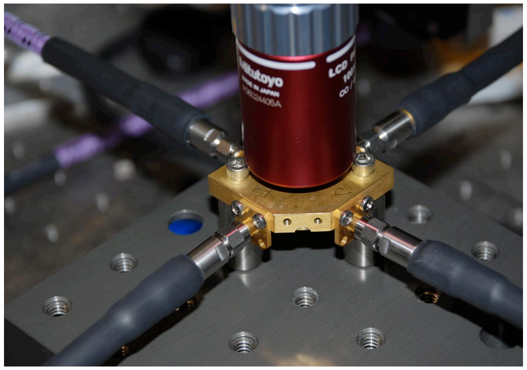
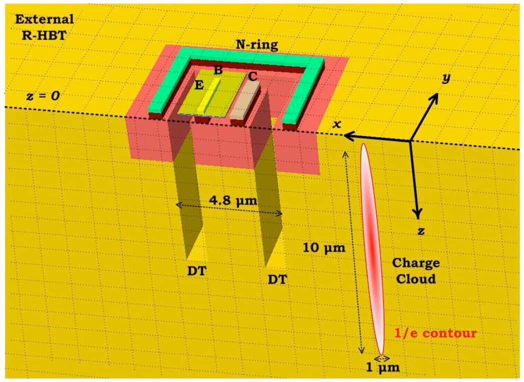
SET in SiGe HBTs (TPA)

- **Use Two-Photon Absorption to Capture Current Transients**
  - needed for fundamental understanding + TCAD calibration
  - results consistent with heavy-ion microbeam



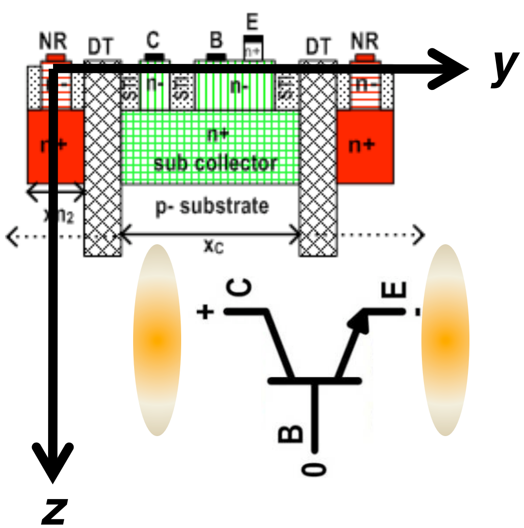


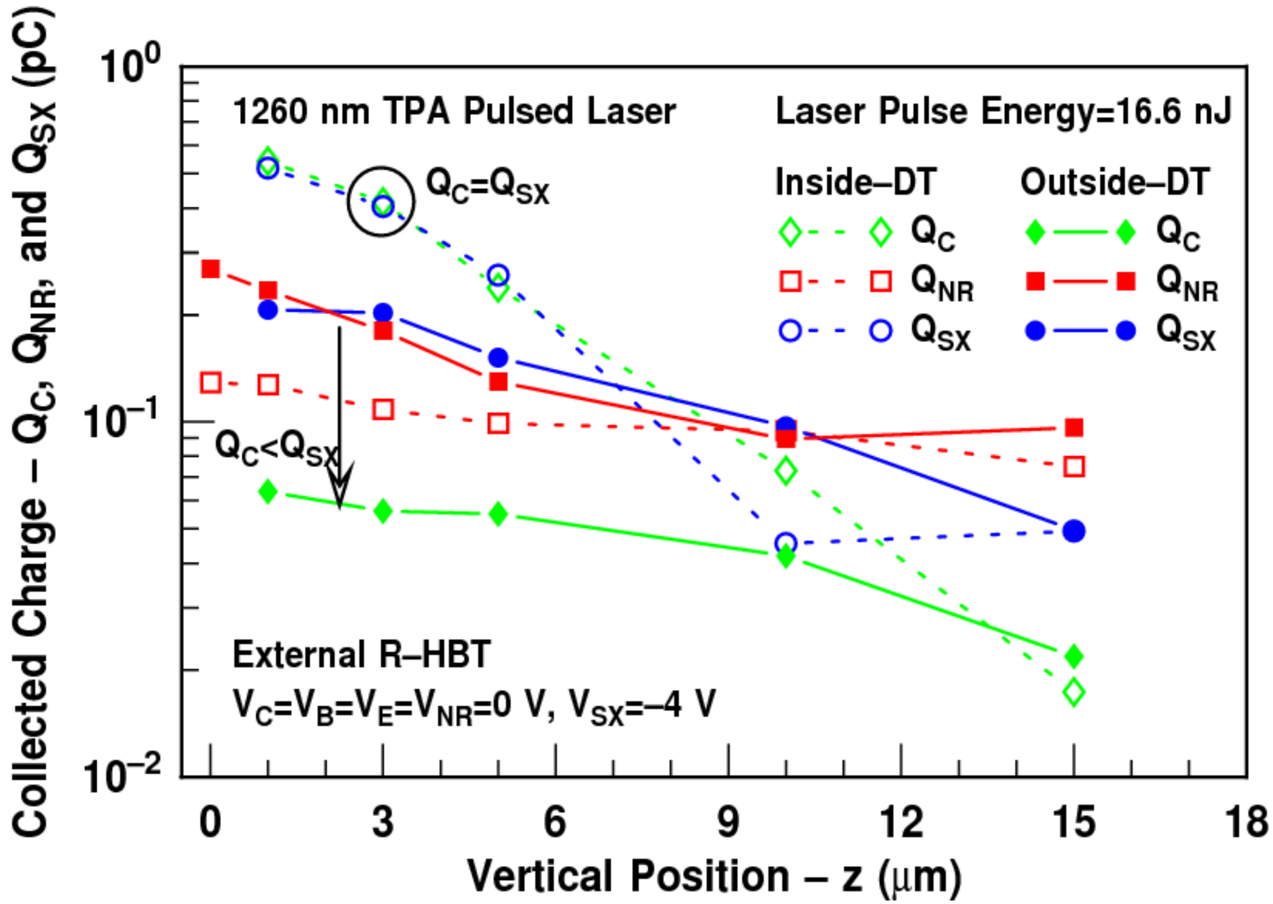


Collaboration with NRL, NASA-NEPP, DTRA, and Vanderbilt teams

Lateral Transient Profile

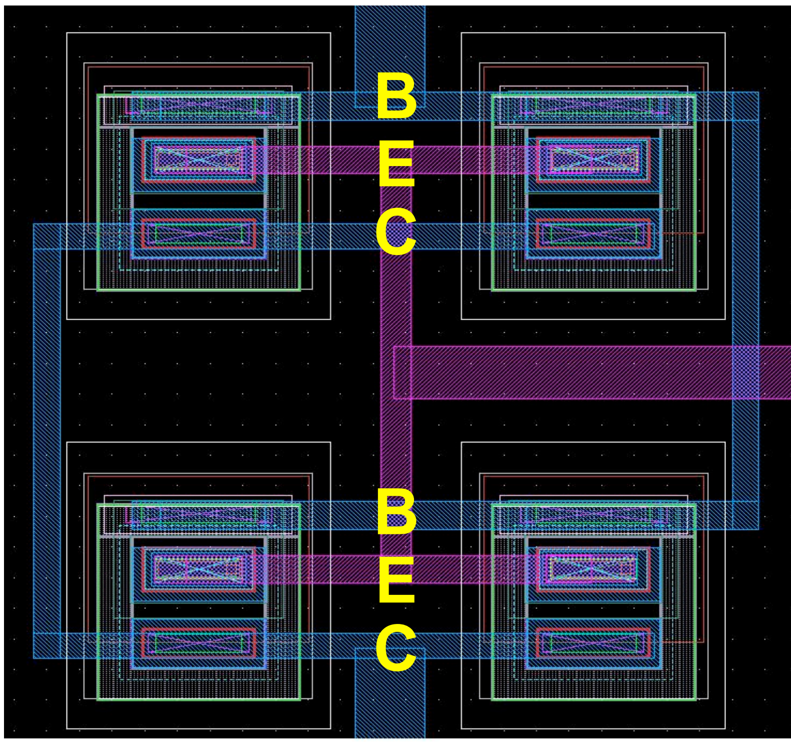
- Positive-going I_{NR} Decreases with Depth Inside the DT
- Larger Z → Focal Spot Further from the Parasitic BJT Structure
- Negative-going I_{NR} Decreases with Depth Outside the DT
- Inside the DT $Q_C \approx Q_{SX}$, and Outside the DT $Q_{NR} \approx Q_{SX}$

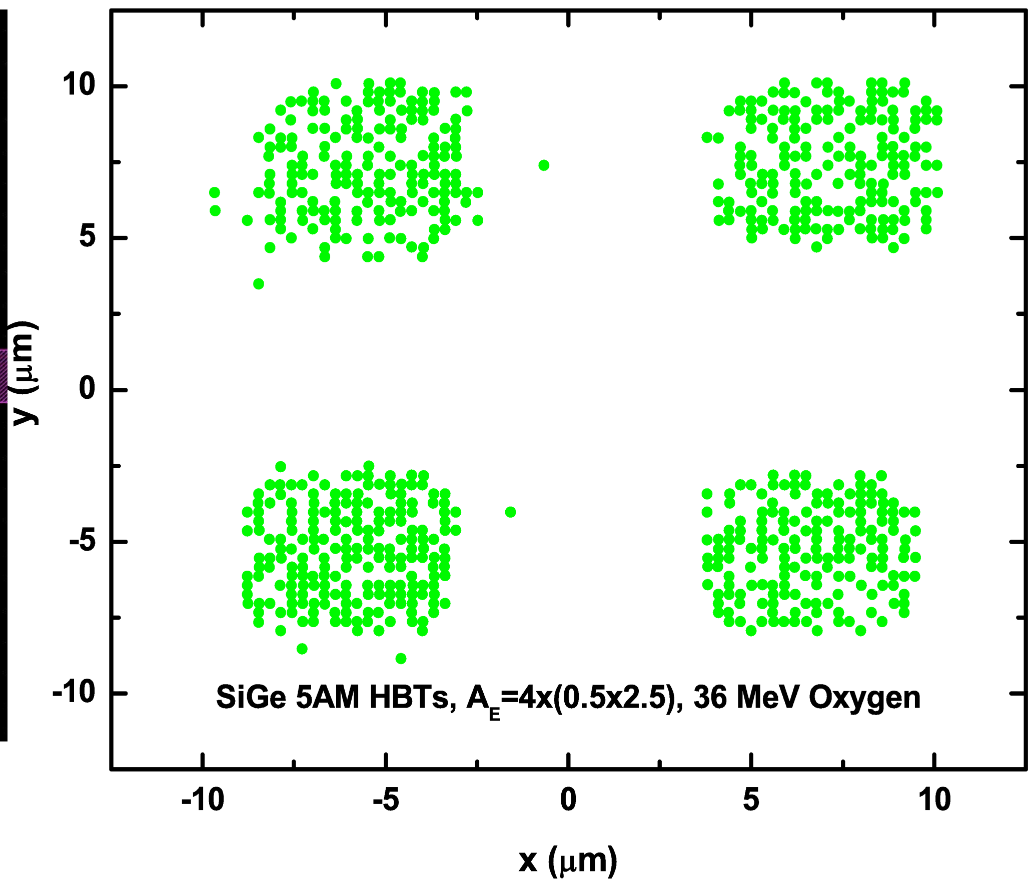




SETs (Ion Microbeam)

- Four Transistors in Parallel Irradiated With 36 MeV Oxygen Ions
- Transients Observed and Captured Inside DT Area for All Four

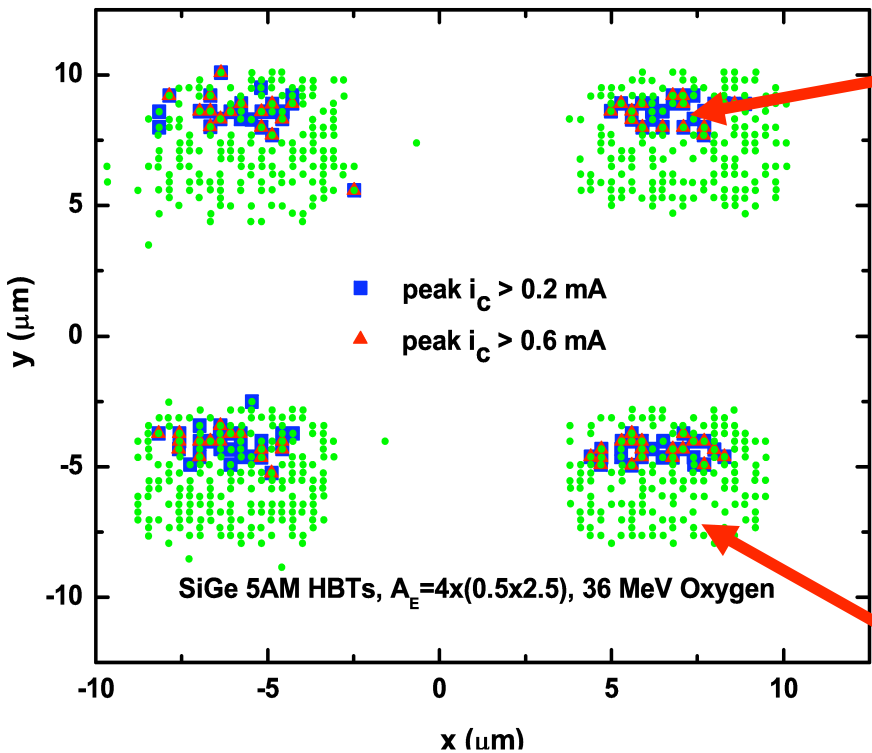


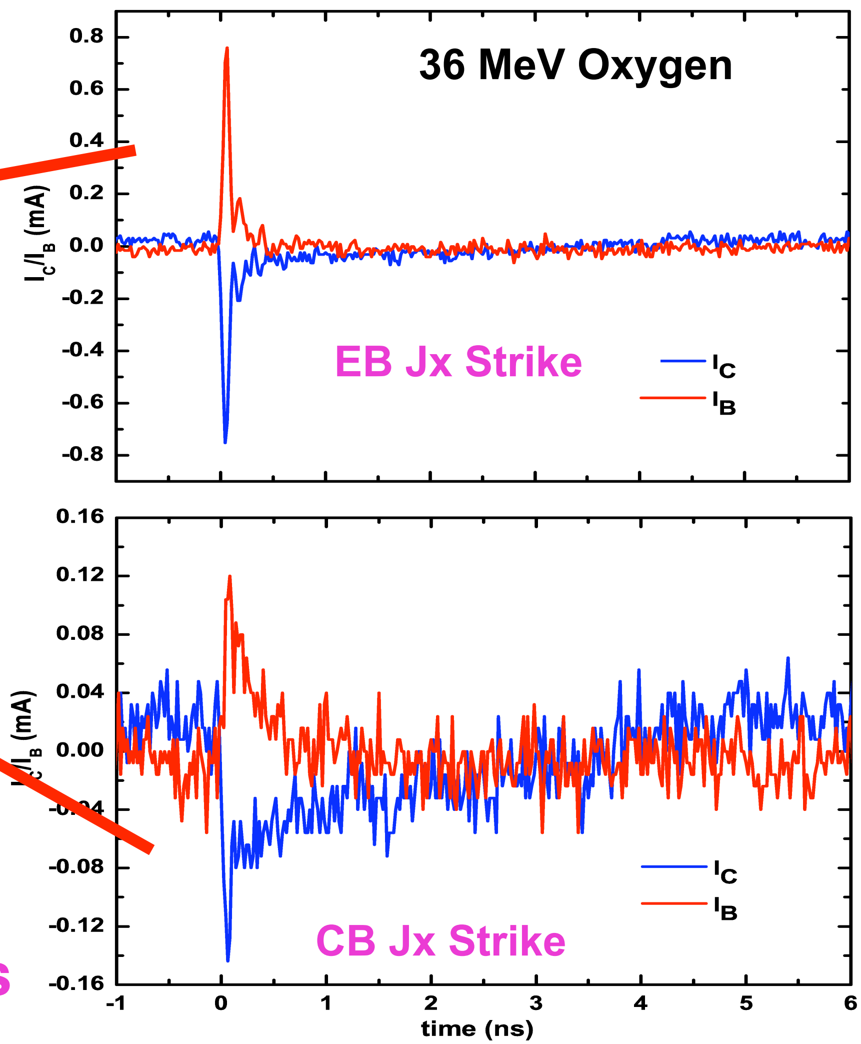


Collaboration with Sandia, NASA-NEPP, DTRA, and Vanderbilt teams

SET in SiGe HBTs

- **Emitter Ion Strikes Show the Largest Transient Amplitudes**
- **Collector-Base Strikes Have Small Transient Amplitudes**



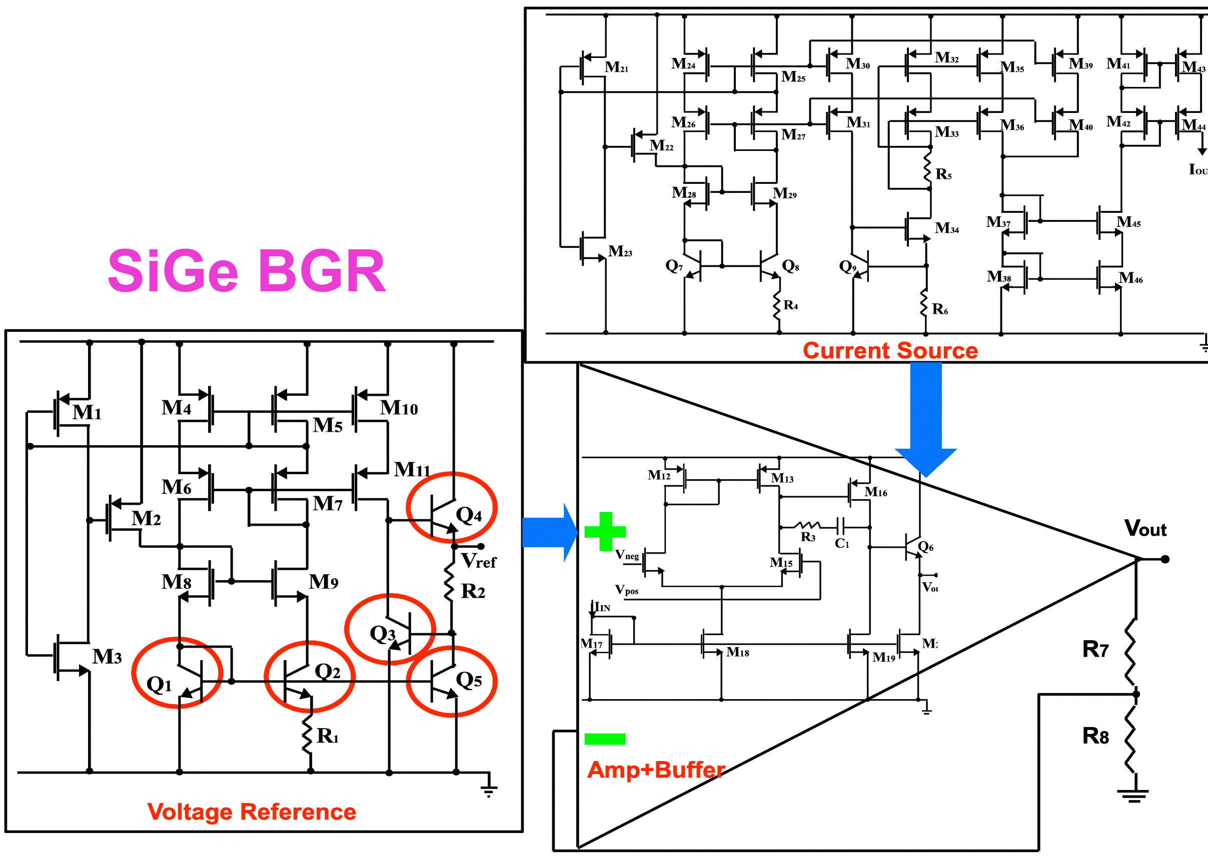


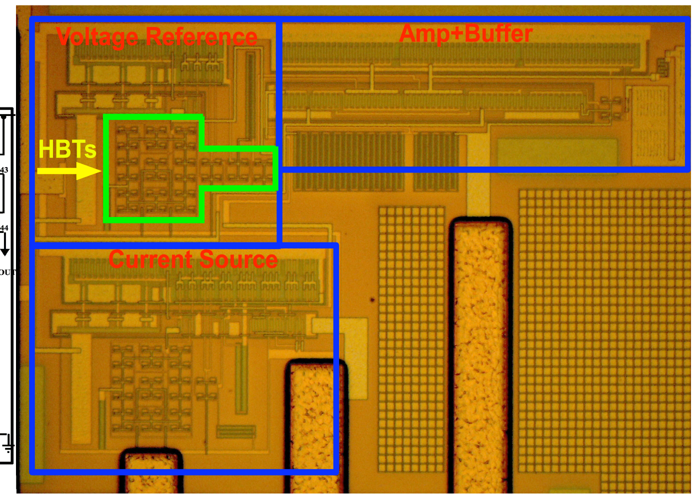
Duration < "few" ns

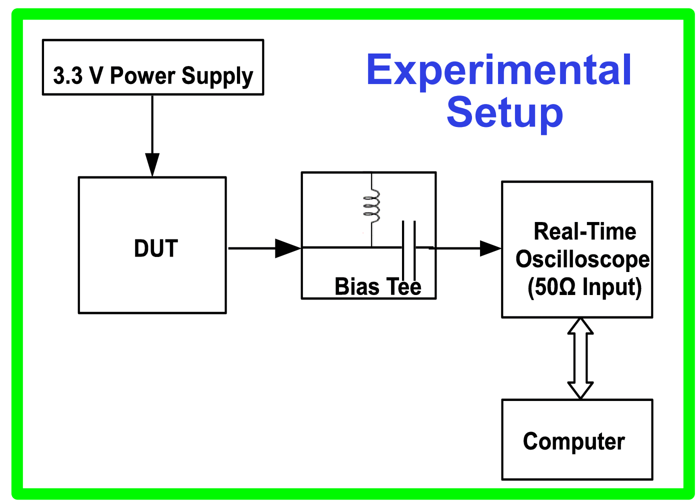
SET in SiGe Circuits

- A Bandgap Voltage Reference Used Inside a Regulator Circuit
- SiGe HBTs in the BGR Irradiated With 36 MeV Oxygen Ions

SiGe BGR

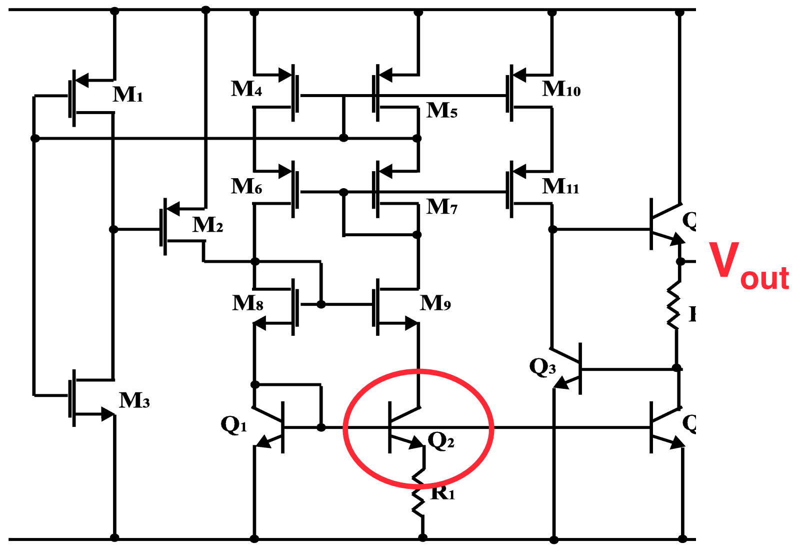


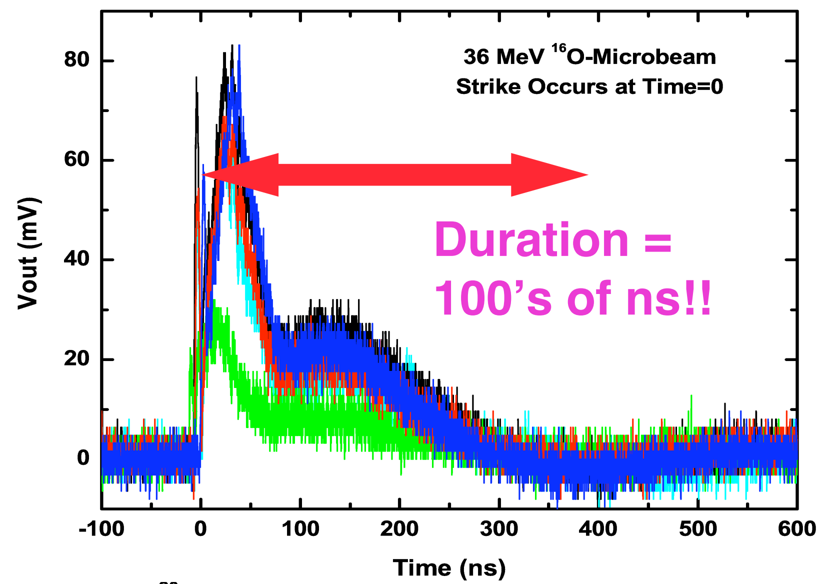


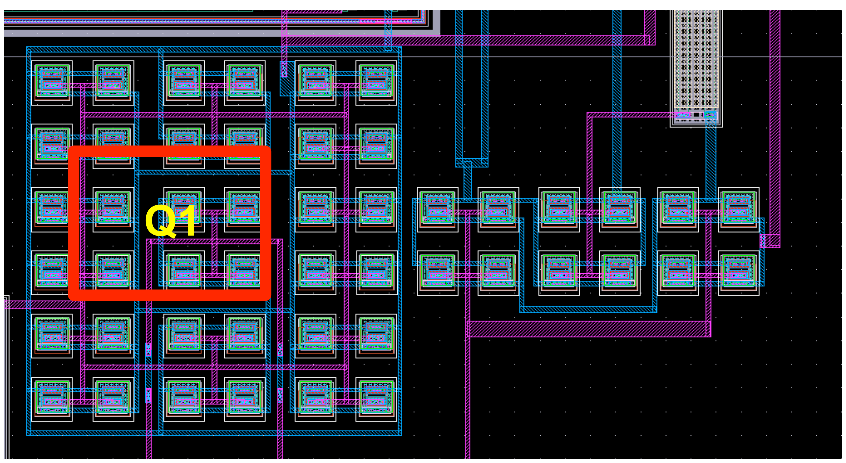


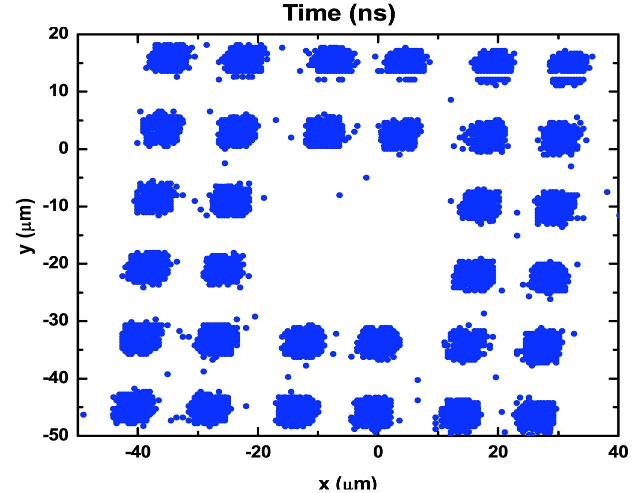
SET in a SiGe BGR

- **Transient Response Depends on the Location of the Ion Strike**
- **Transients on Q2 Give the Worst-Case SET Response**





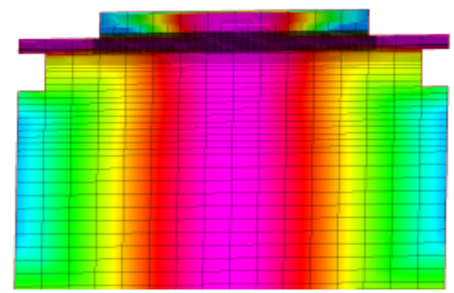




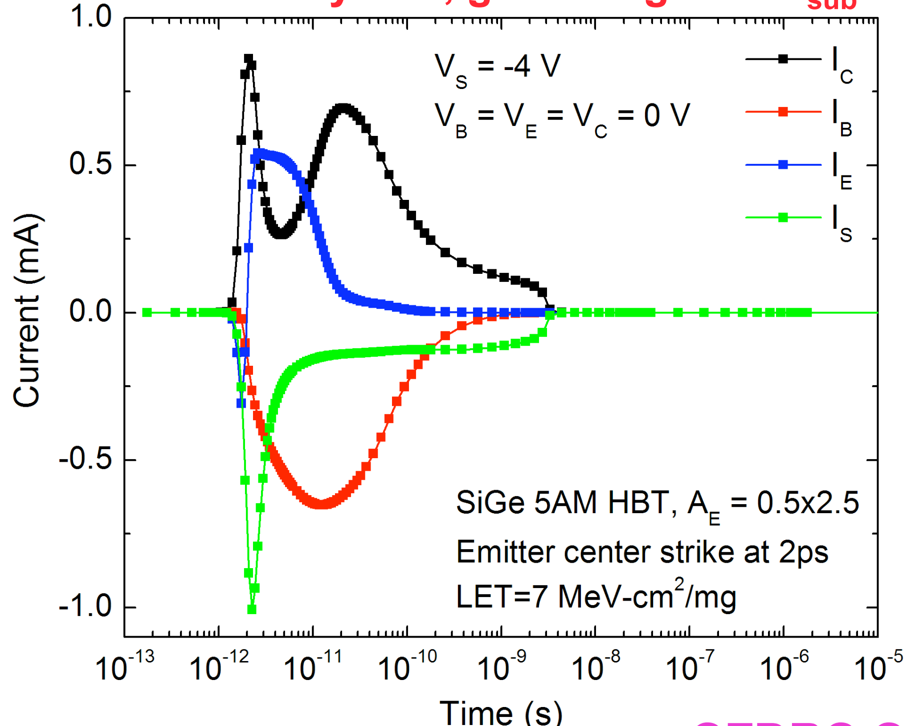
Mixed-mode TCAD

- **3D TCAD Model of 0.5 x 2.5 μm^2 SiGe HBT Calibrated to Data**
- **Goal: Leverage 3D Model to Understand Circuit-level SET Effects**

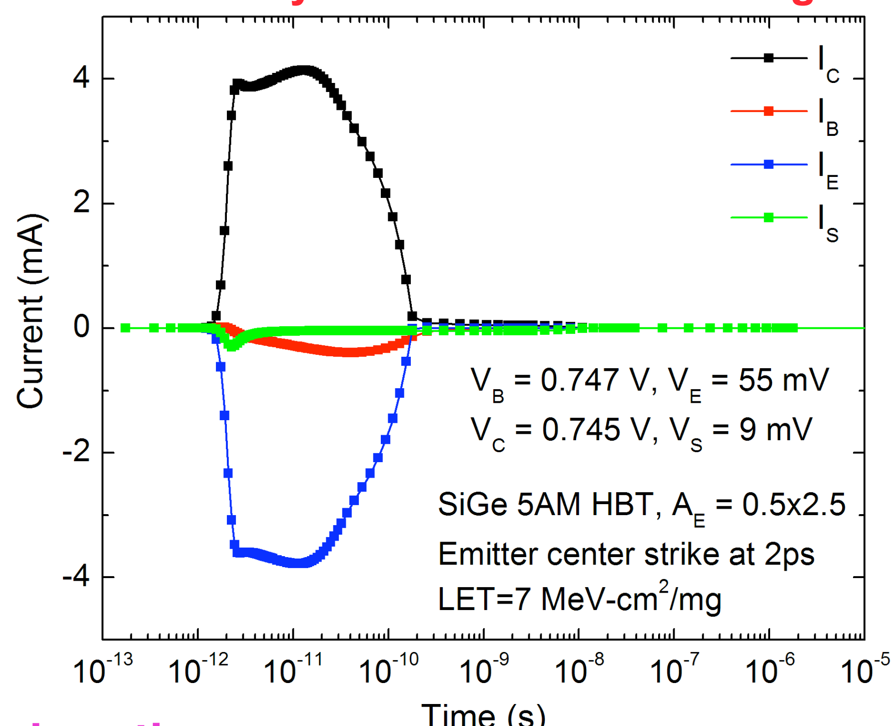
Emitter center strike



Device-only SET, gnd + negative V_{sub}



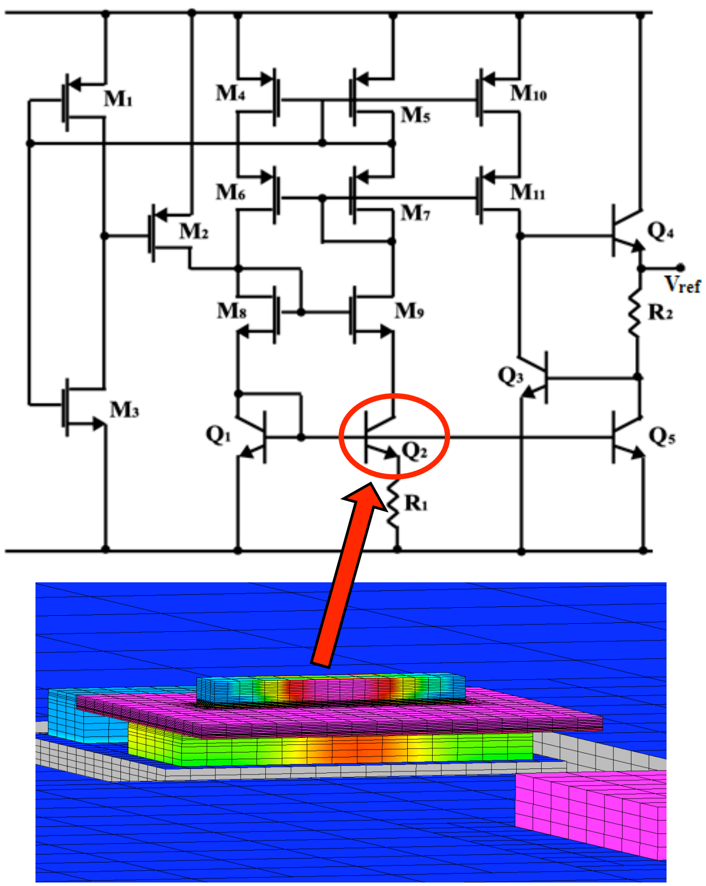
Device-only SET at BGR node voltages

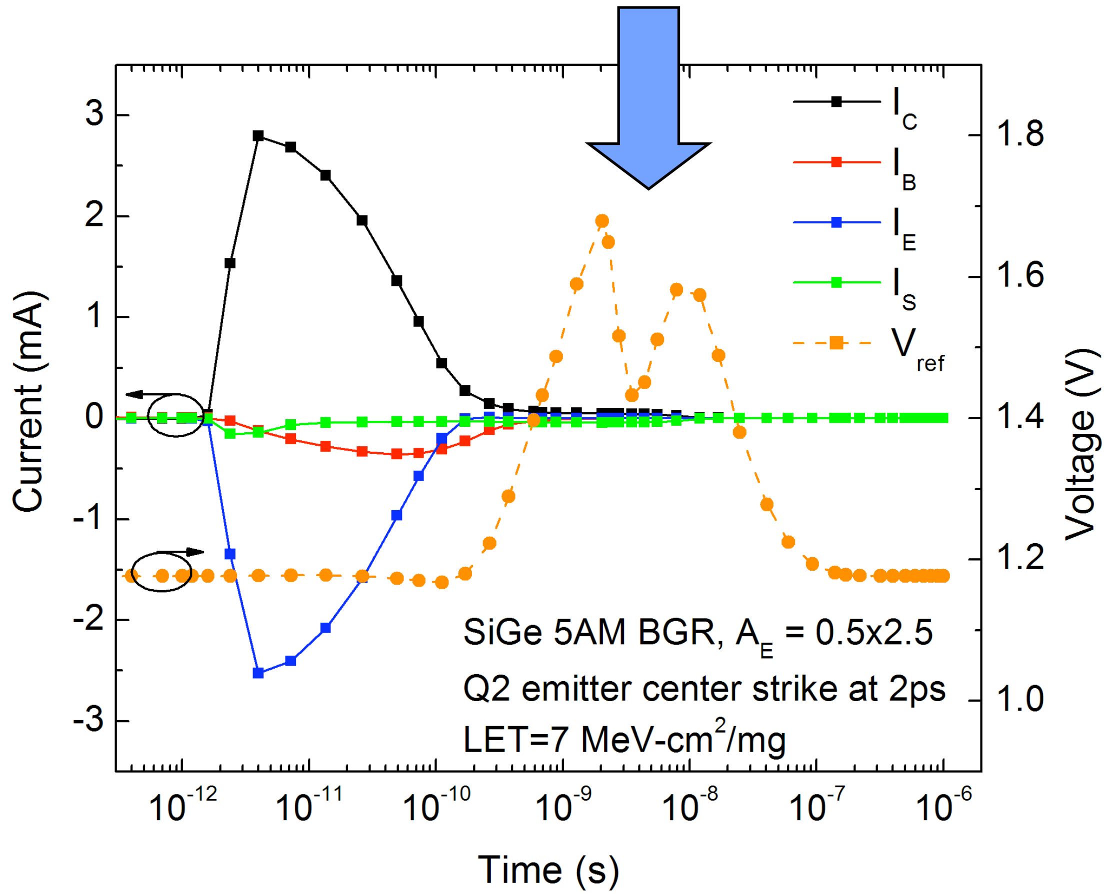


CFDRC Collaboration

True Mixed-mode SET

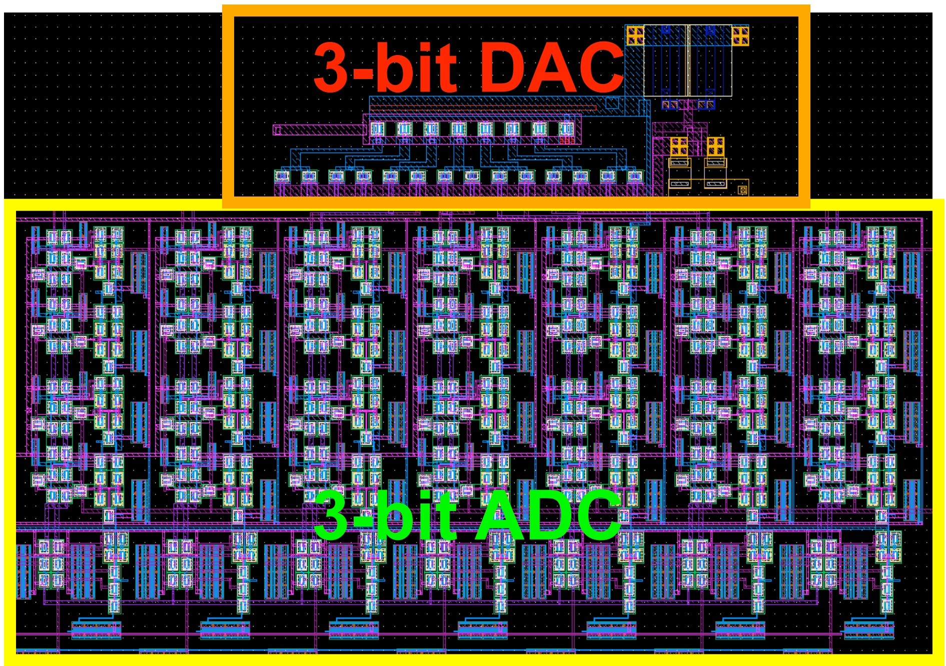
- CFDRC MixCad (Spectre + 3D NanoTCAD) Used to Simulate SET
- SiGe HBT Response in BGR Not Equal to Standalone SiGe HBT!
- Mixed-mode SET Simulation Shows Long Output Transient

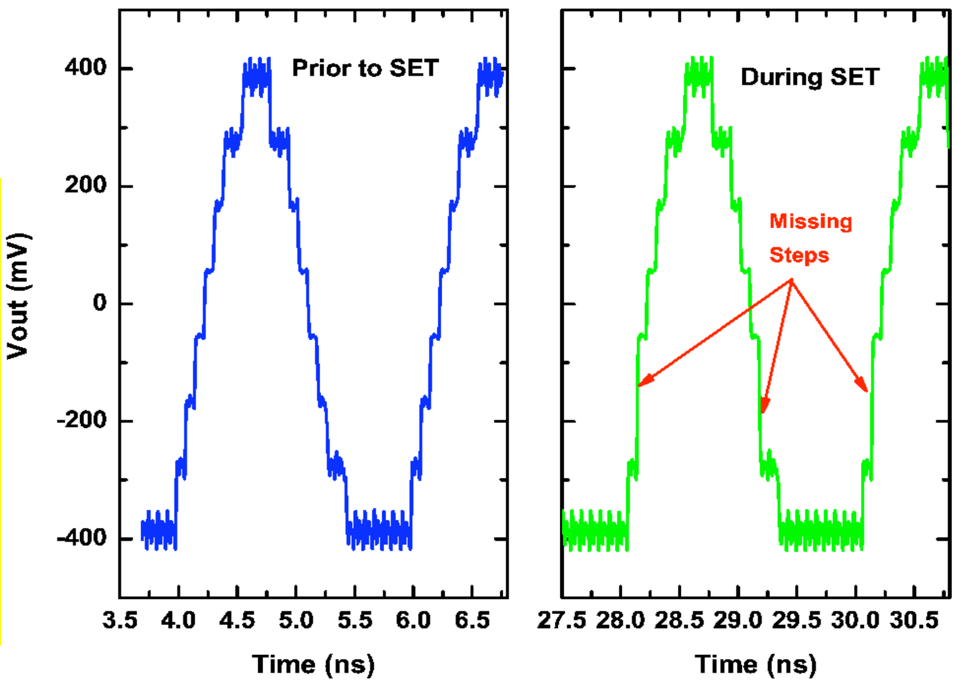




Impact on ADC

- SET in BGR Results in Time-Dependent Reference Voltage
- Comparator in ADC Fails to Generate The Correct Output
- Digital Output Code from DAC Will Be Corrupted





Simulated ADC response

Progress / Plans

- **SiGe Offers Great Potential for Many DoD Applications**
  - SiGe HBT + Si CMOS (RF to mm-wave + analog + digital for SoC / SoP)
- **Much SiGe Radiation Research to be Done! (in progress)**
  - improved understanding of basic damage mechanisms (TID + SEE)
  - understand the effects of temperature on damage mechanisms / SEE
  - **need to assess SET in analog / mixed-signal SiGe devices / circuits**
  - explore other SiGe HBT variants (SiGe HBT on SOI, C-SiGe, etc.)
  - explore other (new) SiGe-based devices (e.g., SiGe n/p-MODFETs)
  - **develop new RHBD approaches (device + circuit) for SEE mitigation**
  - **true mixed-mode 3D TCAD required for understanding of SET**
- **Lots of Leverage for SiGe Hardware / Testing Activity**
  - **many** SiGe tapeouts (IBM, IHP, TI, Jazz, NSC, ST): **devices + circuits**
  - DTRA / NASA-NEPP/ NASA RHESE (P. Marshall, J. Pellish, A. Keys)
  - NRL (D. McMorrow) / Sandia (P. Dodd, G. Vizkelethy)
  - CFDRC for Improved Mixed-mode TCAD (M. Turowski and team)
  - **excellent collaboration between Georgia Tech and Vanderbilt teams**

Publications

Georgia Institute of Technology

2008 Papers

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