Radiation Effects in SiGe Devices

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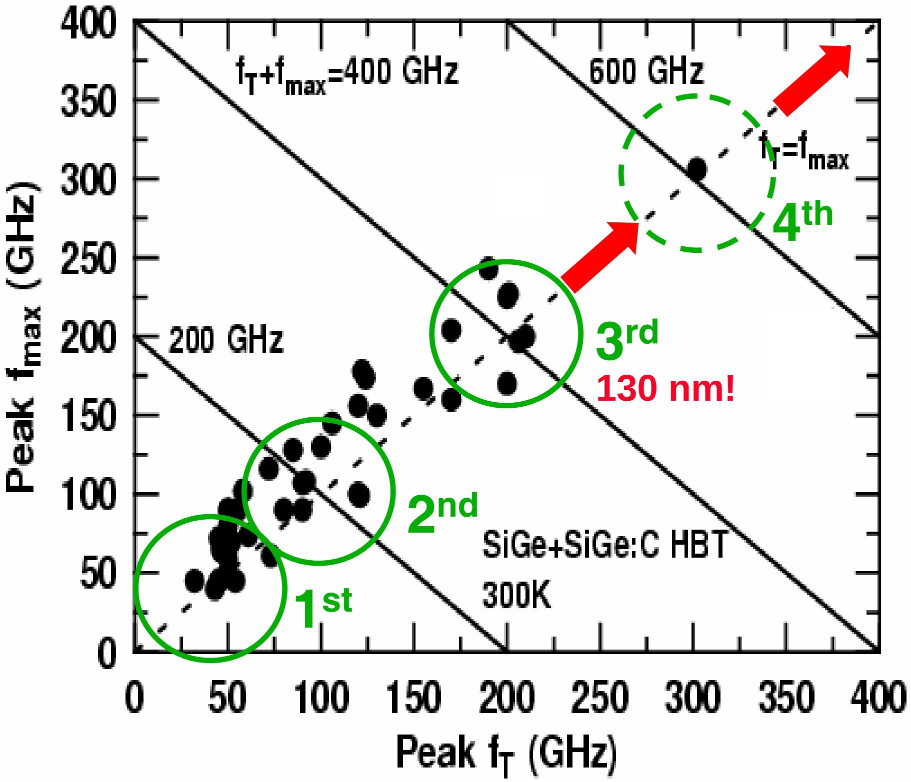
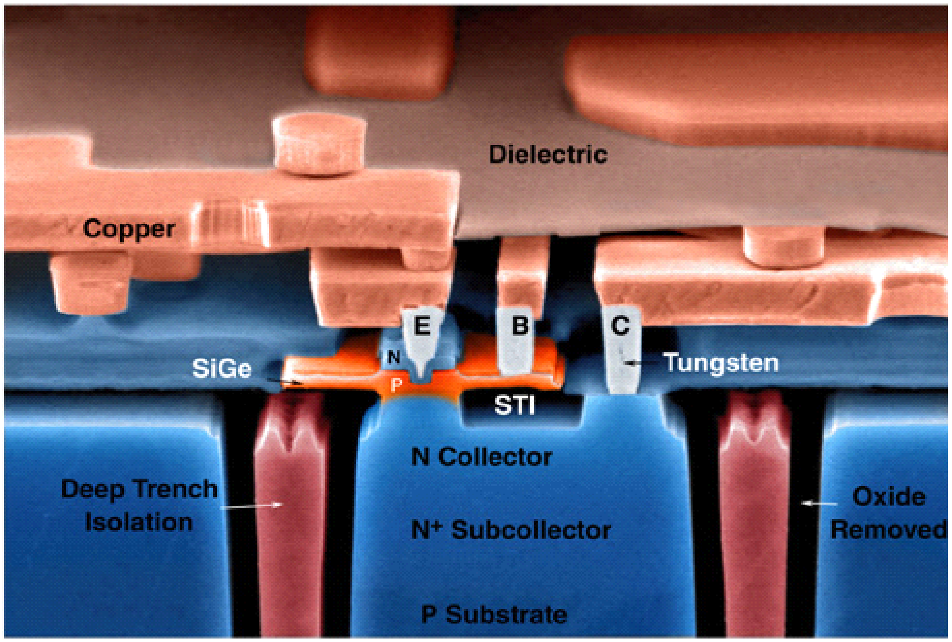
Outline

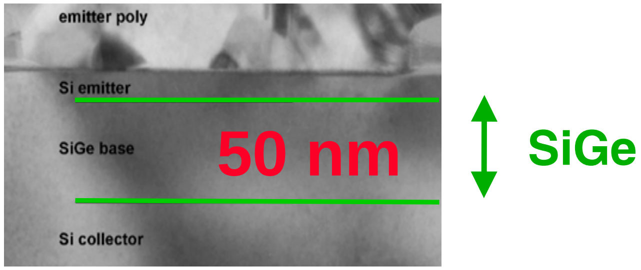
- **Some Updates from the SiGe World**
- **Progress in RHBD for Bulk SiGe HBT Platforms**
  - some new RHBD approaches
- **Radiation Effects in New SiGe Technology Platforms**
  - IBM SiGe 8WL
  - SiGe HBTs on SOI
- **Radiation Effects in Advanced Si/SiGe FETs**
  - SiGe MODFETs (n-channel + p-channel)
  - 65 nm Strained Si RF-CMOS on SOI
- **Progress / Plans**

SiGe Evolution

- SiGe = SiGe HBT + Si CMOS for Highly Integrated Solutions
- Rapid Generational Evolution (full SiGe BiCMOS)
- Significant In-roads in High-speed Communications ICs





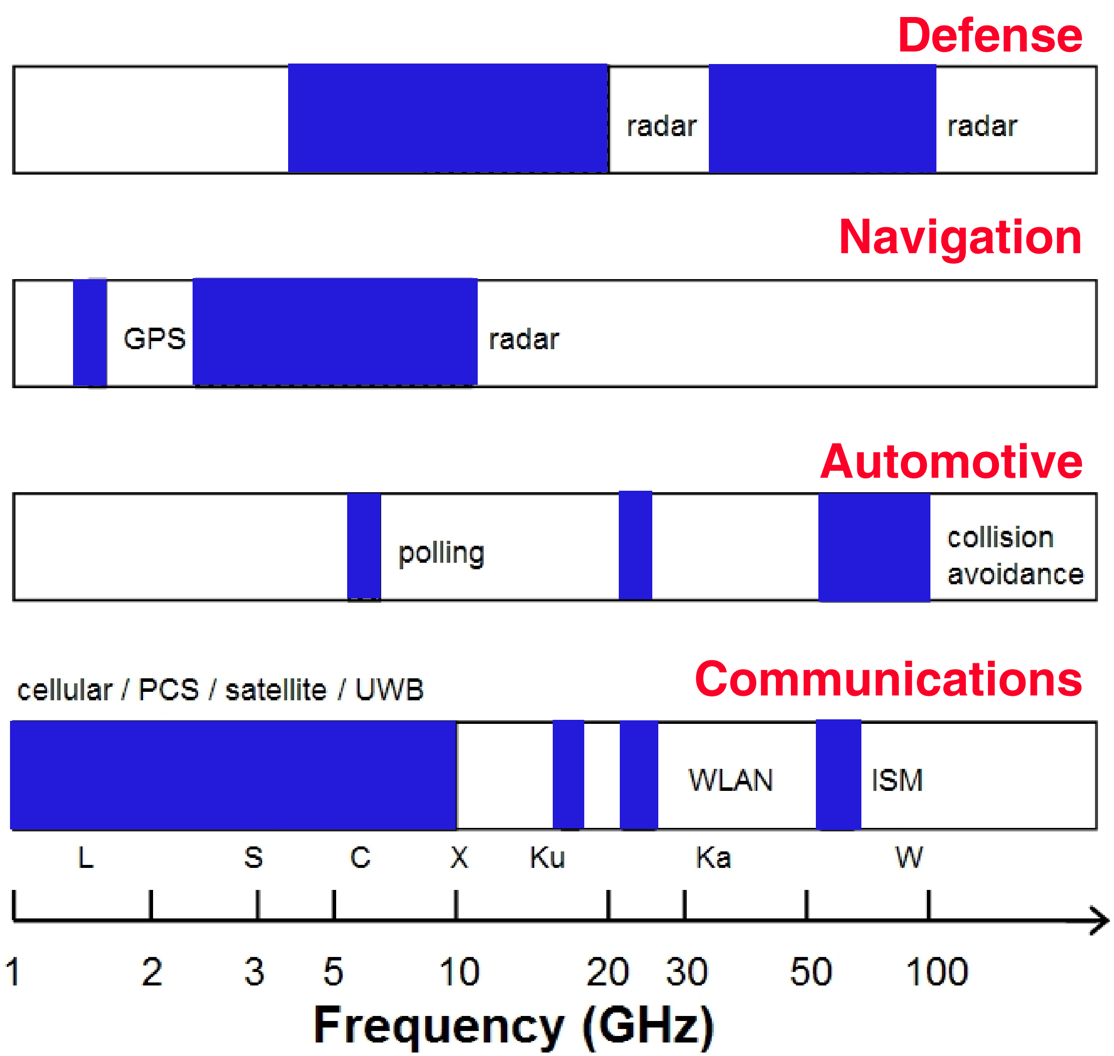


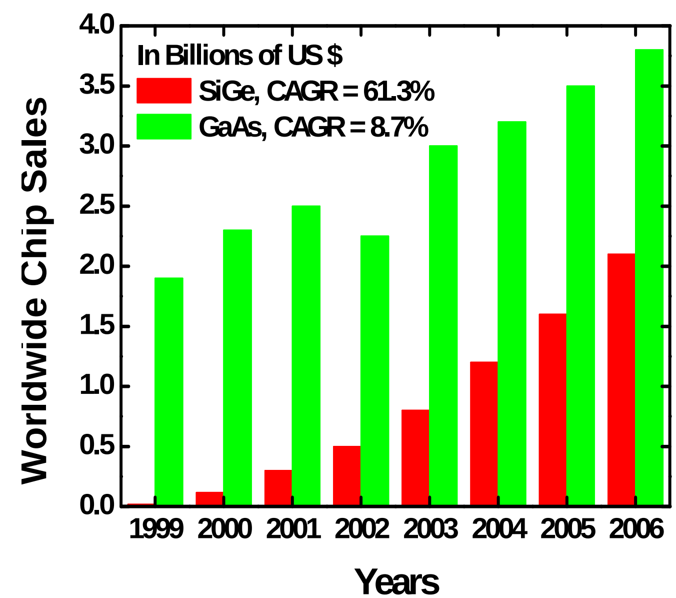
SiGe = III-V Speed + Si Manufacturing

Win-Win!

SiGe Market

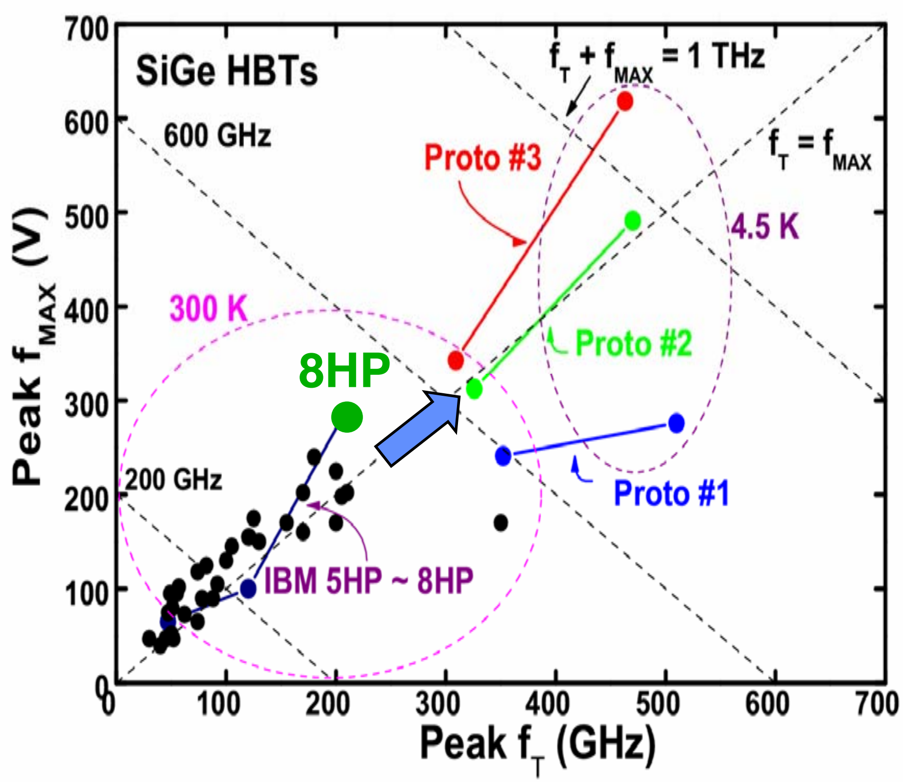
Some Application Bands for SiGe IC's

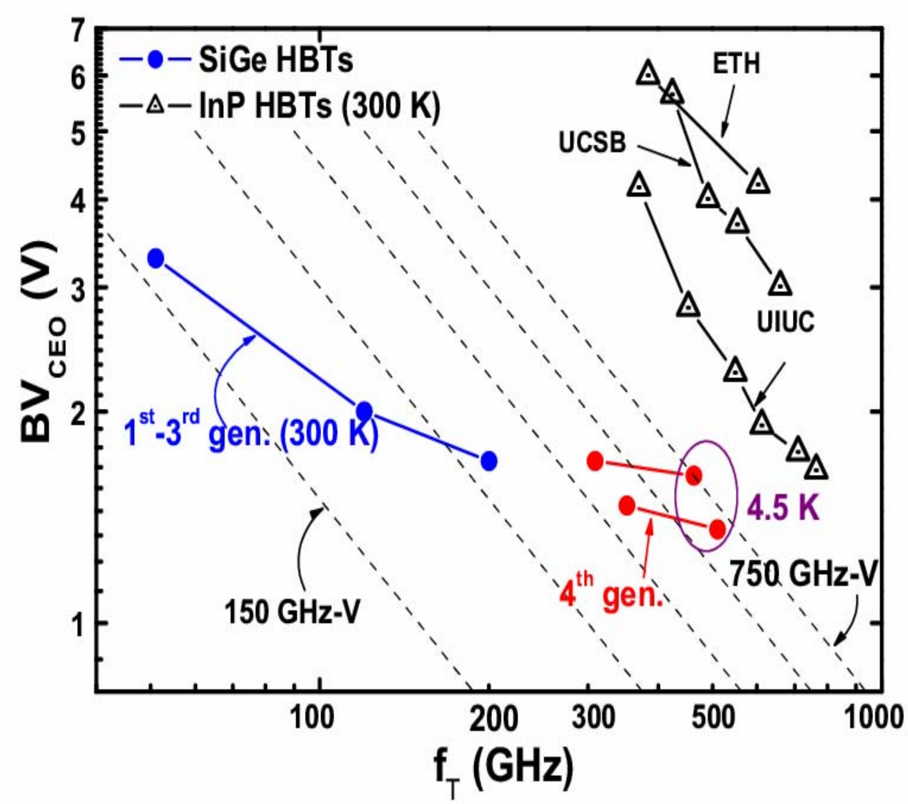




SiGe Performance Limits

- **Half-TeraHertz SiGe HBTs Are Clearly Possible** (at modest lith)
- **Both f_T and f_{max} above 500 GHz at Cryo-T** (T = scaling knob)
- **Goal: Useful BV @ 500 GHz** (BV_{CEO} > 1.5 V + BV_{CBO} > 5.5 V)





200-500 GHz @ 130 nm Node!

New Opportunities

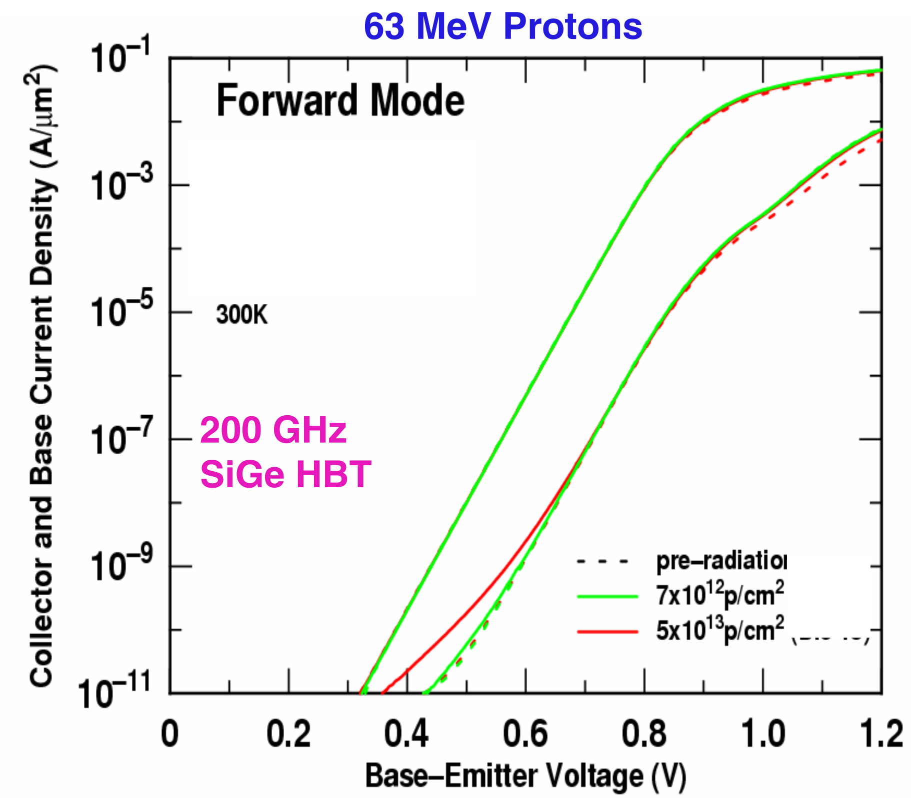
Georgia Institute of Technology

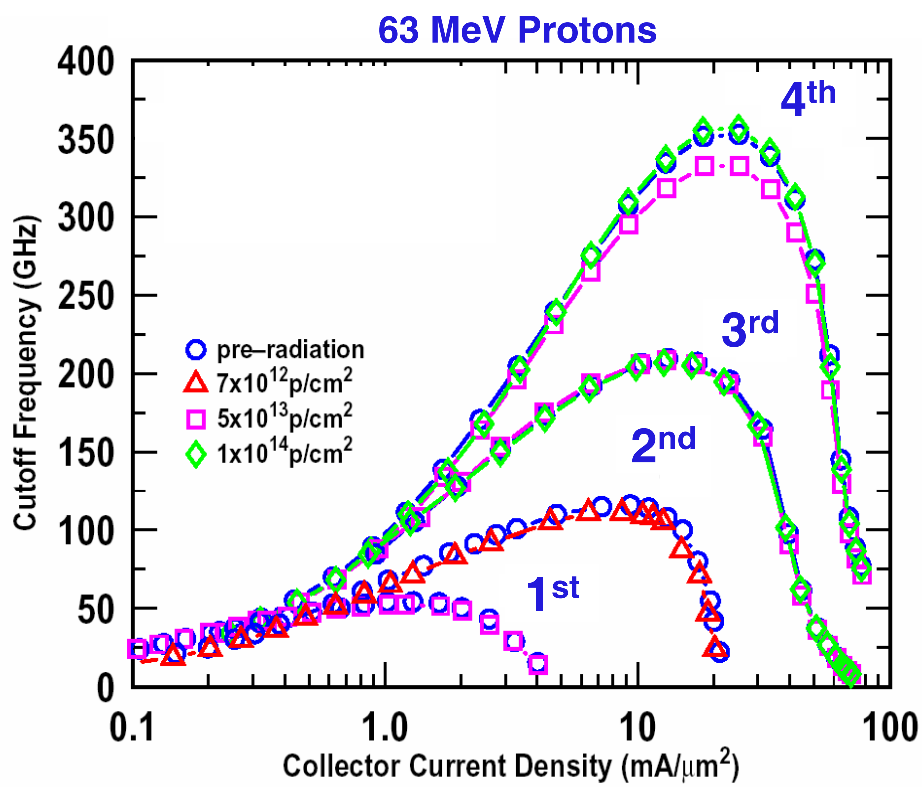
- **SiGe for Radar Systems**
  - **DoD phased arrays** (2-10 GHz and up) **+ automotive** (24, 77 GHz)
- **SiGe for Millimeter-wave Communications / THz Imaging**
  - **Gb/s wireless** (60, 94 GHz) **/ imaging systems** (100-300 GHz)
- **SiGe for Analog Applications**
  - **data conversion** (ADC limits) **+ the emerging role of C-SiGe** (npn + pnp)
- **SiGe for Extreme Environment Electronics**
  - **extreme temperatures** (4K to 300C) + **radiation** (e.g., space systems)
  - **explore performance limits of SiGe** (goal: 1 THz aggregate $f_T + f_{max}$)
- **SiGe for Enhanced Dynamic Range Systems**
  - **improved understanding of linearity / extreme wideband transceivers**

All Are Highly DoD Relevant!

Total-Dose Response

- **Multi-Mrad Total Dose Hardness (with no intentional hardening!)**
  - **- ionization + displacement damage very minimal; no ELDRS either!**
- **Radiation Hardness Due to Epitaxial Base Structure (not Ge)**
  - - thin emitter-base spacer + heavily doped extrinsic base + very thin base

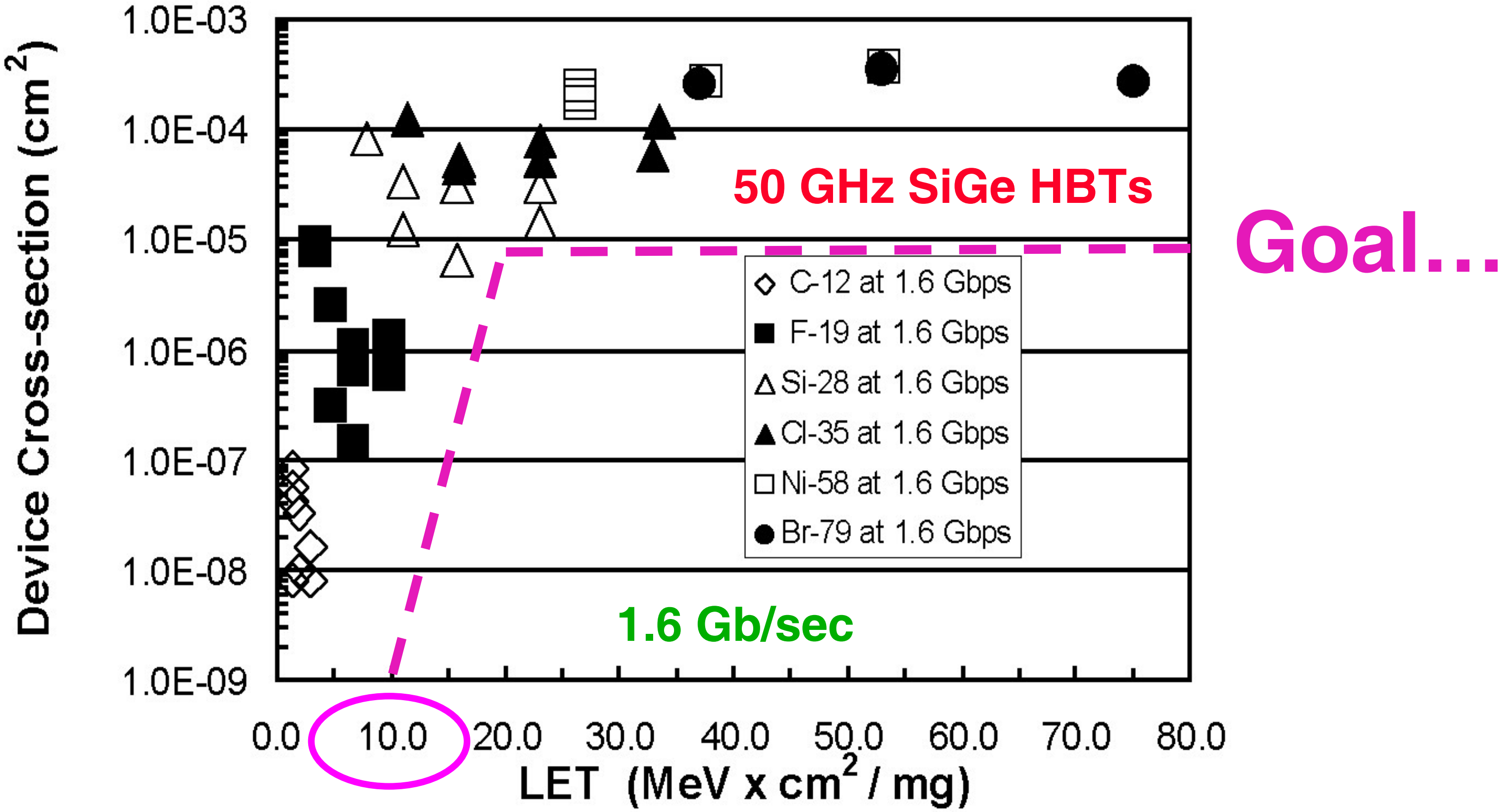




63 MeV protons @ 5×10^{13} p/cm^2 = 6.7 Mrad TID!

Single Event Effects

- **Observed SEU Sensitivity in SiGe HBT Shift Registers**
  - low LET threshold + high saturated cross-section



P. Marshall *et al.*, *IEEE TNS*, 47, p. 2669, 2000

SEU RHBD in SiGe

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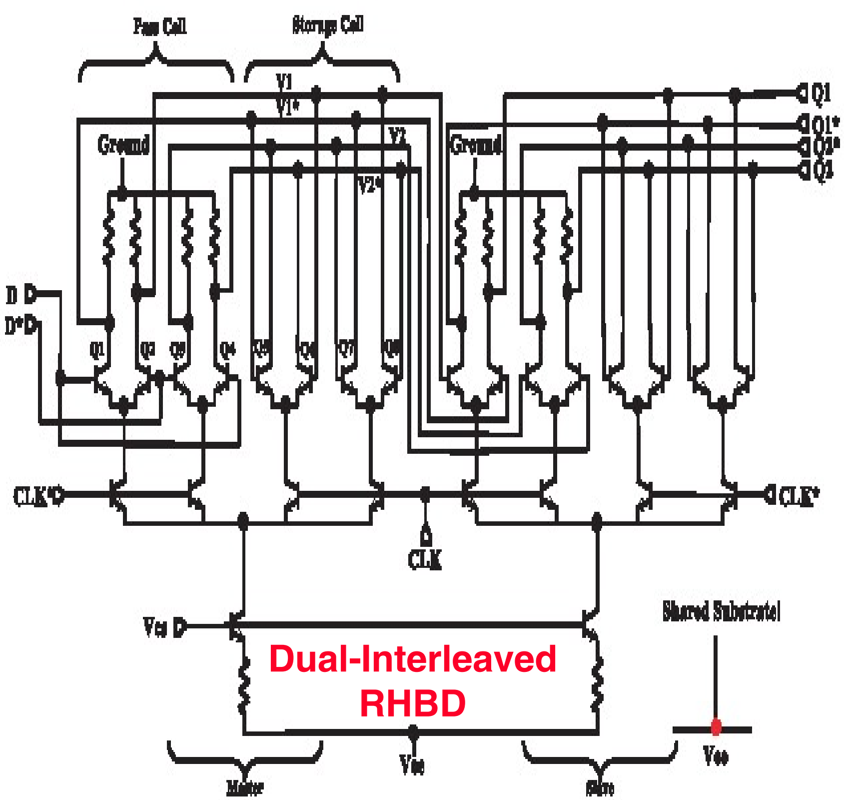
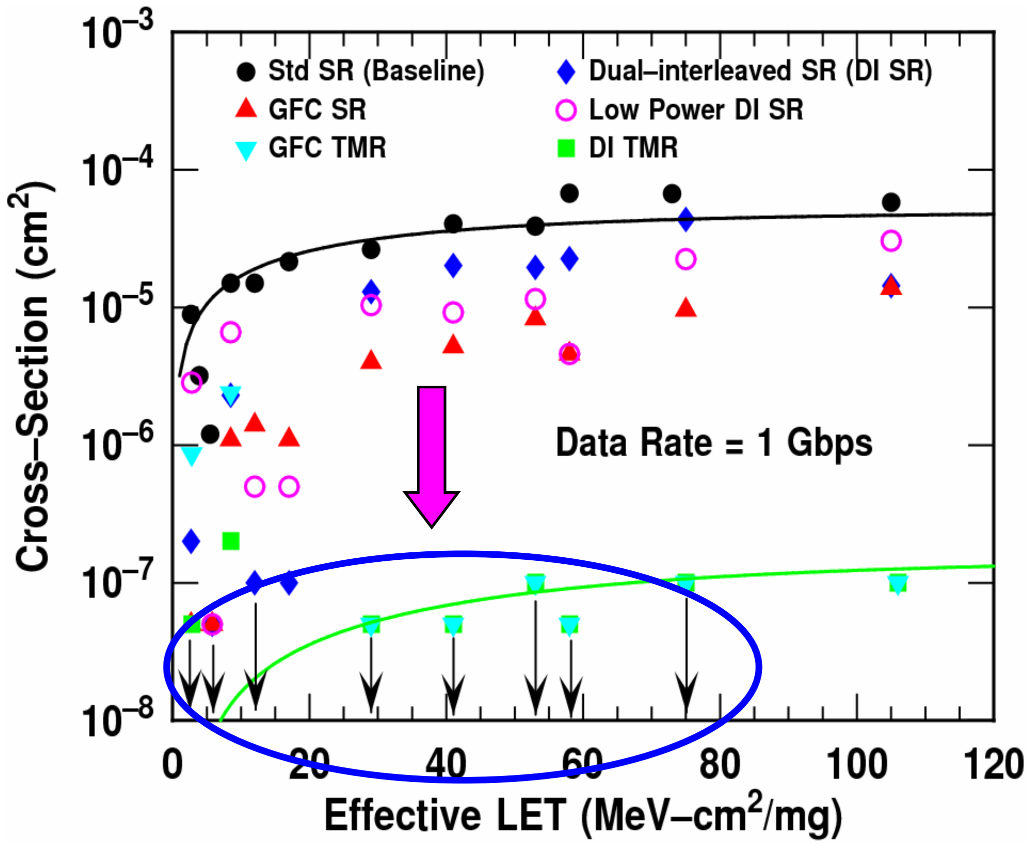
- **Reduce Tx-Tx Feedback Coupling Internal to the Latch**
- **Circuit Architecture Changes + Transistor Layout Changes**





Q: Can We Eliminate TMR?

Proton Cross-Section

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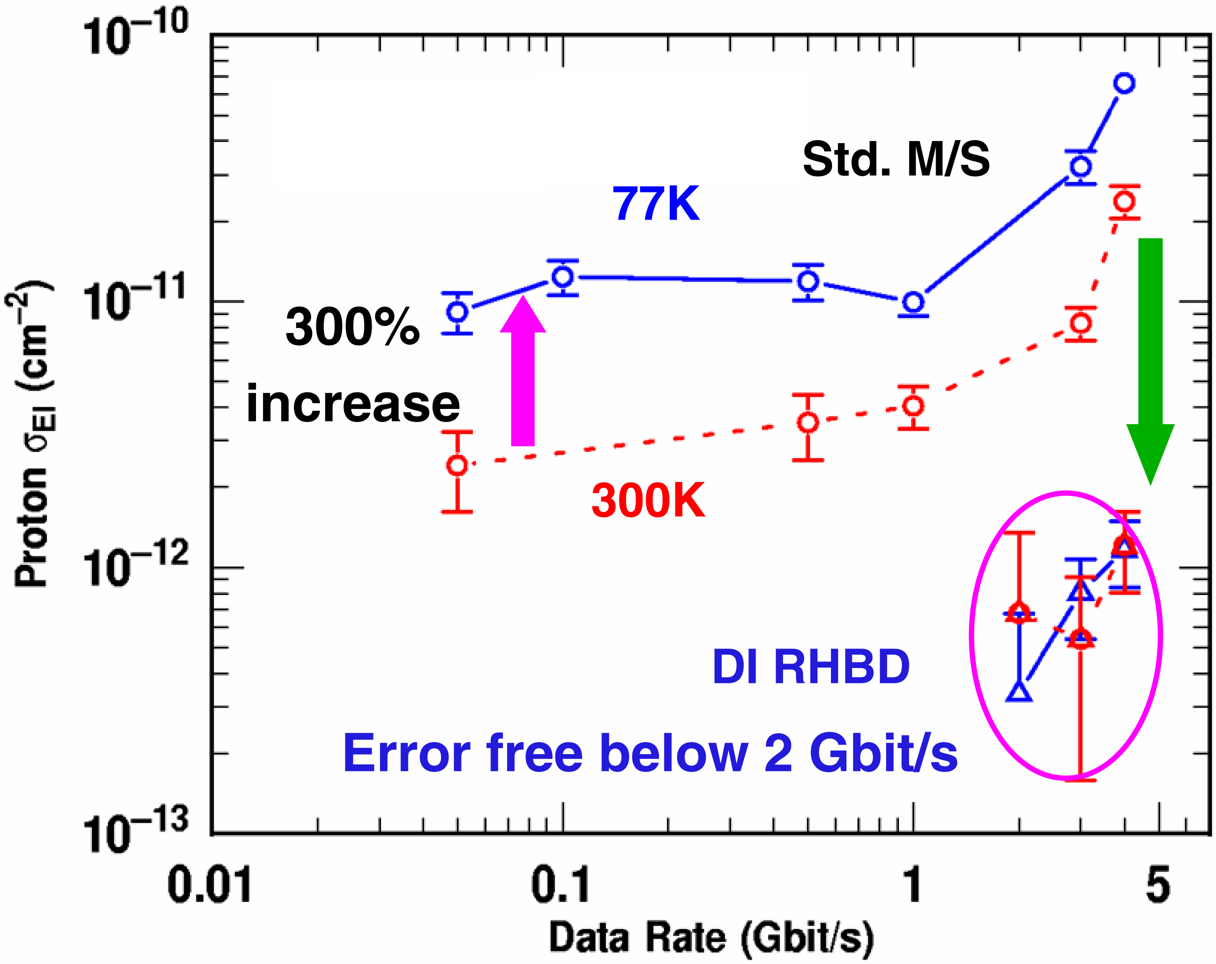
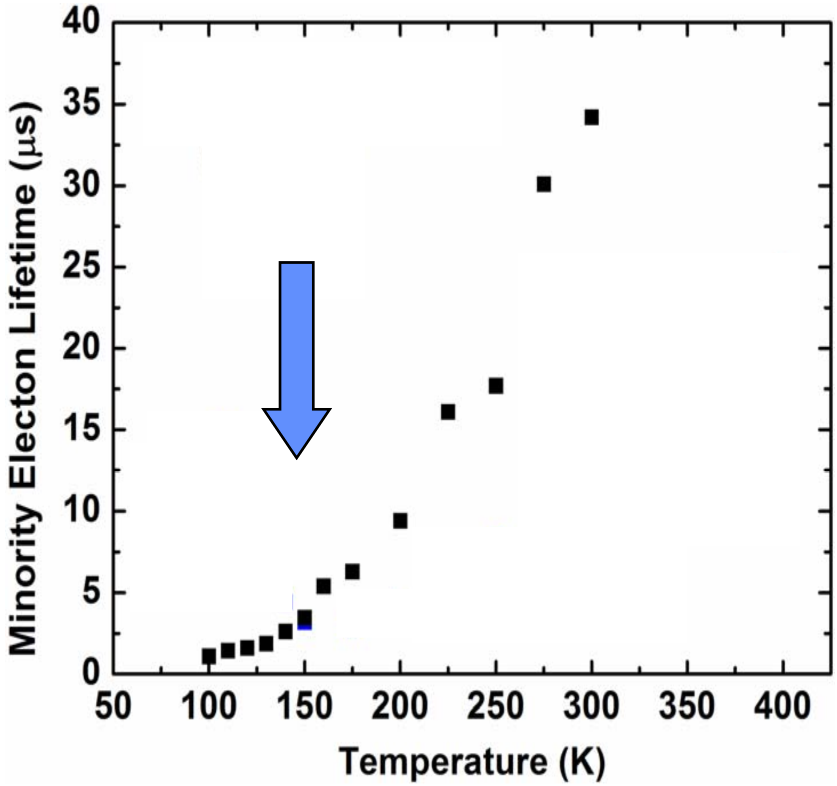
- Proton σ_{EI} is 5 Orders of Magnitude Less Than Heavy Ion σ_{EI}
- 3X Increase in Proton Cross-section at 77K for Std. M/S … BUT
- DI RHBD is Error-free < 2 Gbit/s and Insensitive to Temperature

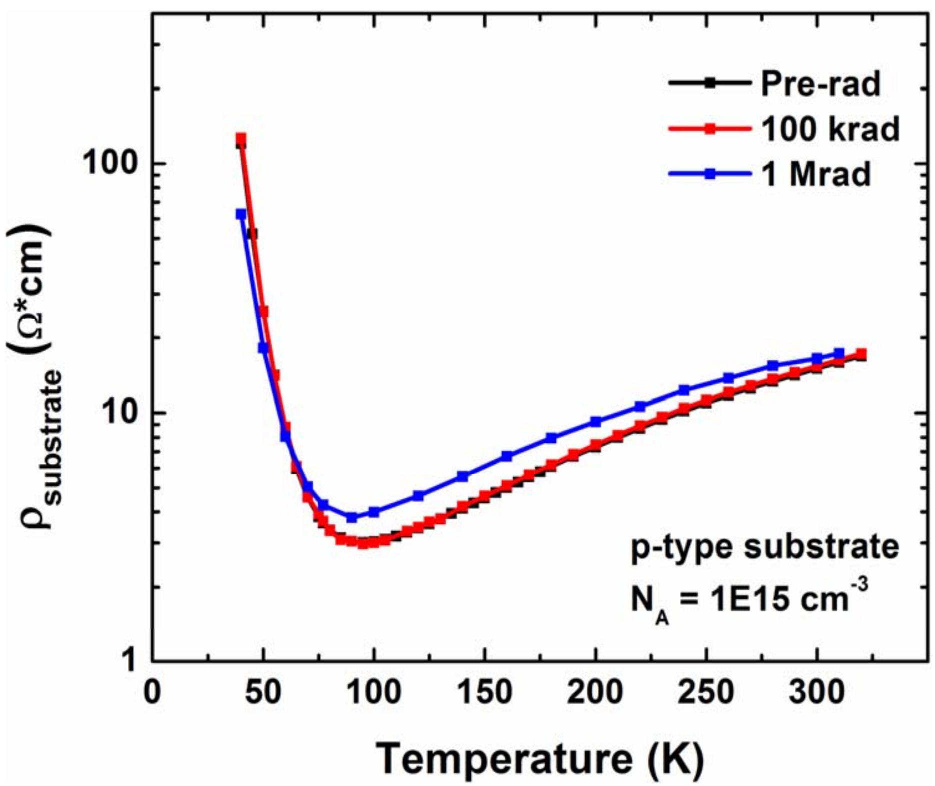


$$\sigma_{EI} = \frac{\text{Number of Error Intervals}}{\text{Fluence } (\Phi)}$$

Transport Parameters

- Bulk Minority Carrier Lifetime in Substrate as f(T)
- Substrate Resistivity (mobility) as f(T) – Key for SEU

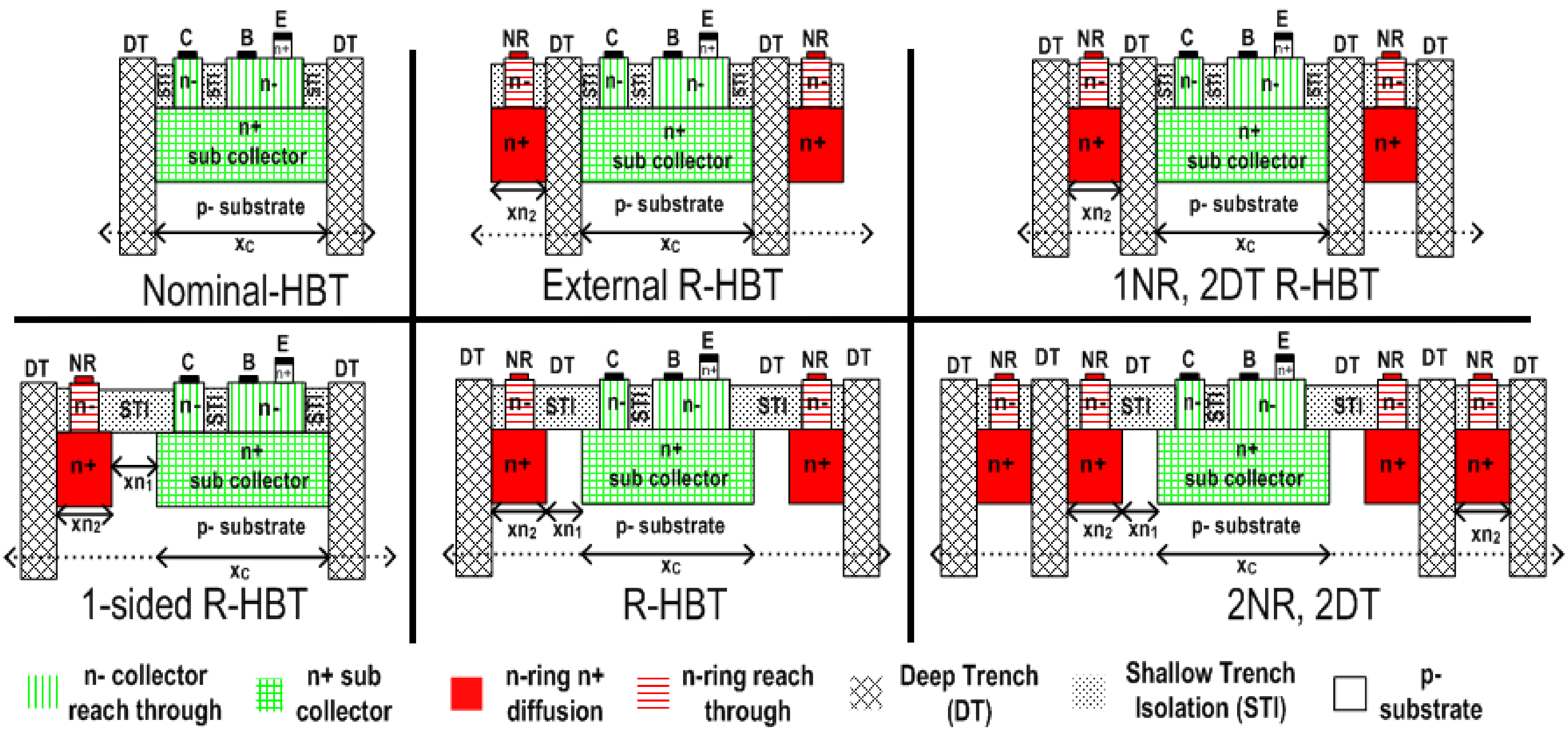




Robust Measurements are NON-TRIVIAL!

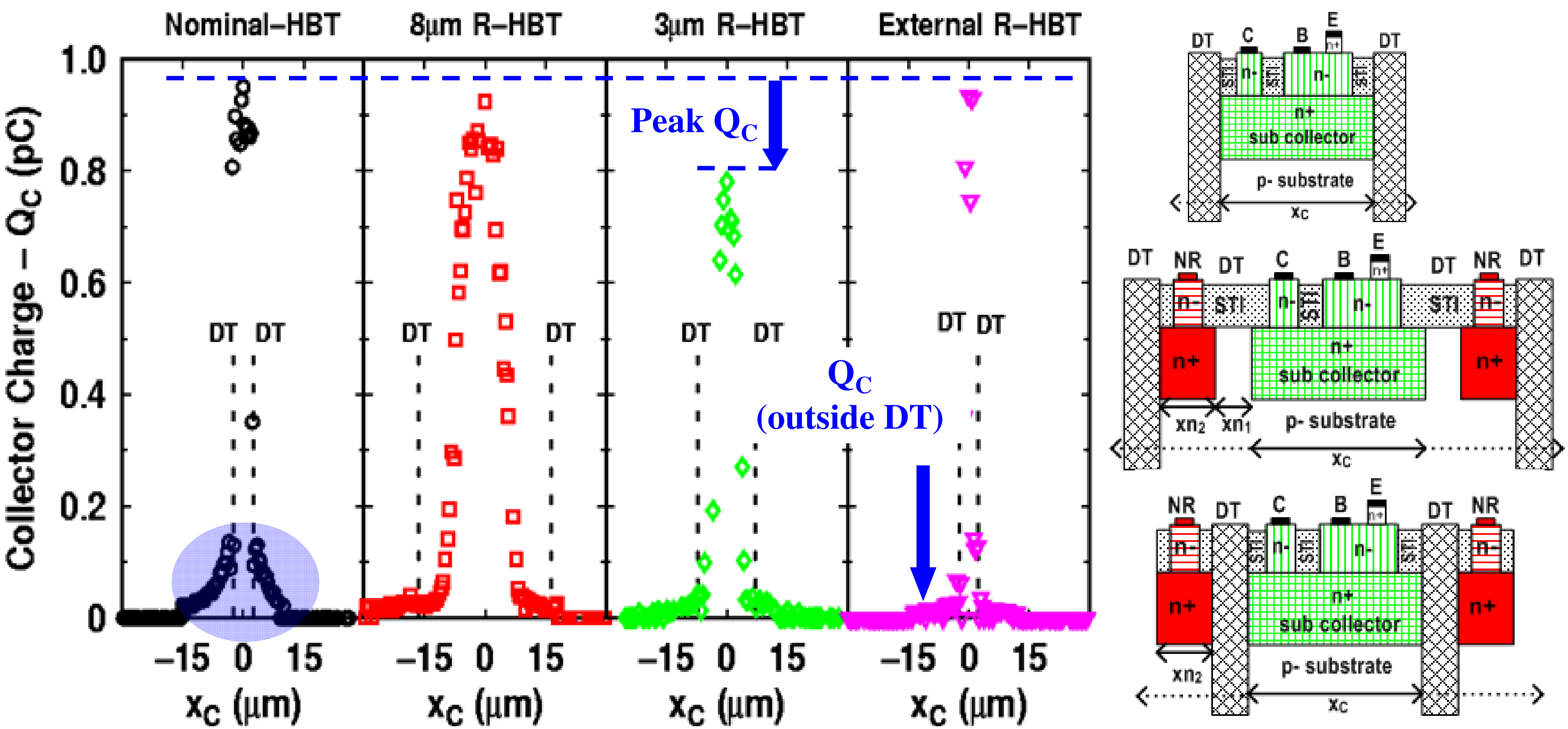
Layout-Based RHBD

- **Alternate Reverse-biased pn Junction** ***(Sx to N-ring)***
  - identical doping profile to device sub-collector
  - internal and/or external DT placement possible



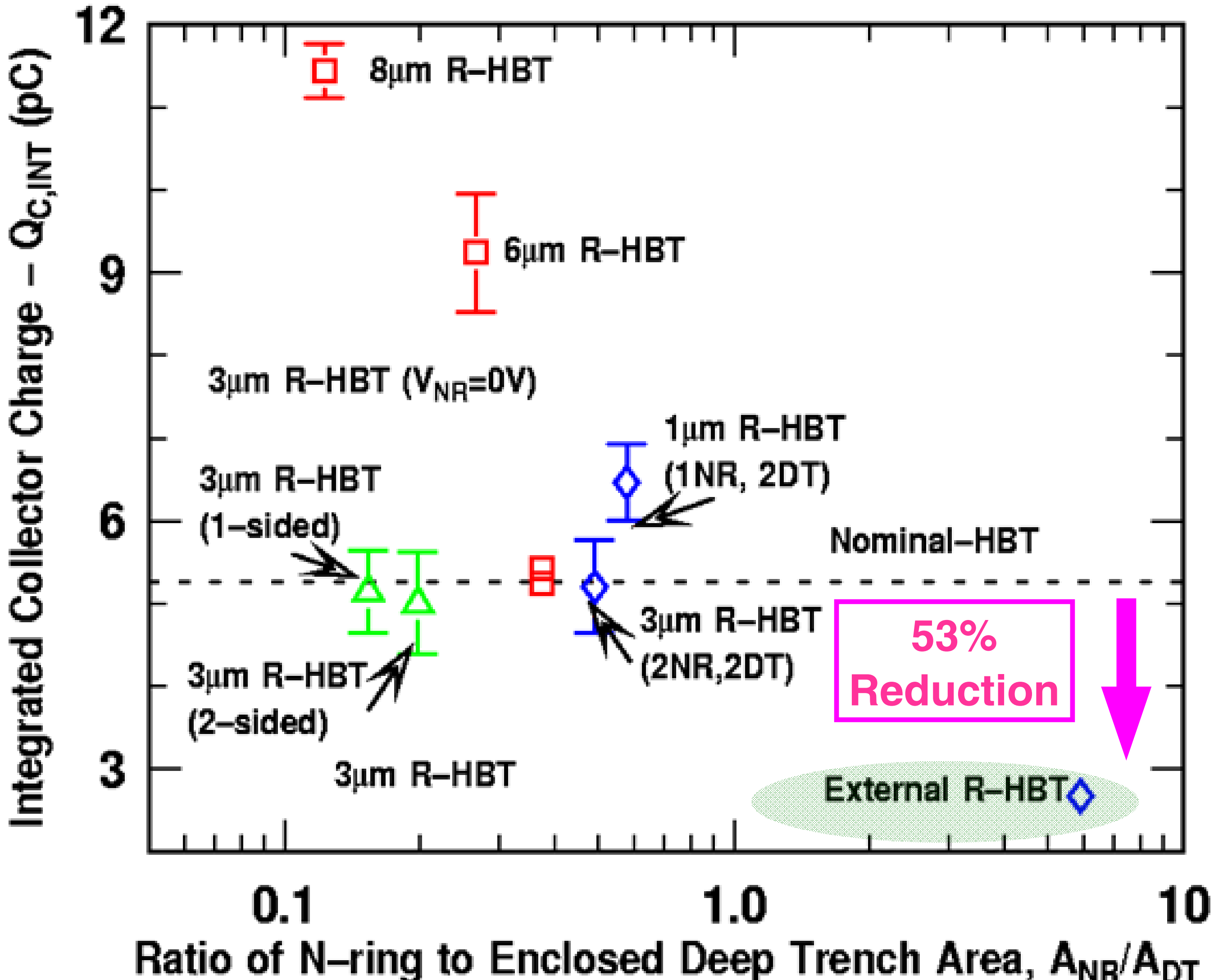
Microbeam Testing

- **5-probe IBICC Measurement** (Sandia National Lab)
  - 36 MeV O_2 ions, LET= 7 MeV-cm^2/mg, 25 μm Si range
  - 100 μm^2 scan, $V_C=V_B=V_E=0$ V, V_{SX}= -4 V, V_{NR} = 0 - 4V



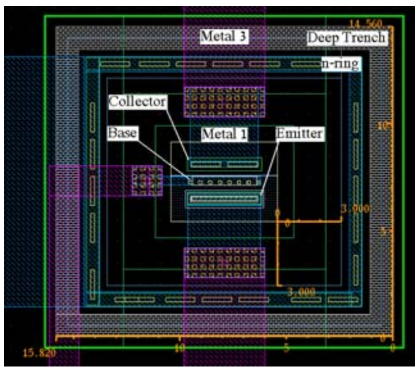
RHBD Bottom-Line

- $Q_{C,INT}$ Decreases with Increasing A_{NR}/A_{DT}



TCAD SEU Simulations

- **NanoTCAD 3-D Ion Strike Simulations (CFDRC SBIR)**
  - Cadence layout + SIMS profile → **3-D solid geometry**
  - encased in wrapping layer (absorbing boundary τ_W=50 ns)
  - SRH + Auger; doping, E-field, scattering dependent models



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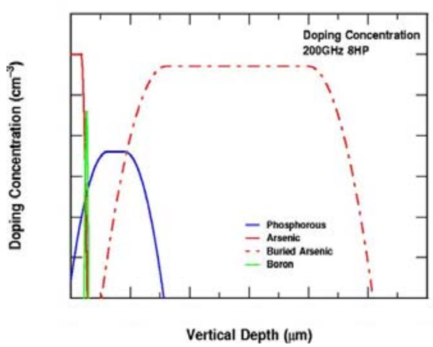
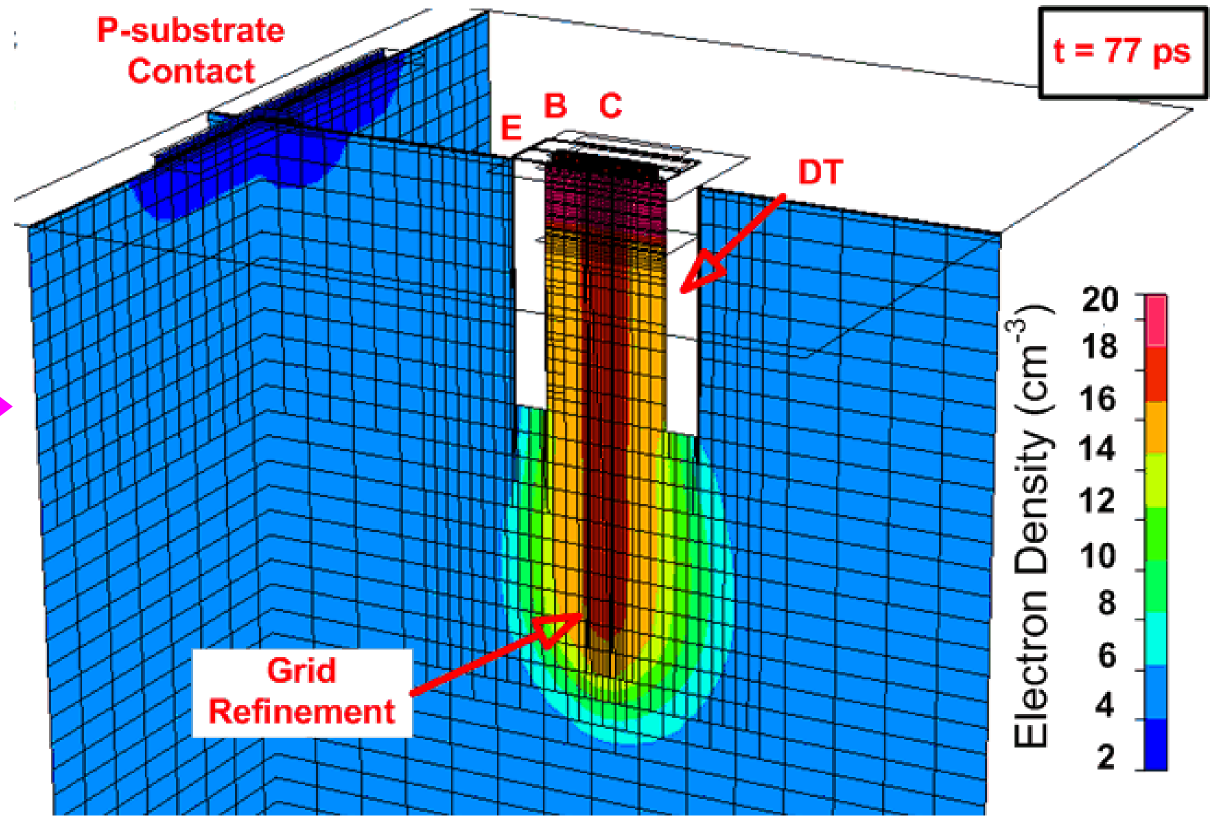
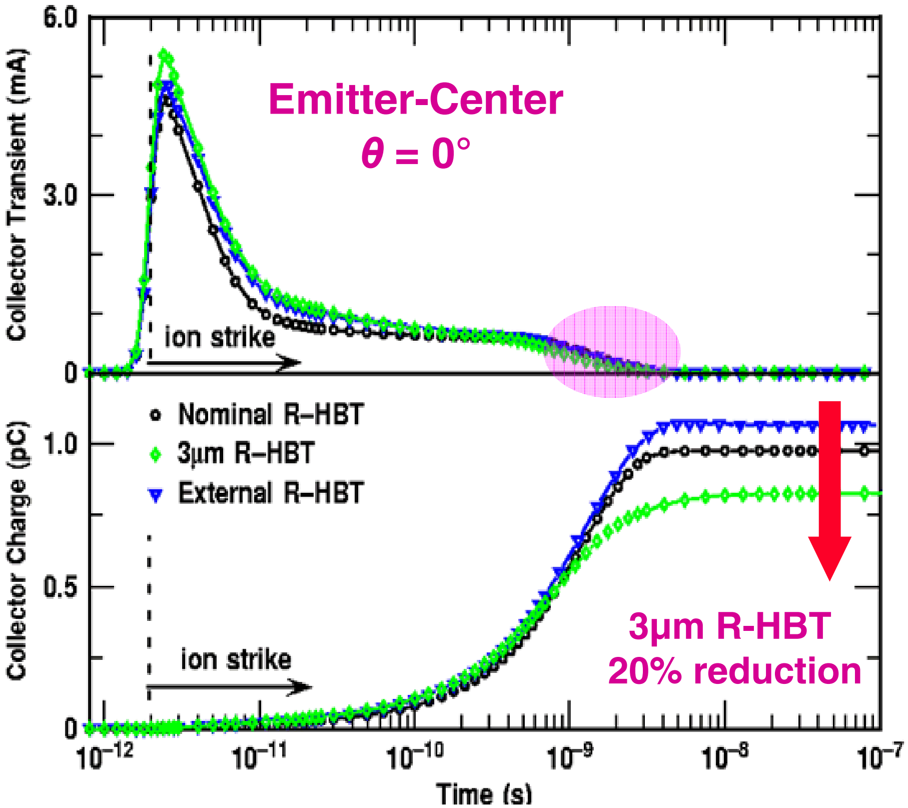
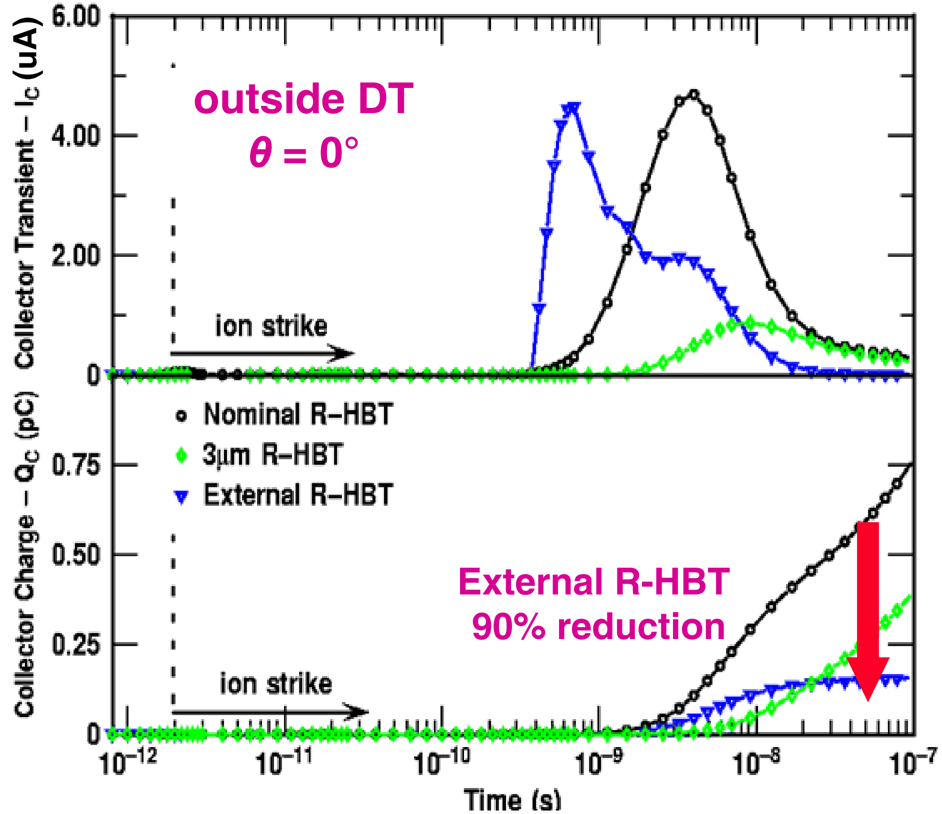




SE Transients

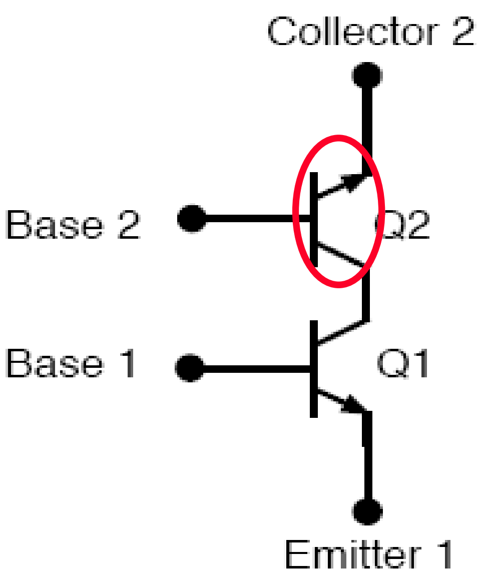
- **RHBD (E-center vs. outside DT strikes)**
  - n-ring does not affect prompt collection (drift dominated)
  - 3μm R-HBT E-center strike → 20% reduced Q_C
  - external R-HBT outside DT strike → **90% reduced Q_C!**

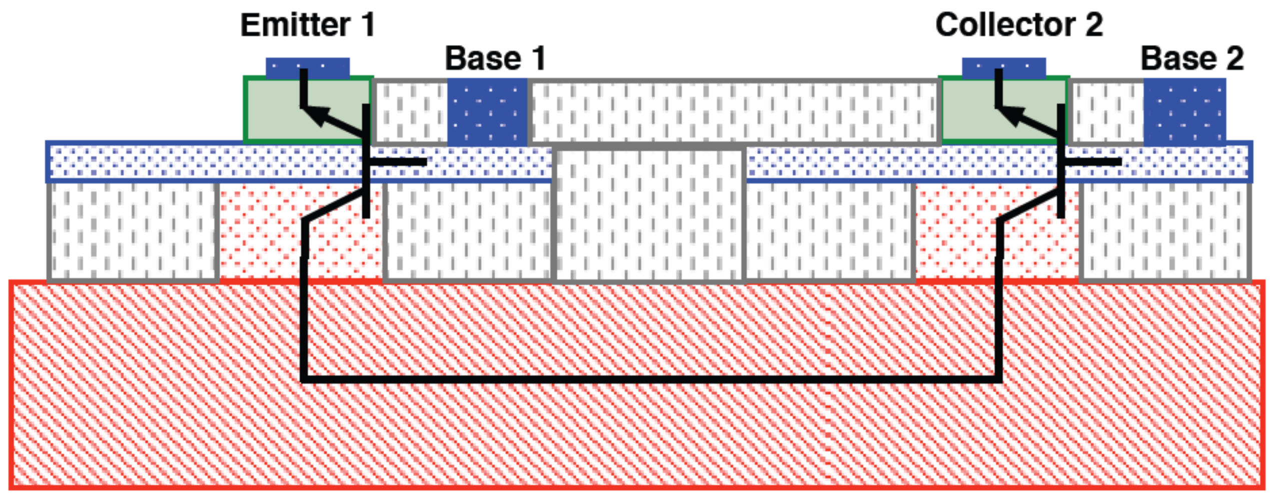


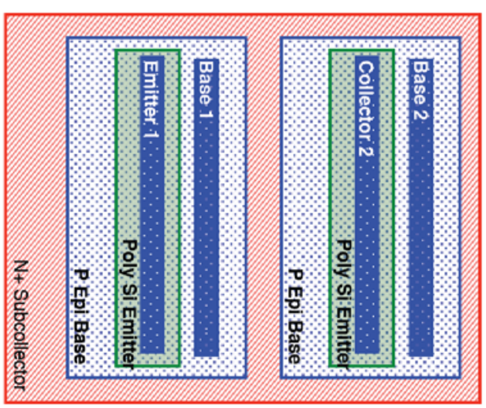


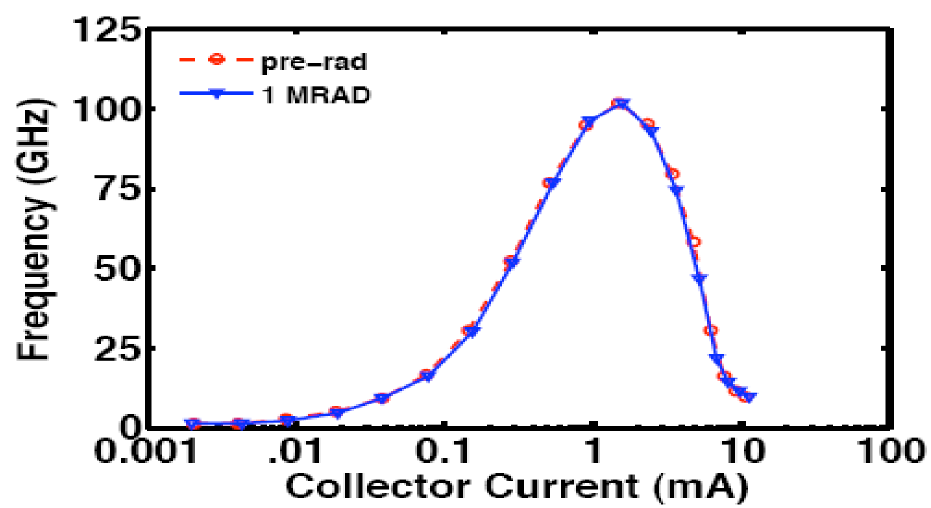
Inverse-Cascode RHBD

- **Cascode Structure with Inverse Mode Common-Base Device**
- **Compact Layout + Excellent Performance! Q: SEU Leverage?**









New Circuit-level RHBD

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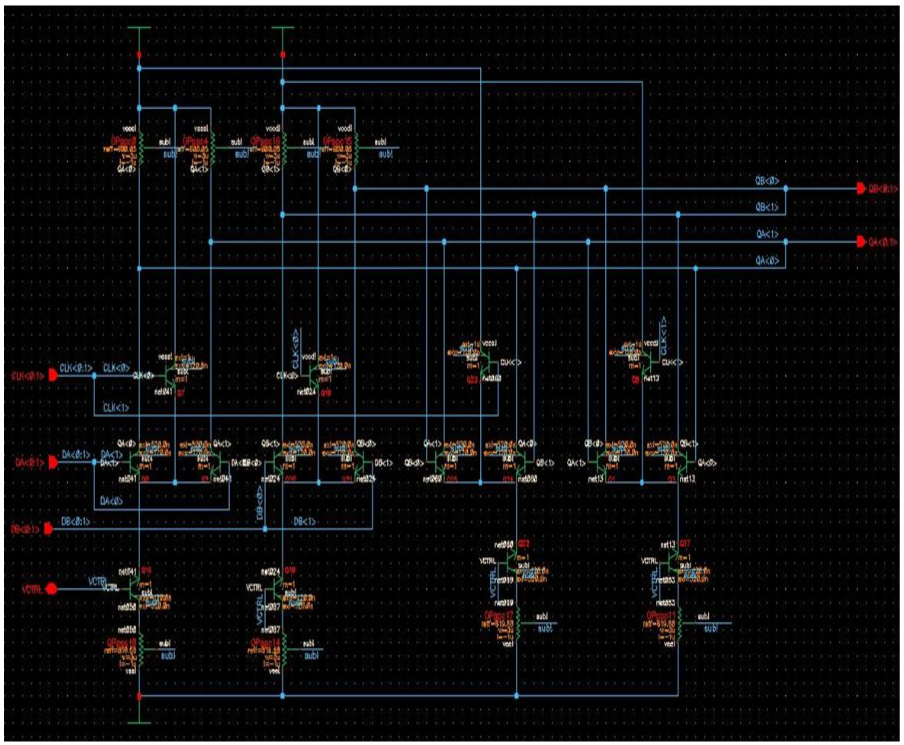
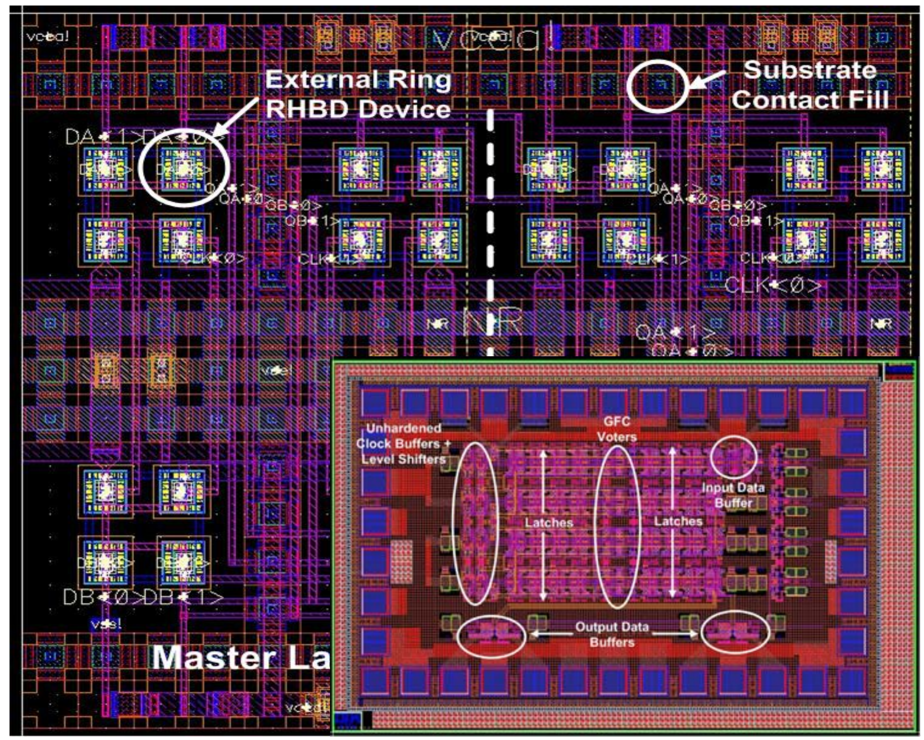
- **"Triple Tail Cell Latch"**
  - clock transistors <u>emitter</u>-coupled to differential pair
  - inverse voltage controlled current source + dual interleaved
  - 8HP 16-bit SR with GFC + device hardened buffers (in fab)



Ref: Razavi JSSC 1994



New RHBD Shift Register

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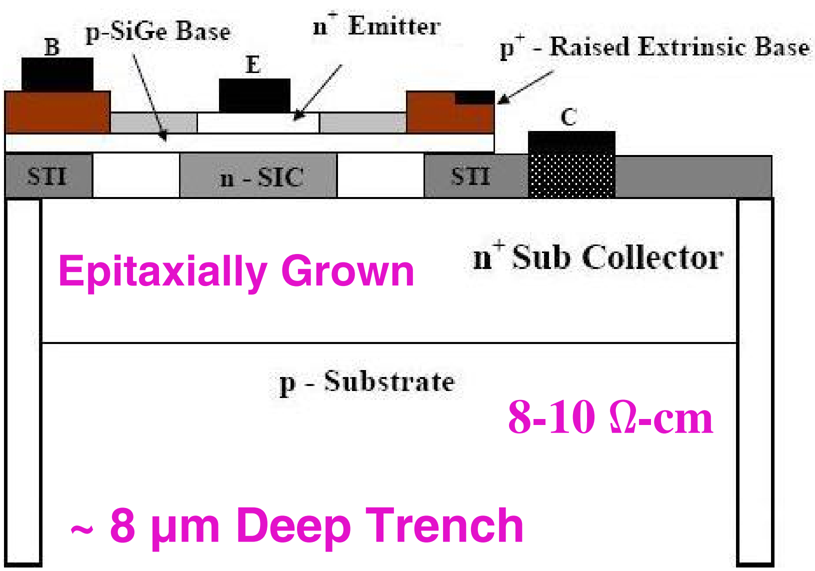
- Some Updates from the SiGe World
- Progress in RHBD for Bulk SiGe HBT Platforms
  - some new RHBD approaches
- **Radiation Effects in New SiGe Technology Platforms**
  - IBM SiGe 8WL
  - SiGe HBTs on SOI
- **Radiation Effects in Advanced Si/SiGe FETs**
  - SiGe MODFETs (n-channel + p-channel)
  - 65 nm Strained Si RF-CMOS on SOI
- **Progress / Plans**

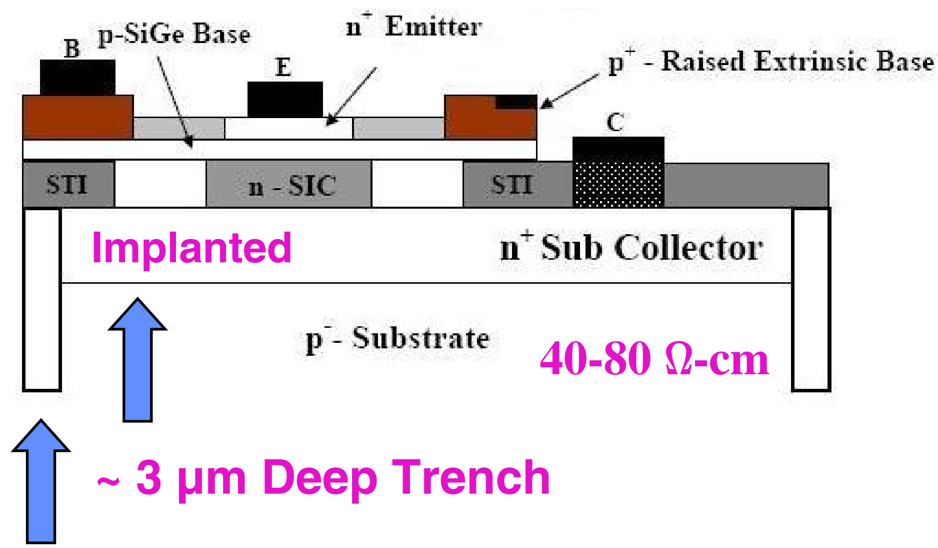
IBM 8WL SiGe BiCMOS

- **Cost-Performance Platform Incorporating 130 nm SiGe HBTs**
  - implanted subcollector **(much shallower subcollector-substrate jx)**
  - "shallow" deep trench isolation ~ **3 μm** **(vs. 8 μm for 8HP)**
  - lightly doped substrate ~ **40-80 Ω-cm** **(vs. 8-10 Ω-cm for 8HP)**
  - 100 / 200 GHz peak f_T / f_{max} **(vs. 200 / 285 GHz for 8HP)**

8HP SiGe HBT



8WL SiGe HBT



Q: Impact on Charge Collection / TID Response?

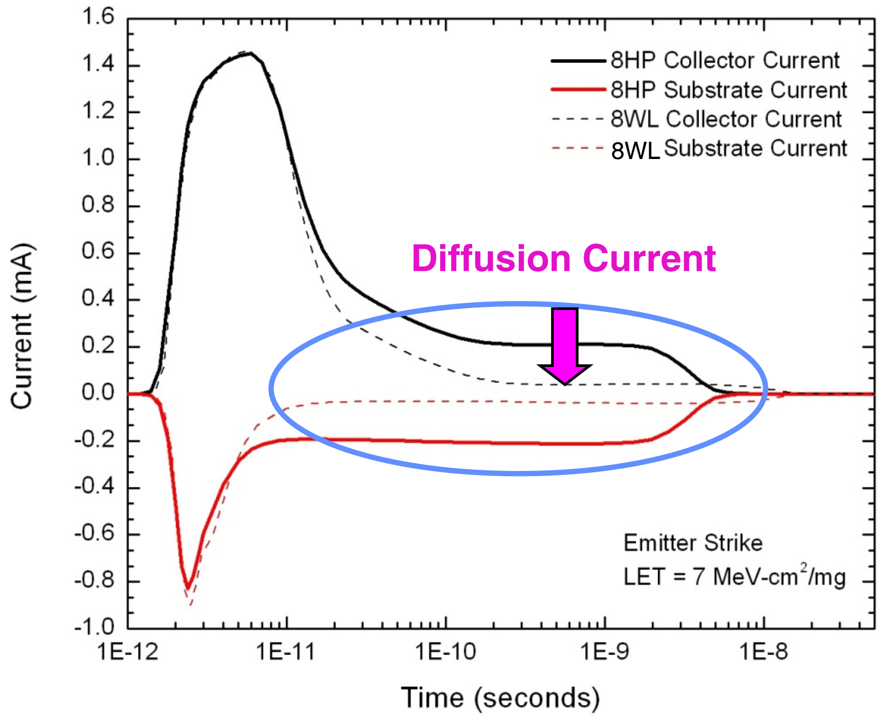
8HP vs. 8WL SEU

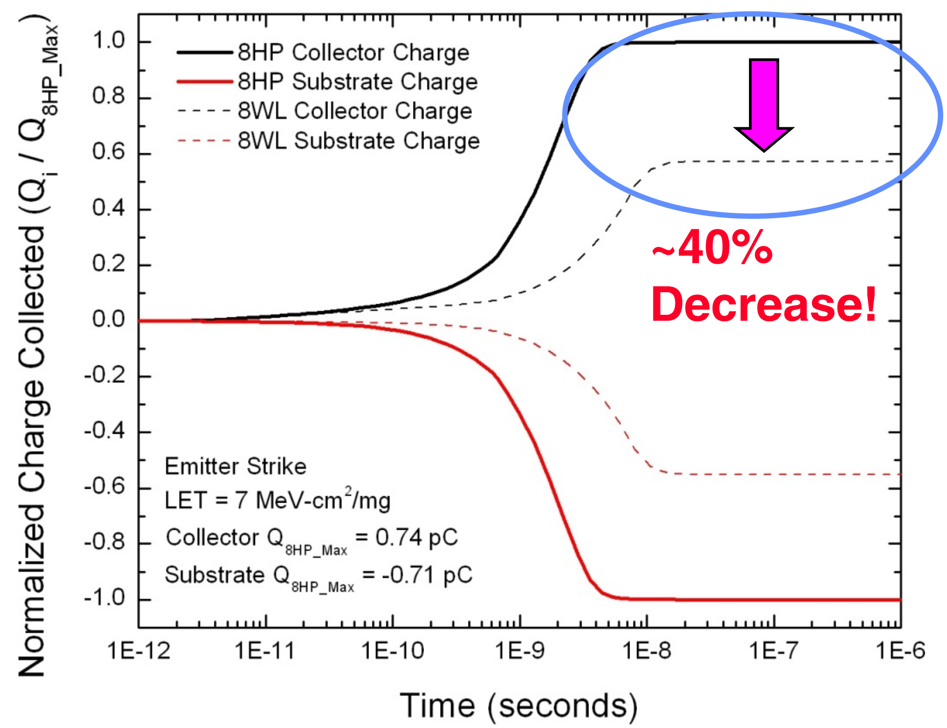
- **Drift-Dominated Charge Collection Similar for 8HP and 8WL**

  … BUT …

- **Diffusion- Dominated Charge Collection Suppressed in 8WL**

  Q: Less Charge Confinement Inside DT?



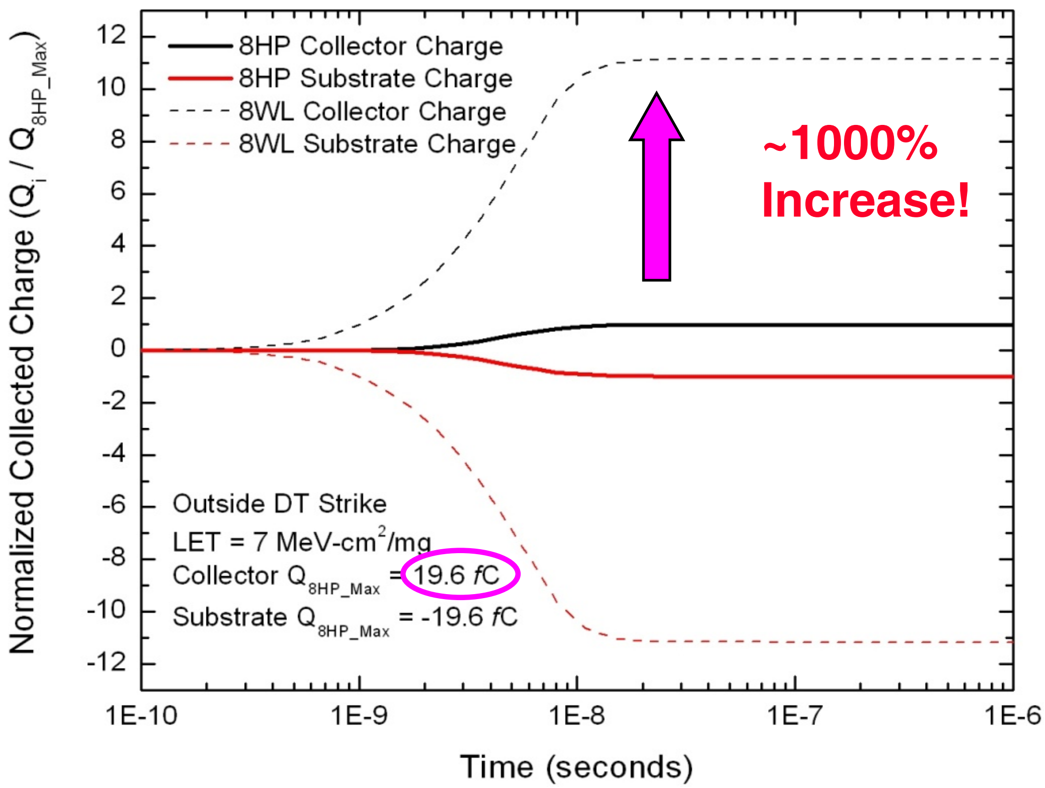


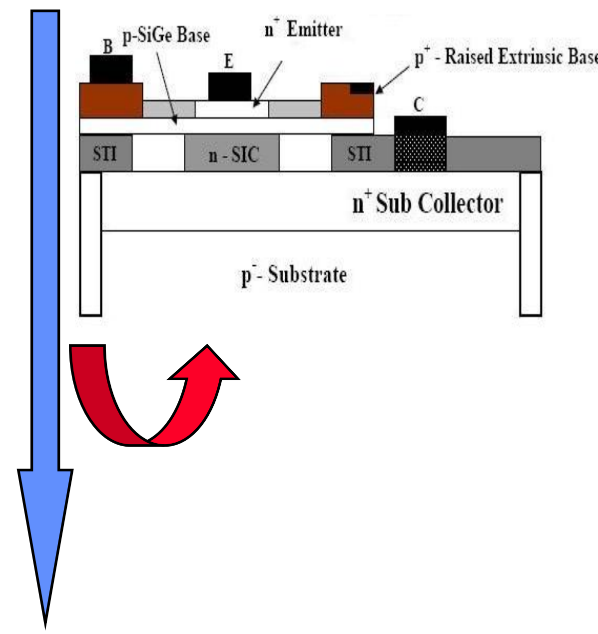
Emitter-Center Ion Strike

8HP vs. 8WL SEU

- **Shallower Deep Trench → less isolation for outside DT hit**
  - **more carrier diffusion (Q: higher substrate mobility / lifetime?)**

BUT … Small Absolute Change ⟹ Net Win for Charge Collection

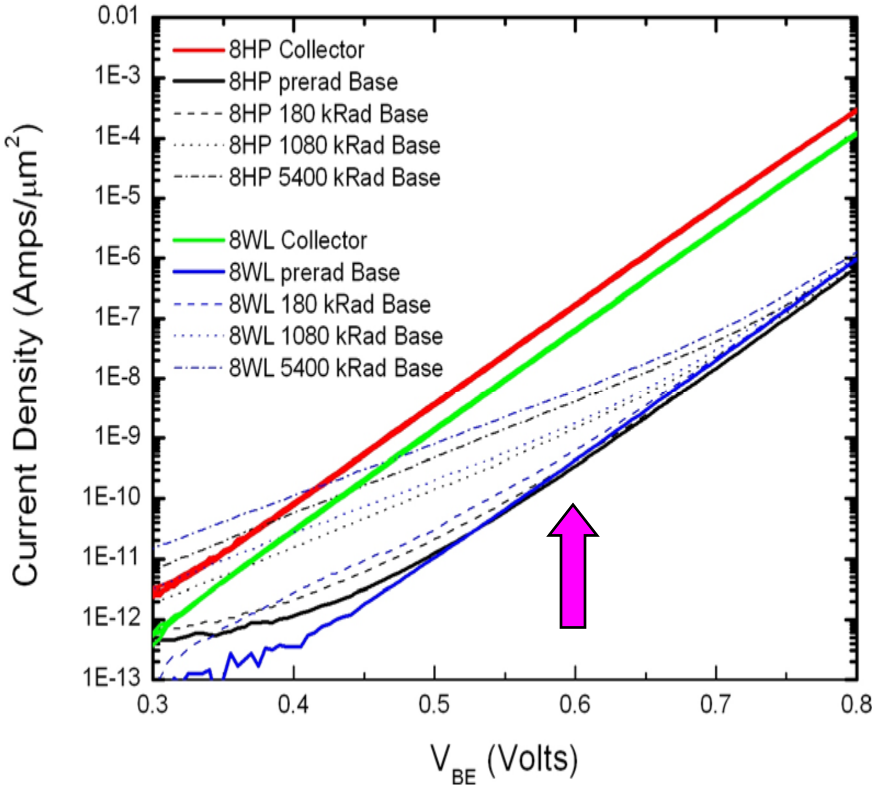


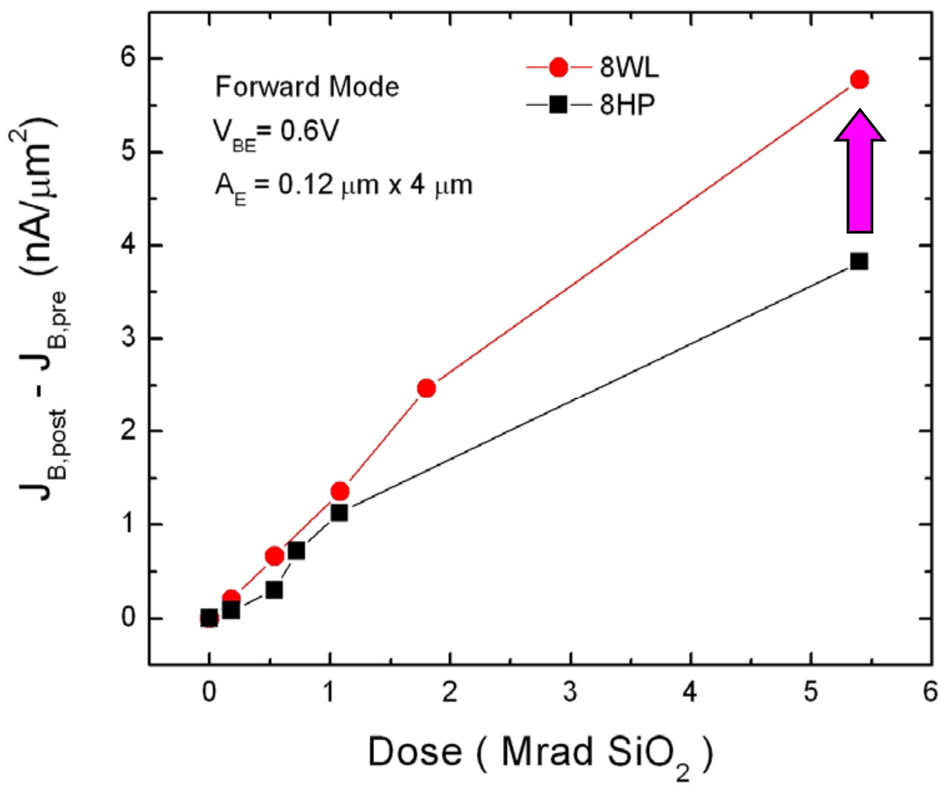


Outside Deep-Trench Ion Strike

8WL TID Response

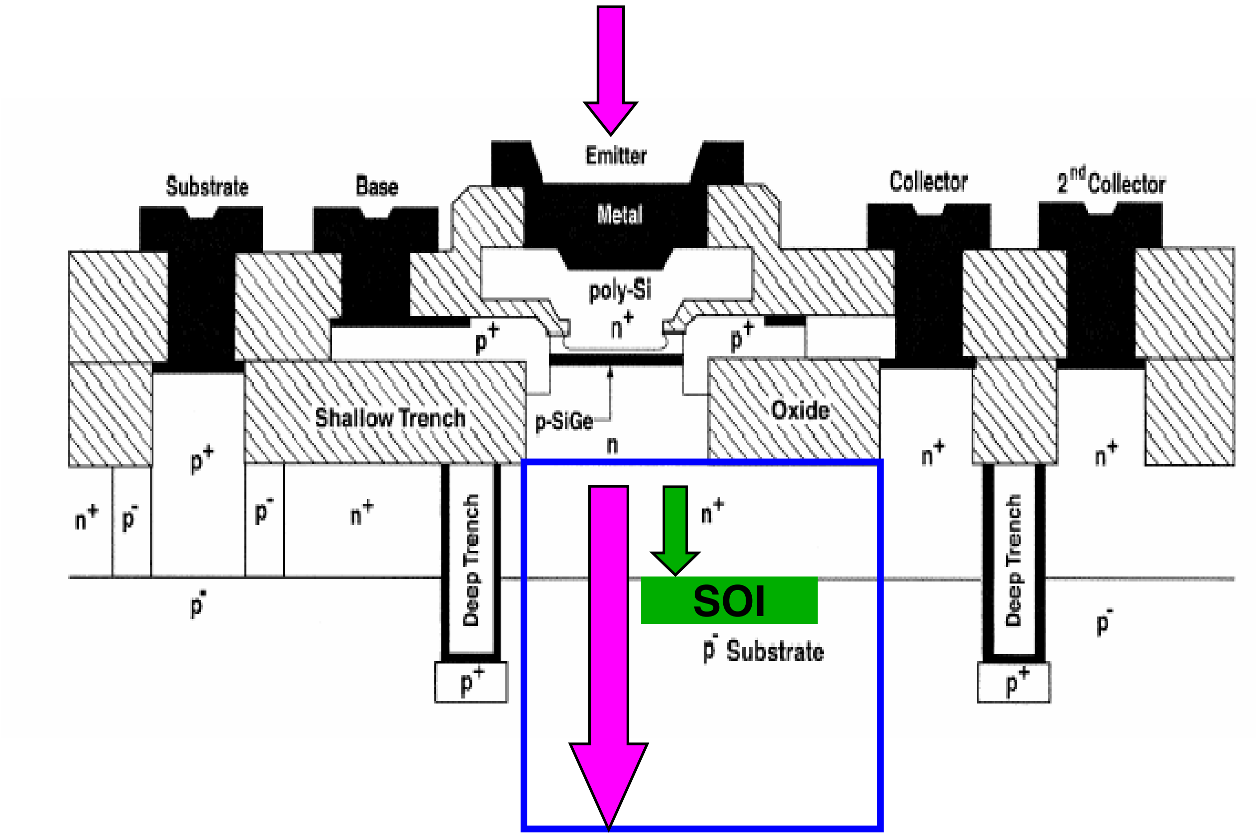
- **8WL & 8HP HBTs Irradiated up to 5.4 Mrad with 10 keV X-rays**
- **8WL Has Enhanced Degradation Compared to 8HP**
  - **Q: impact of different doping / vertical profile?**
  - **Q: differences in EB / STI oxide processing?**

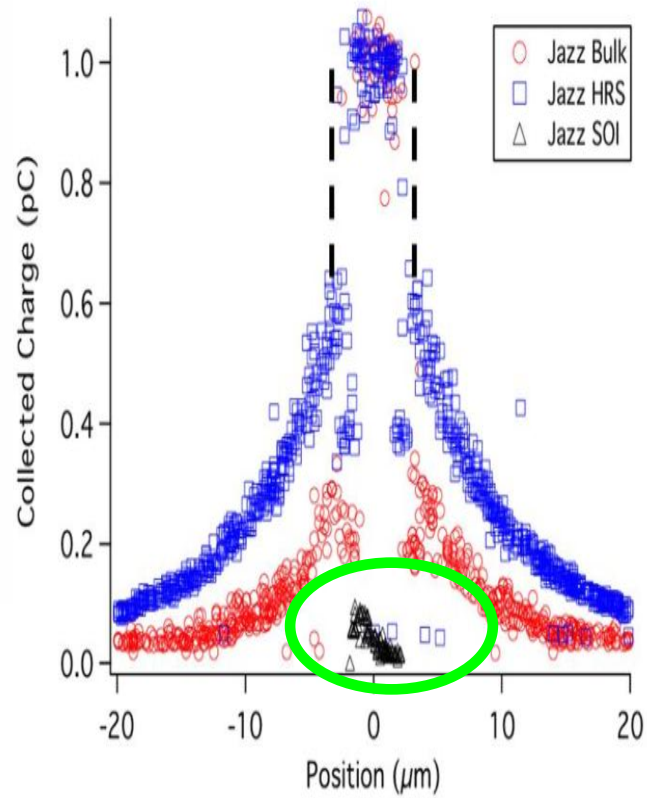




The Path to SiGe on SOI

- Collector-Substrate Junction Aids Charge Collection
- SOI Shuts Down Substrate Charge Collection Path

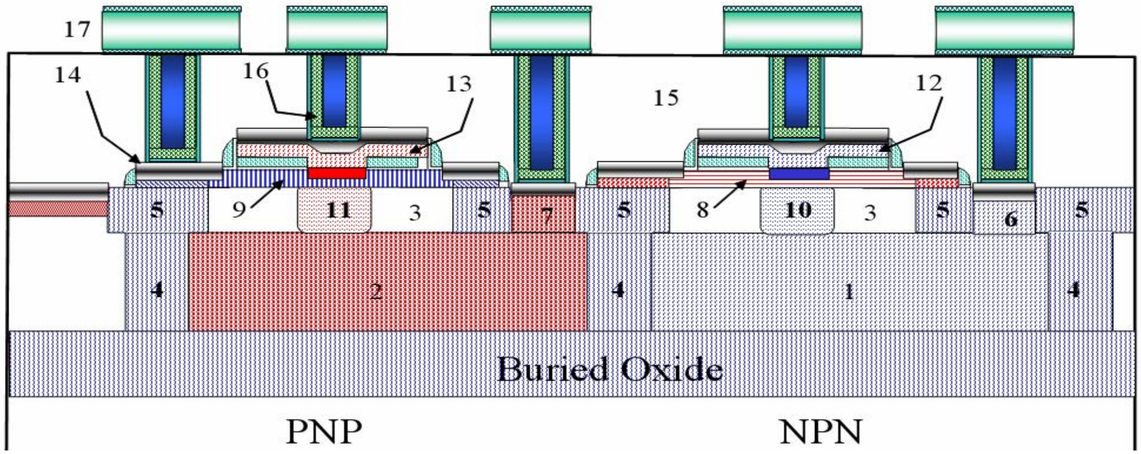




Pellish *et al.*

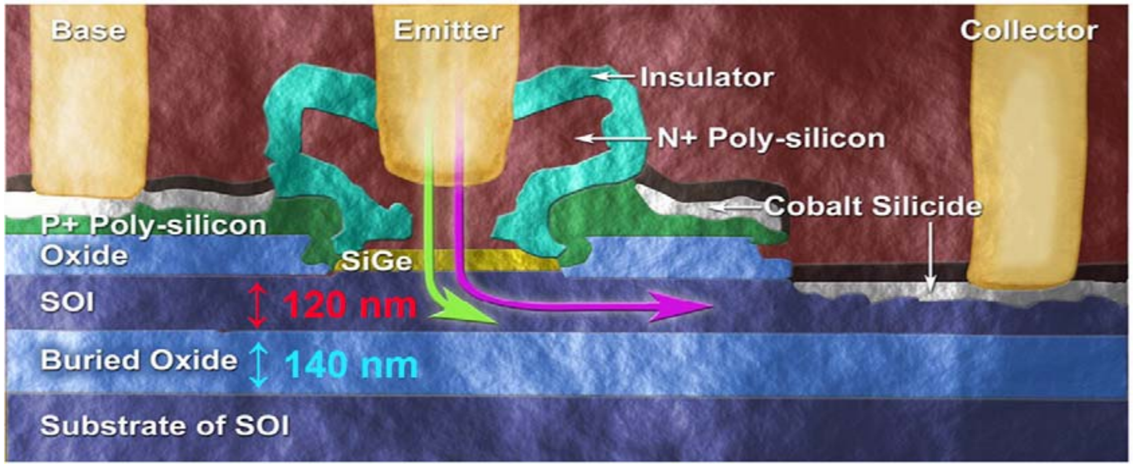
Thick vs Thin Film SOI

- Thick Film SiGe-on-SOI (TI) - works like a bulk SiGe HBT
- Thin Film SiGe-on-SOI (IBM) - VERY different device!



Thick-Film SOI

↕ 1.5 μm SOI

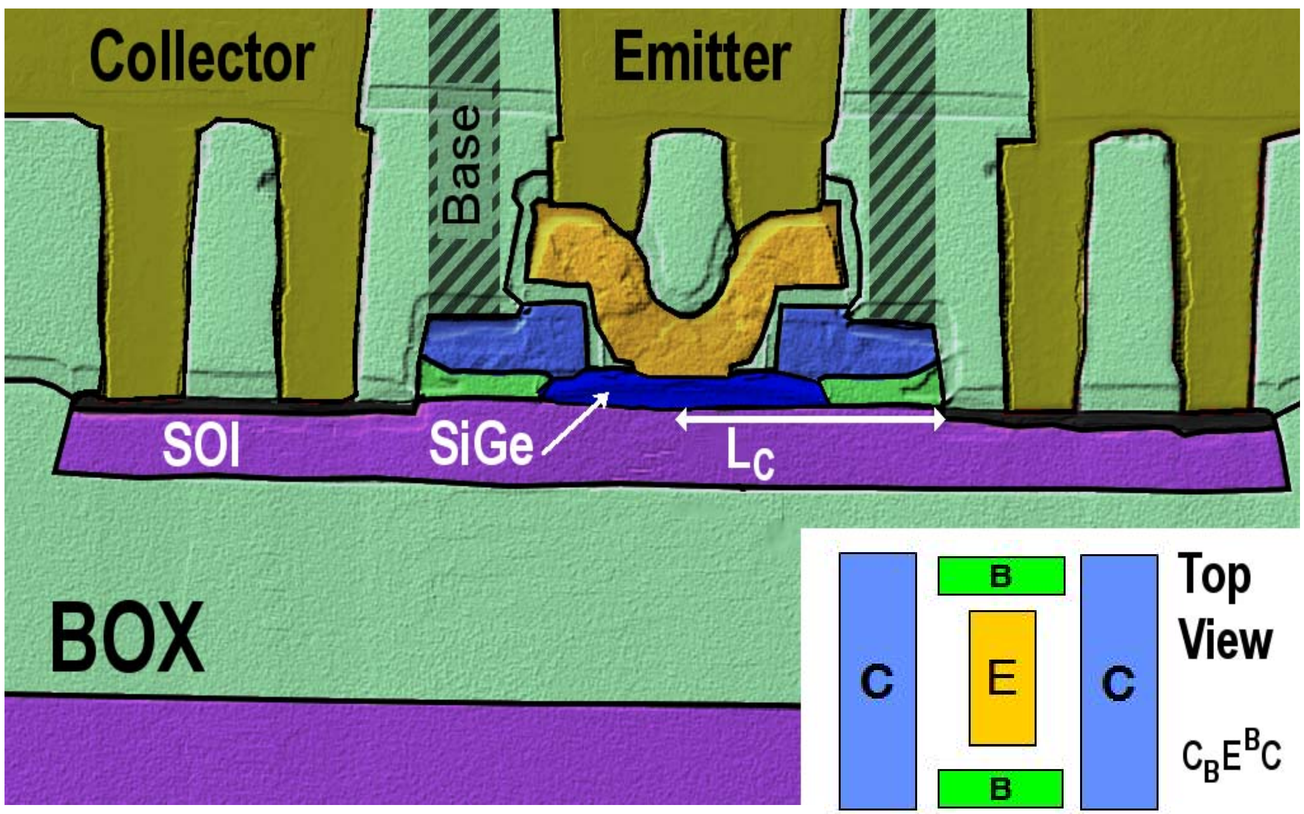


Thin-Film SOI

↕ 0.12 μm SOI

New SiGe/SOI Platform

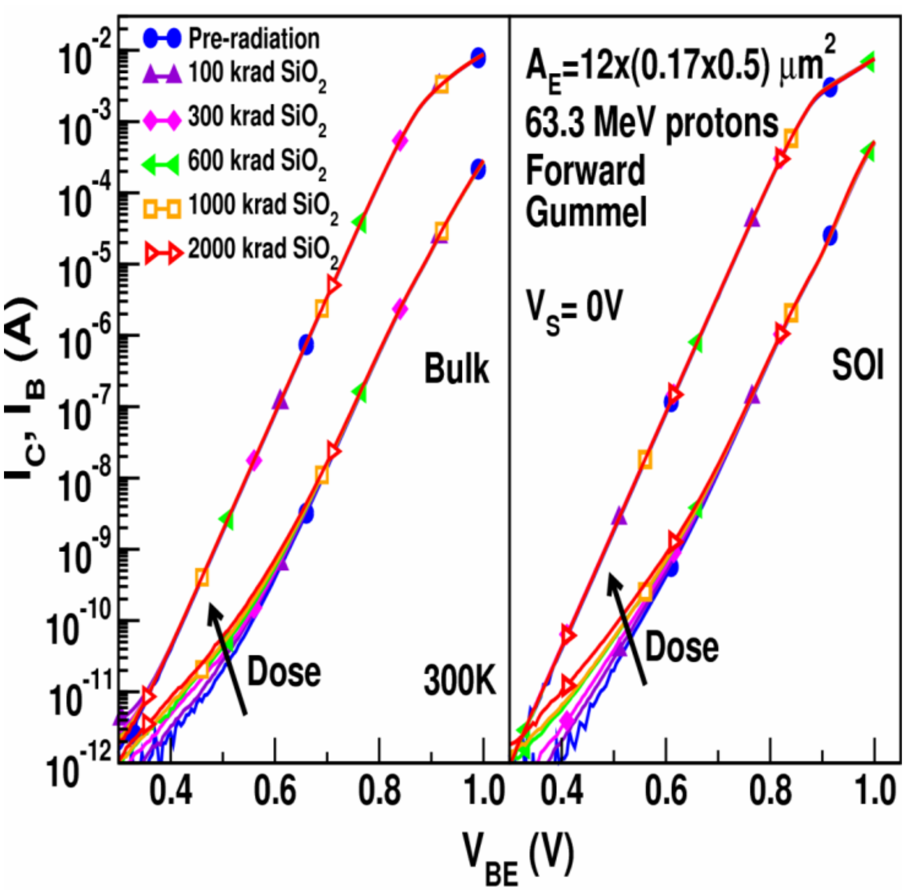
- **ST Microelectronics: SiGe HBT on Thin Film SOI**
  - compatible with 130 nm CMOS/SOI platform **(and C-SiGe!)**
  - uses a folded collector design (novel layout)
  - **npn SiGe HBT:** peak f_T / BV_{CEO} of 70 GHz / 2.3 V (34 / 5.5)
  - **pnp SiGe HBT:** peak f_T / BV_{CEO} of 39 GHz / 2.9 V (17 / 6.7)



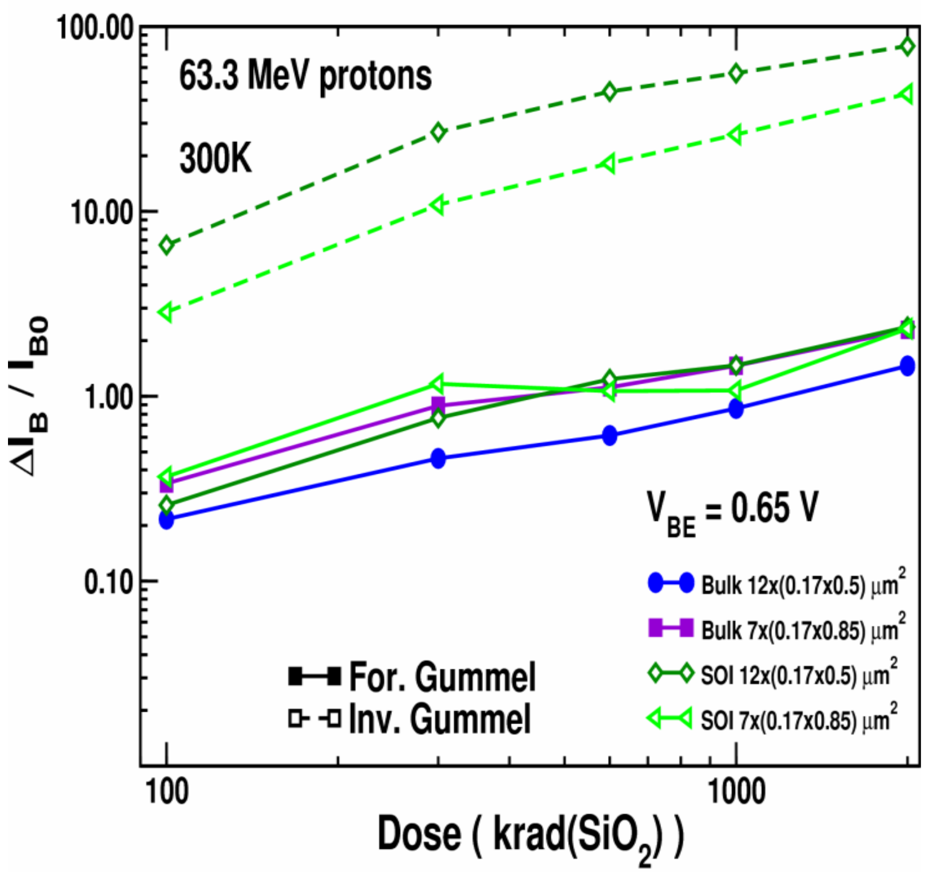
Proton DC Response

- SOI and Bulk Devices with Identical EB Structure
- No Degradation Introduced by SOI

Bulk SiGe HBT SiGe HBT on SOI

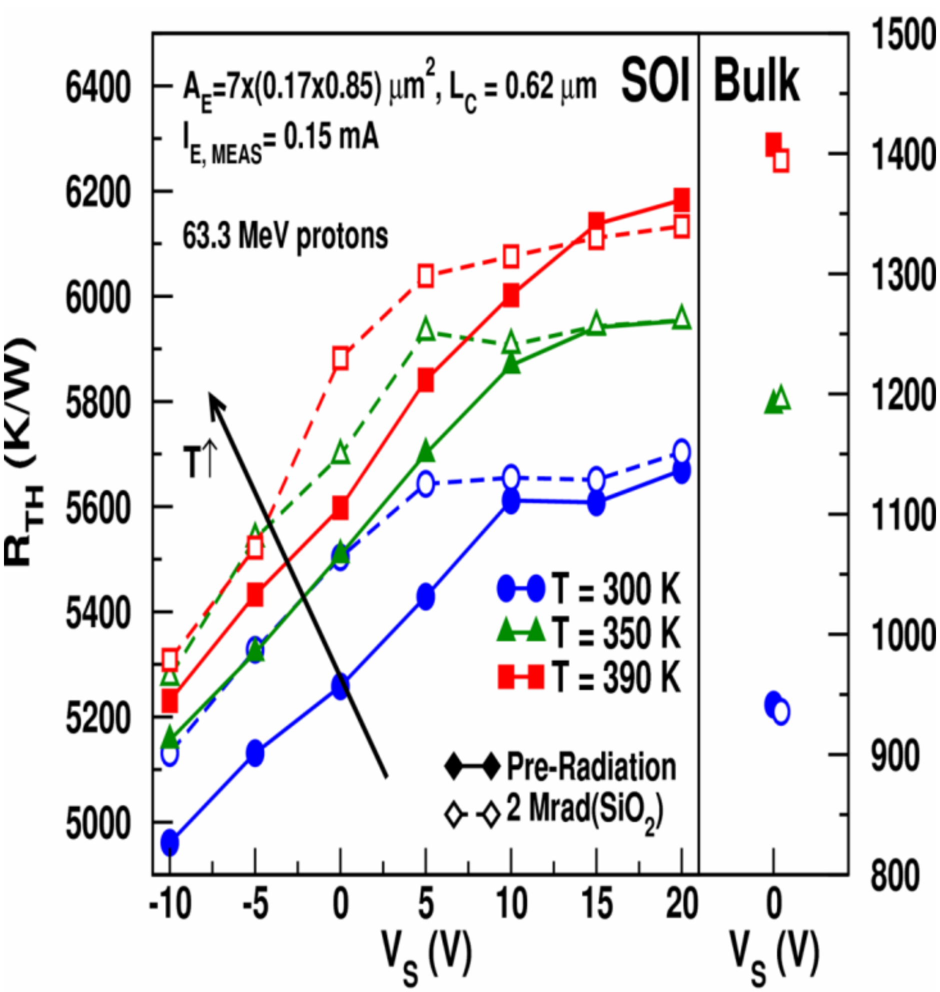


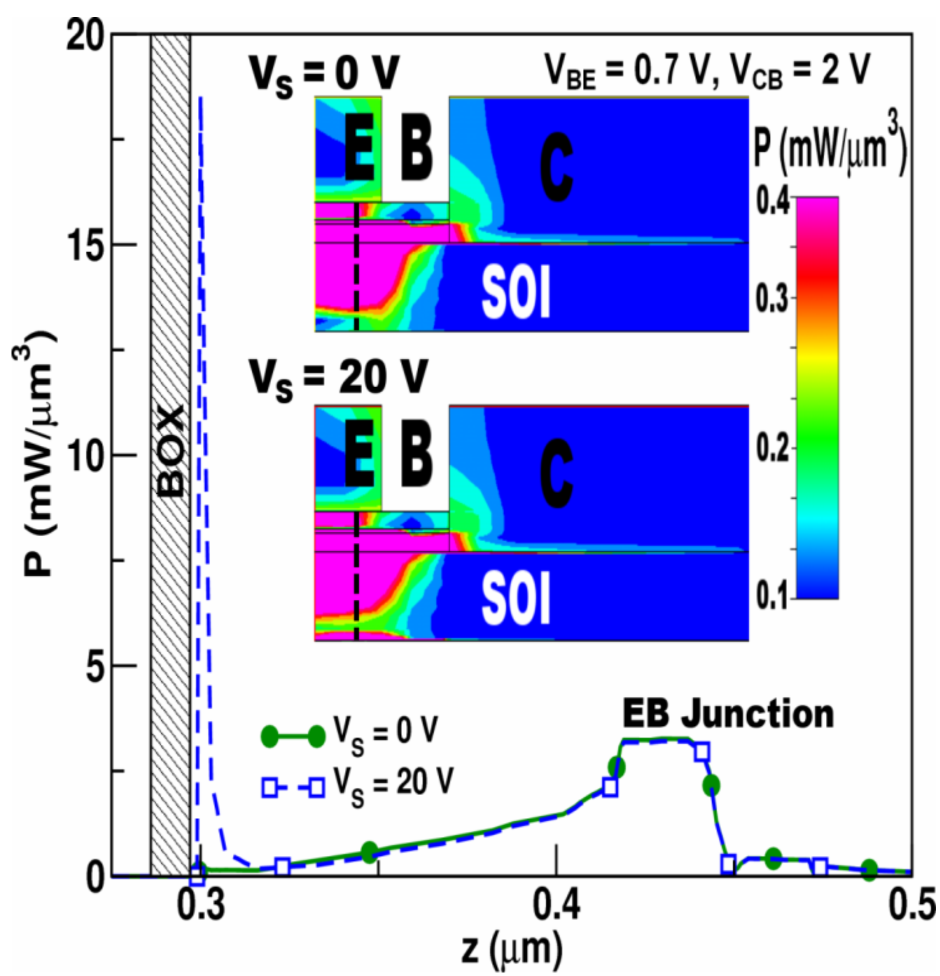
Excess Base Current



Thermal Resistance

- R_{TH} of HBT-on-SOI Increases with V_S and Radiation
- More Power Dissipated at the SOI / BOX Interface

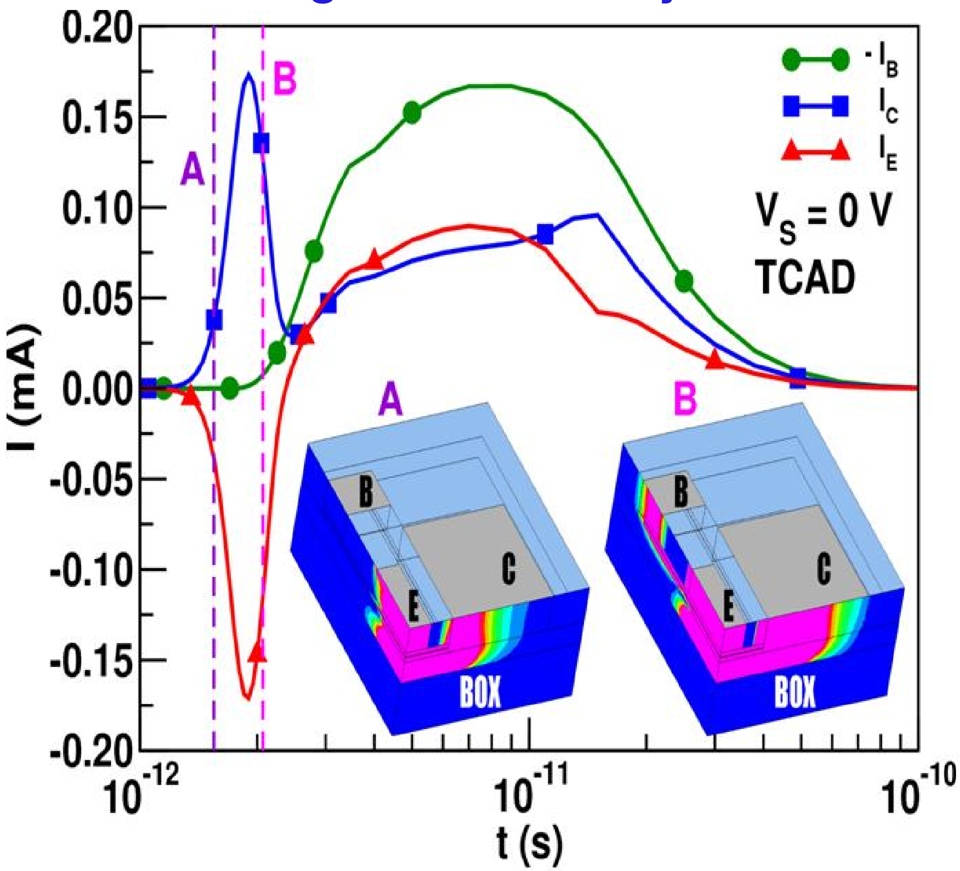




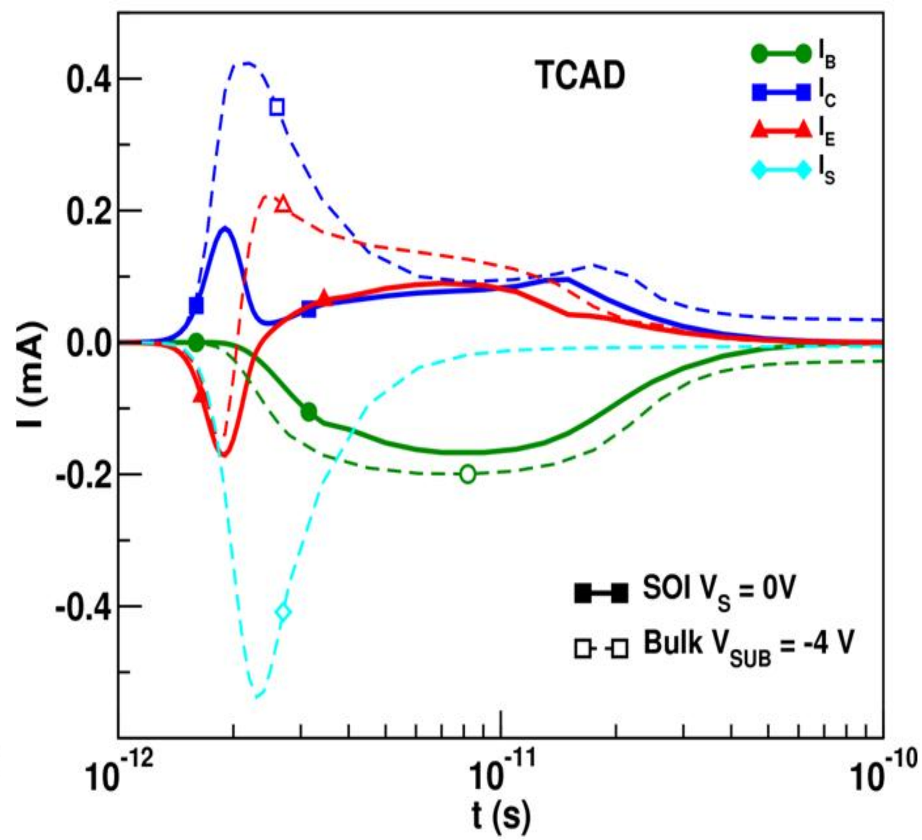
SEU TCAD in SiGe/SOI

- Unusual Charge Collection Dynamics (true 3-D effects)
- Strong SEU Advantage for SOI Compare to Bulk

Charge Collection Dynamics



SOI vs Bulk SiGe HBT



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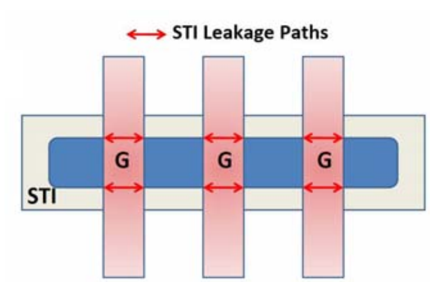
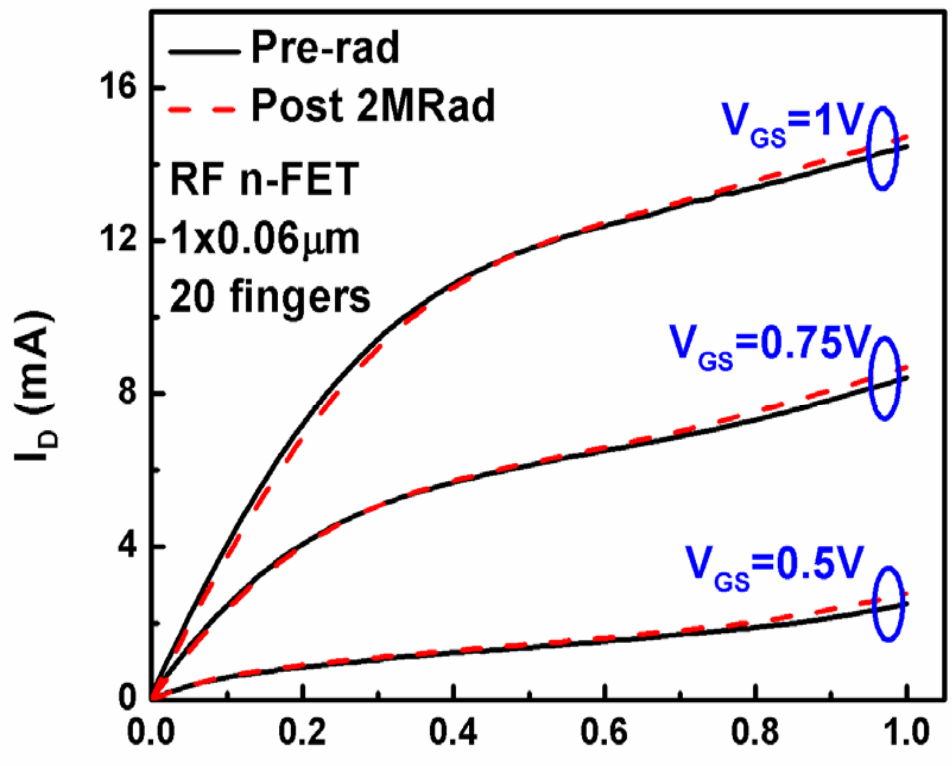
- **Progress / Plans**

65nm SOI RF-CMOS (DC)

- **65 nm RF-CMOS on SOI (IBM) – Uses Strain Engineering**
- **High f_T / f_{max} in CMOS Comes Only at VERY High W (# fingers)**
- **Impact of Radiation-Induced Damage on DC Characteristics**
  - sub-threshold degradation + enhanced floating body effects

V_{DS} = 50 mV

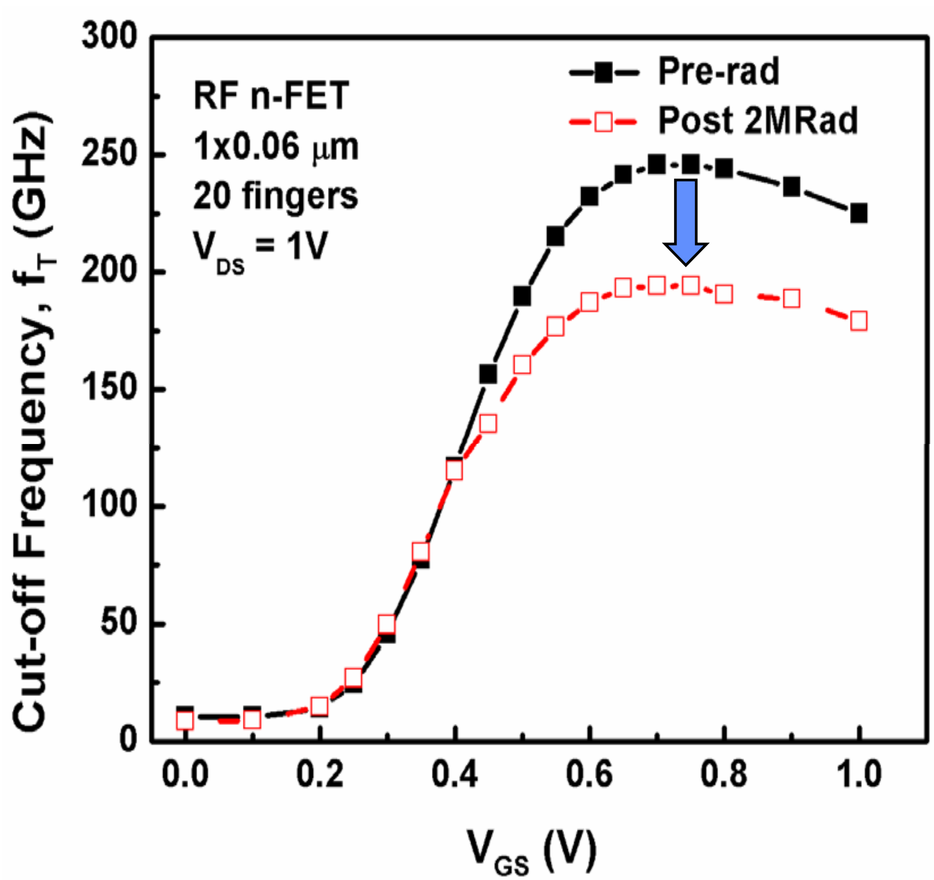


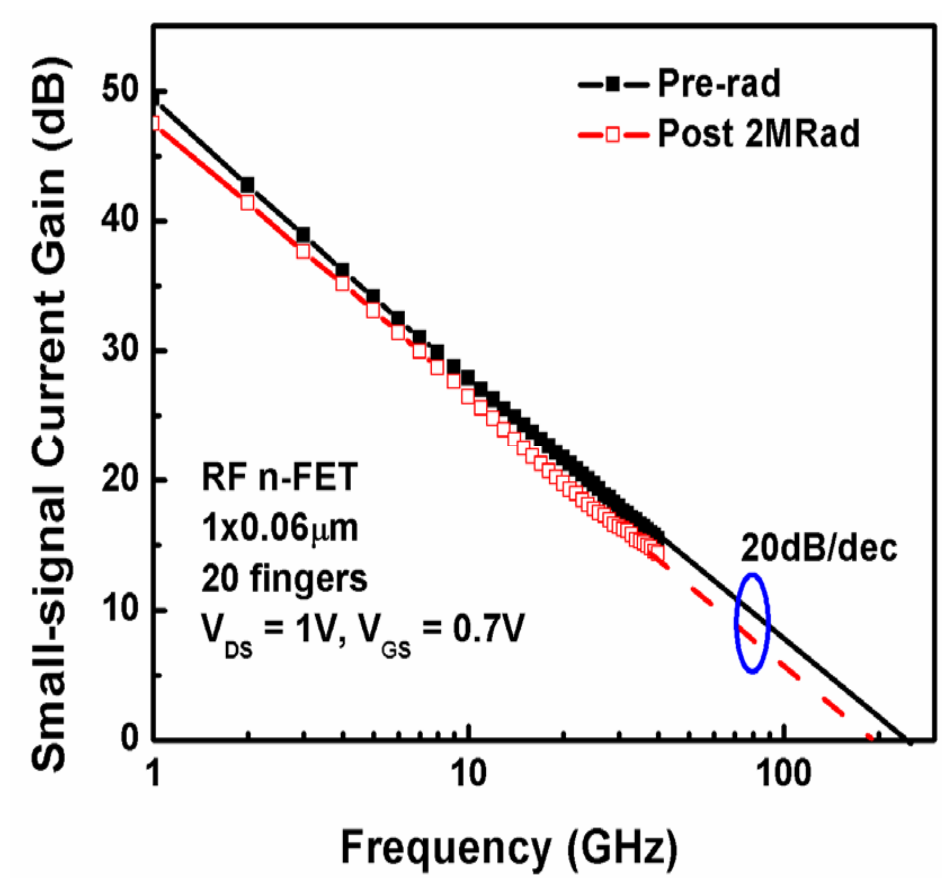


63 MeV Protons

65 nm SOI RF-CMOS (AC)

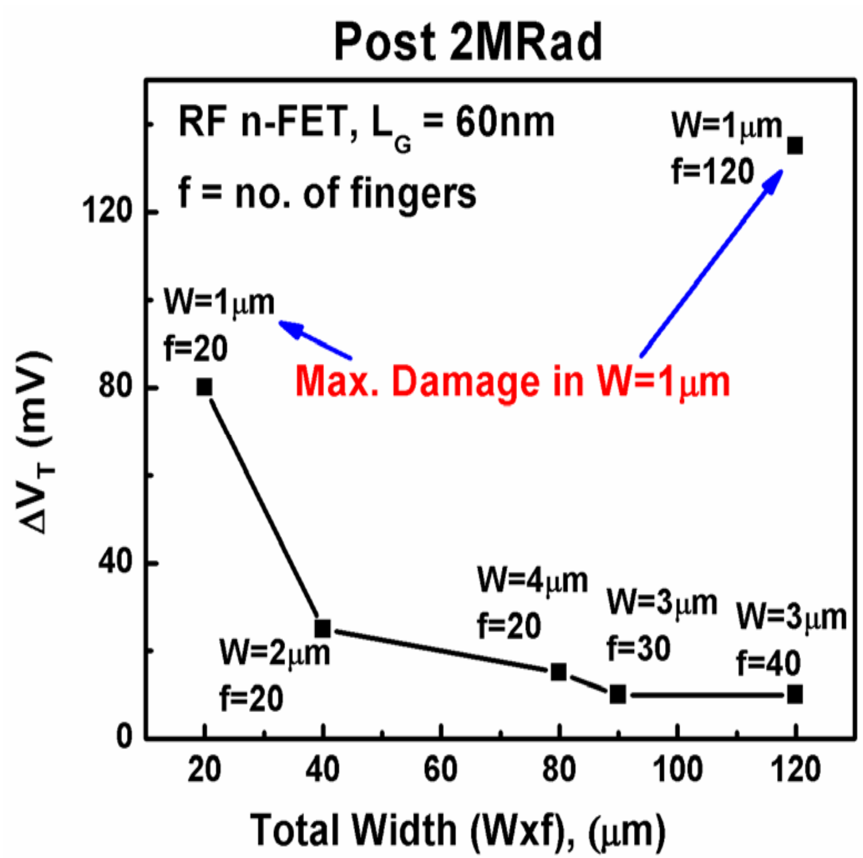
- **Radiation Impact on RF Characteristics of 65 nm RFCMOS/SOI**
  - 63 MeV Proton irradiation degrades f_T considerably
  - h_{21} degradation observed at 2 Mrad total dose

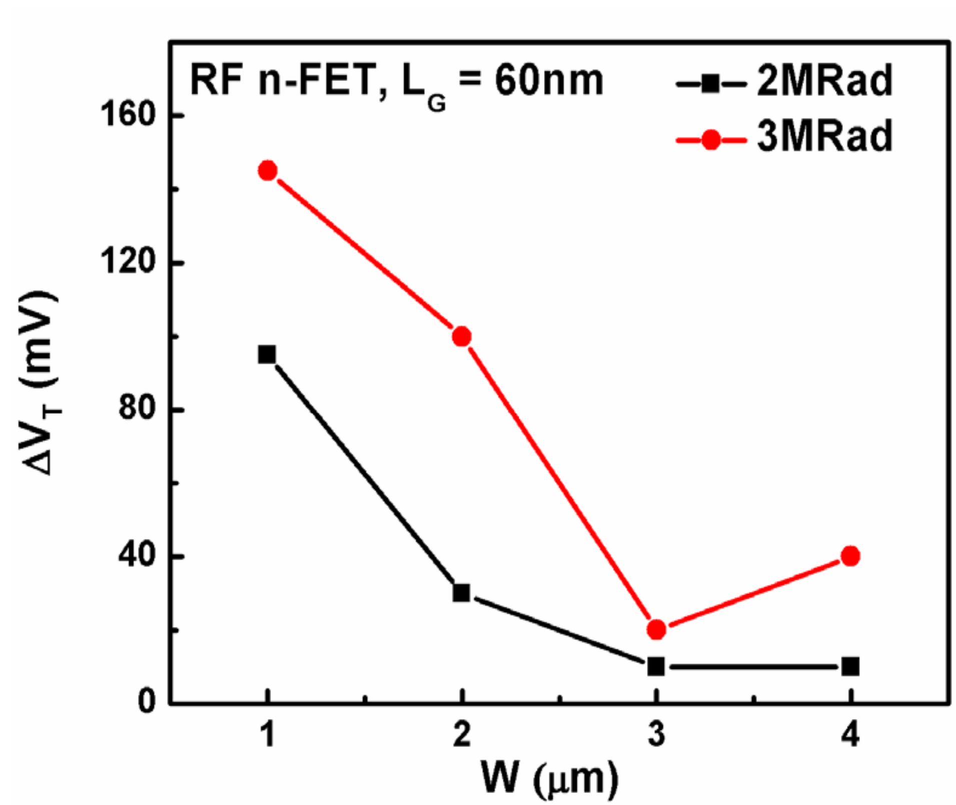




Geometrical Issues

- **Impact of Radiation-Induced Damage on DC Characteristics**
  - damage is highly W dependent
  - suggestive of STI sidewall parasitic conduction (not BOX)
  - **response of logic nFET very different than RF nFET**





Progress / Plans

- **SiGe Offers Great Potential for Many DoD Applications**
  - SiGe HBT + Si CMOS (RF to mm-wave + analog + digital for SoC / SoP)
- **Many Issues in SiGe Still Need Attention**
  - improved understanding of basic damage mechanisms (TID + SEE)
  - understand the effects of temperature on damage mechanisms / SEE
  - need to assess SET in analog/mixed-signal SiGe circuits **(in progress)**
  - explore other SiGe HBT variants (SiGe HBT on SOI, C-SiGe, etc.)
  - explore other (new) SiGe-based devices (SiGe n/p-MODFETs, RF-CMOS)
  - develop new RHBD approaches (device + circuit) for SEE mitigation
  - need improved 3D TCAD for understanding SEE (and TID)
- **Lots of Leverage for SiGe Hardware / Testing Activity**
  - **many** SiGe tapeouts (IBM, IHP, TI, Jazz, ST): **devices + circuits**
  - DTRA / NASA-NEPP (Paul Marshall)
  - NASA SiGe ETDP Project (RHESE)
  - CFDRC SBIR (DTRA / NASA) for Improved TCAD for SEU / Cryo-T, etc.
  - excellent collaboration between Georgia Tech and Vanderbilt teams

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