Modeling Total Ionizing Dose Effects in Deep Submicron CMOS Technologies

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Acknowledgements

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Motivation

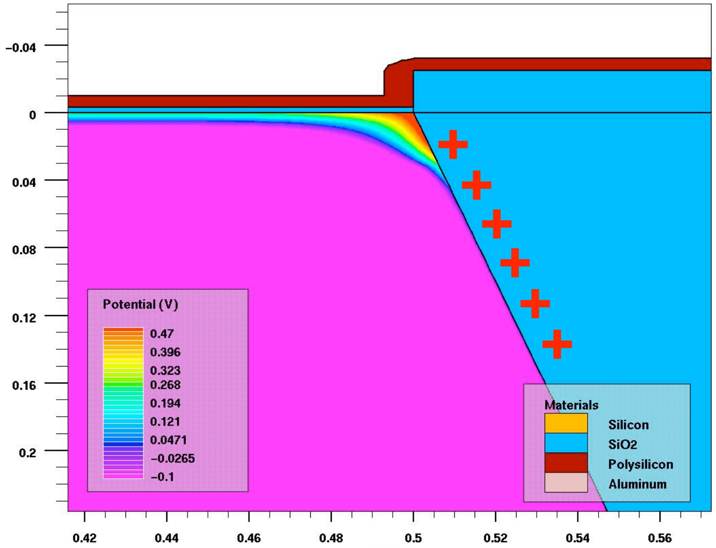
- Characterize and model radiation damage effects in modern CMOS device technologies
- Technologies:
  - deep submicron bulk CMOS,
  - silicon on insulator (El-Mamouni - VU, Sanchez - ASU)

Previous Research

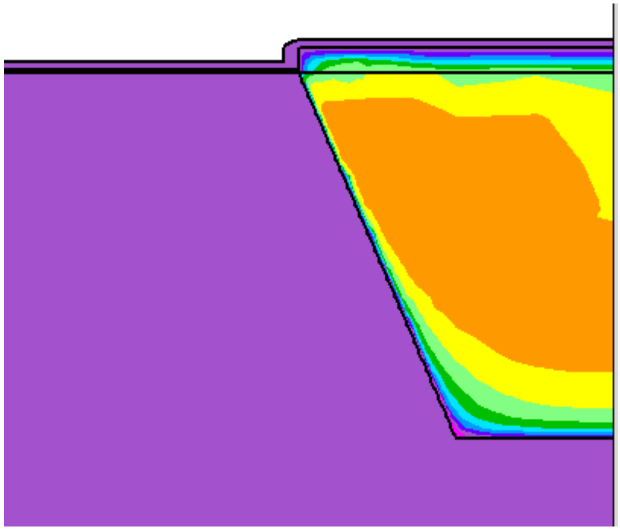
- May 2005 - “Device-level Radiation Effects Modeling”

  Overview of numerical (TCAD) simulation approaches to modeling radiation effects in CMOS devices

Sheet Charge



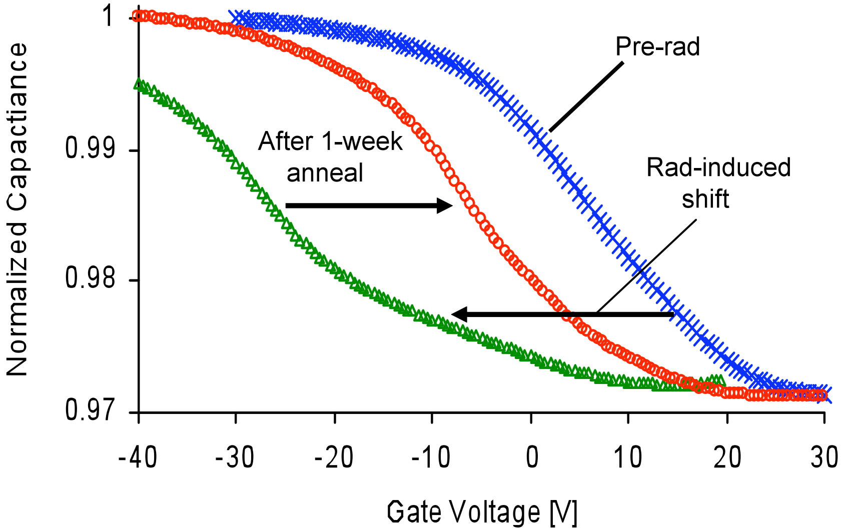
Trapped Charge vol. distribution

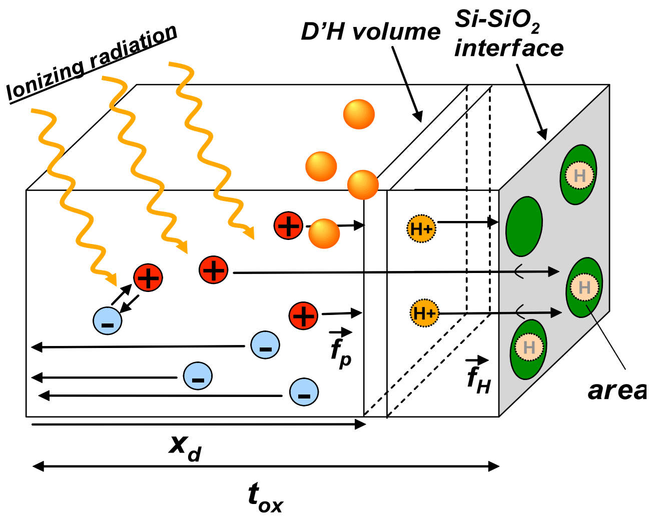


Previous Research

- June 2006 - “Total Ionizing Dose Effects in Bulk Technologies and Devices”

  Characterize, parameterize TID effects. Formalize closed form analytical expressions for TID effects in devices (130nm CMOS).





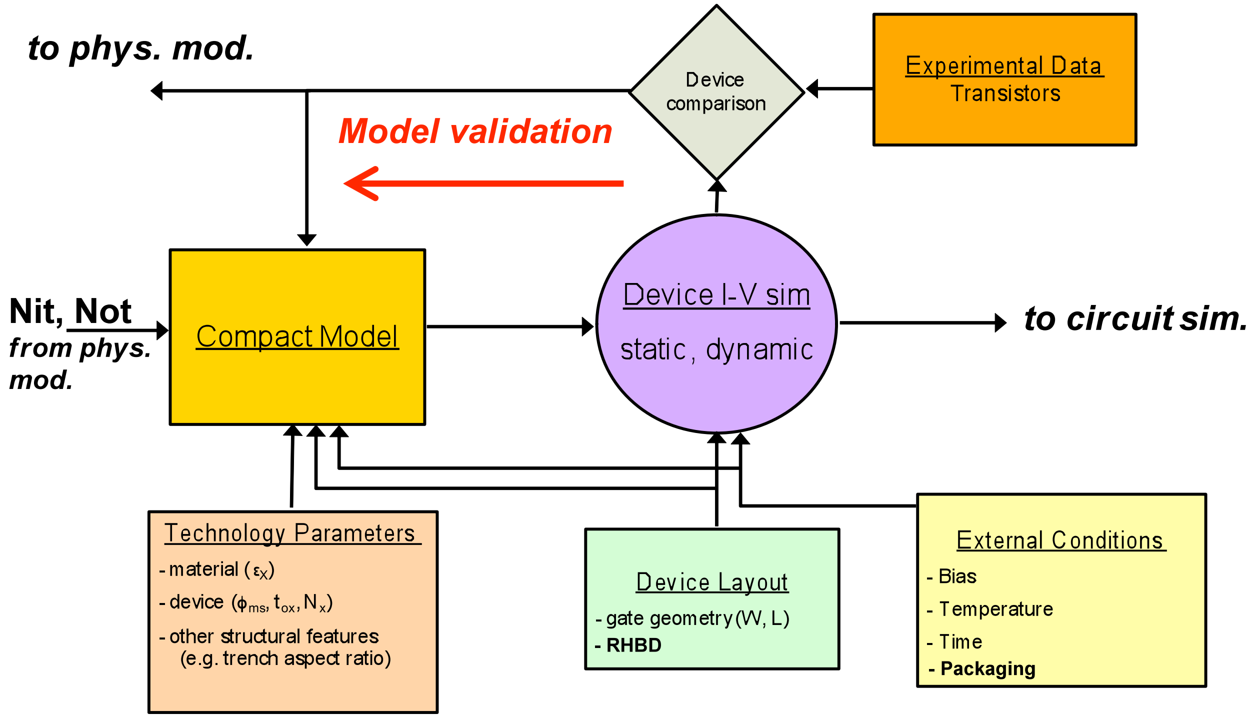
$$\Delta N_{ot} \approx D k_g f_y(\vec{\varepsilon}) f_{ot}(\vec{\varepsilon}) t_{ox}$$

$$\Delta N_{it} \approx D k_g f_y(\vec{\varepsilon}) f_{DH} f_{it} t_{ox}$$

Previous Research

- June 2007 - “Modeling Total Ionizing Dose Effects in Deep Submicron Bulk CMOS technologies”

  Description and initial validation of radiation-enabled compact modeling approach for CMOS technologies (≥ 90nm CMOS).



to phys. mod.

Device comparison

Experimental Data
Transistors

Model validation

Nit, Not *from phys. mod.*

Compact Model

Device I-V sim
static, dynamic

to circuit sim.

Technology Parameters
- material (ε_X)
- device (ϕ_{ms}, t_{ox}, N_x)
- other structural features (e.g. trench aspect ratio)

Device Layout
- gate geometry (W, L)
- **RHBD**

External Conditions
- Bias
- Temperature
- Time
- **Packaging**

Previous Research

- May 2008 – Surface potential-based analytical modeling of TID effects in bulk CMOS devices

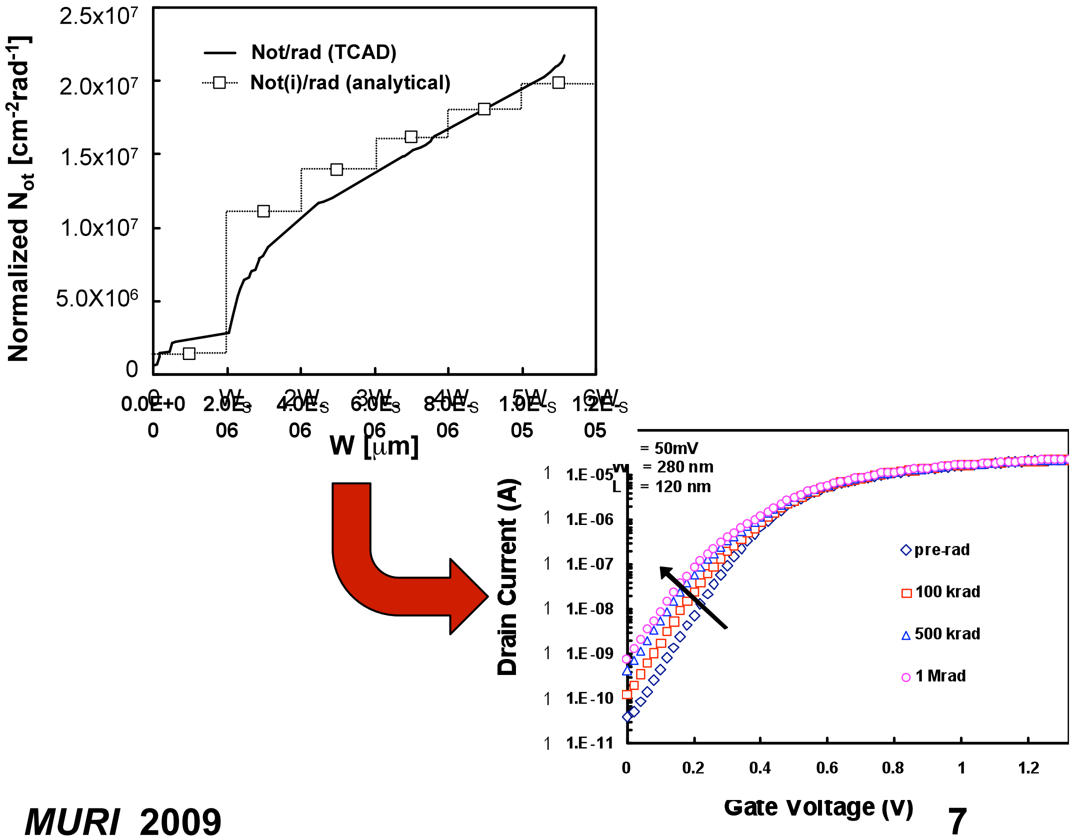
  Closed form analytical models used to estimate charge build-up in STI sidewall and fit degraded I-V characteristics in nFETs

$$t_{ox}(i)$$

$$\varepsilon_{ox}(i) \approx \frac{V_{gb}}{t_{ox}(i)}$$

$$f_y(i) \approx \frac{\varepsilon_{ox}(i)}{\varepsilon_{ox}(i) + \varepsilon_0}$$

$$\Delta N_{ot}(i) \approx N_T \sigma D g_o f_y(i) t_{ox}(i)$$



Recent Work (2009)

- **Demonstration of analytical model of TID effects on bulk CMOS isolations oxides**
  - **Revised analytical model for TID defect buildup compared to FOXFET I-V and TCAD simulations**
  - **Demonstration of modeling approach: SRAM with reverse body bias**
- **Effects of Channel Implant Variation on Edge Leakage Currents**
- **Modeling TID effects in Multiple Gate FETs**

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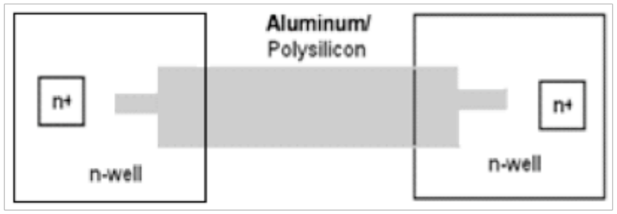
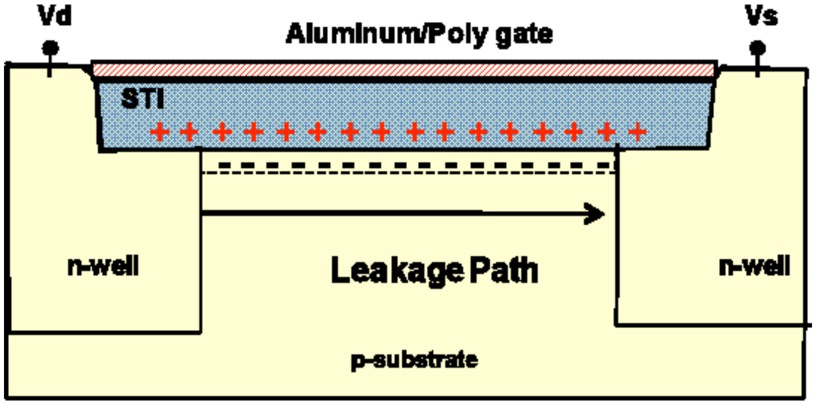
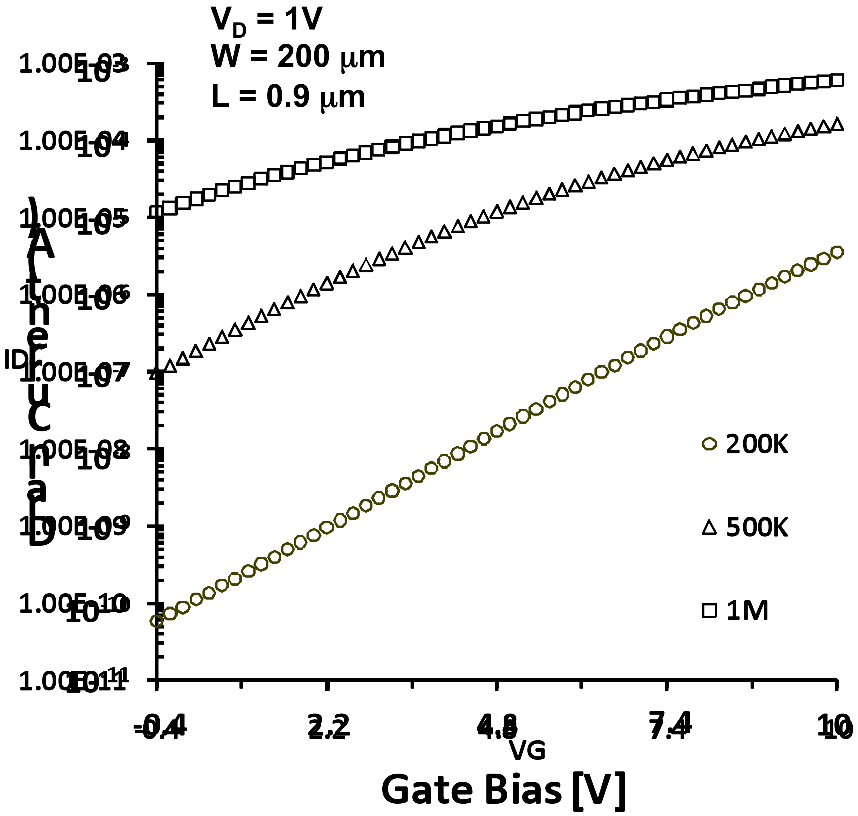
Field Oxide FET Measurements

TID experiments on FOXFETS used to calibrate the analytical model







- ^{60}Co irradiation source (DR ~ 20 rad/s)
- 90 nm LP technology

Defect Extraction

Defect potential in SP equations used to fit FOXFET data

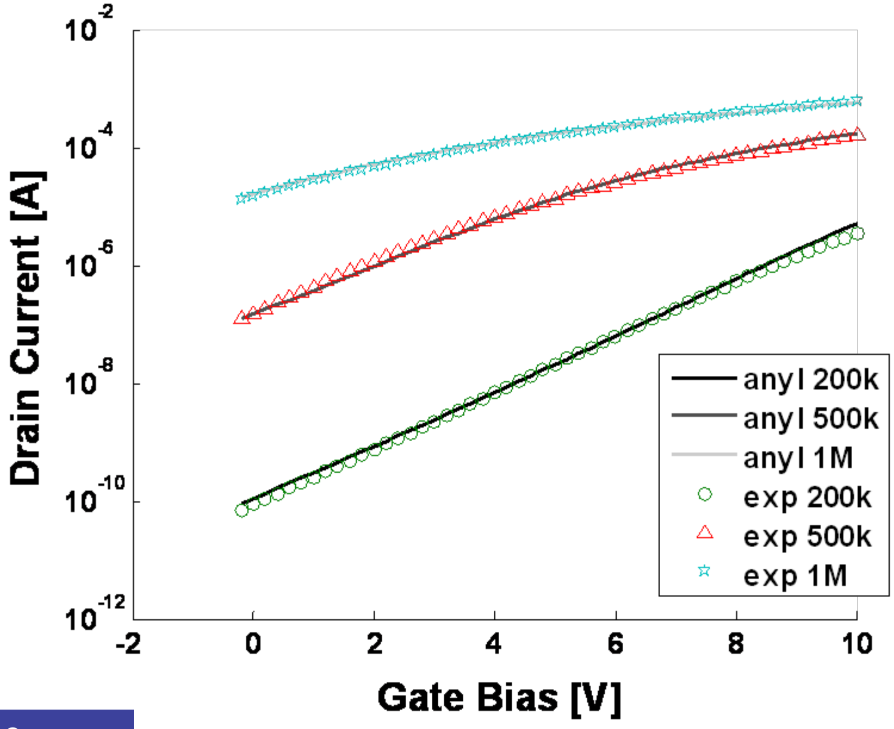
$$I_{Drift} = (V_{gb} - V_{fb})(\psi_{sd} - \psi_{ss}) - \frac{1}{2}(\psi_{sd}^2 - \psi_{ss}^2)$$

$$- 2\frac{\gamma}{3}\left[(\psi_{sd} - \varphi_t)^{3/2} - (\psi_{ss} - \varphi_t)^{3/2}\right]$$

$$I_{Diff} = \varphi_t\left(\psi_{sd} - \psi_{ss} + \gamma\left(\sqrt{\psi_{sd} - \varphi_t} - \sqrt{\psi_{ss} - \varphi_t}\right)\right)$$

$$(V_{gb} - \varphi_{ms} + \varphi_{nt} - \psi_s)^2 = \gamma^2 \cdot \varphi_t H(u)$$

$$\varphi_{nt} = \frac{q}{C_{ox}}\left(N_{ot} - D_{it} \cdot (\psi_s - \varphi_b)\right)$$



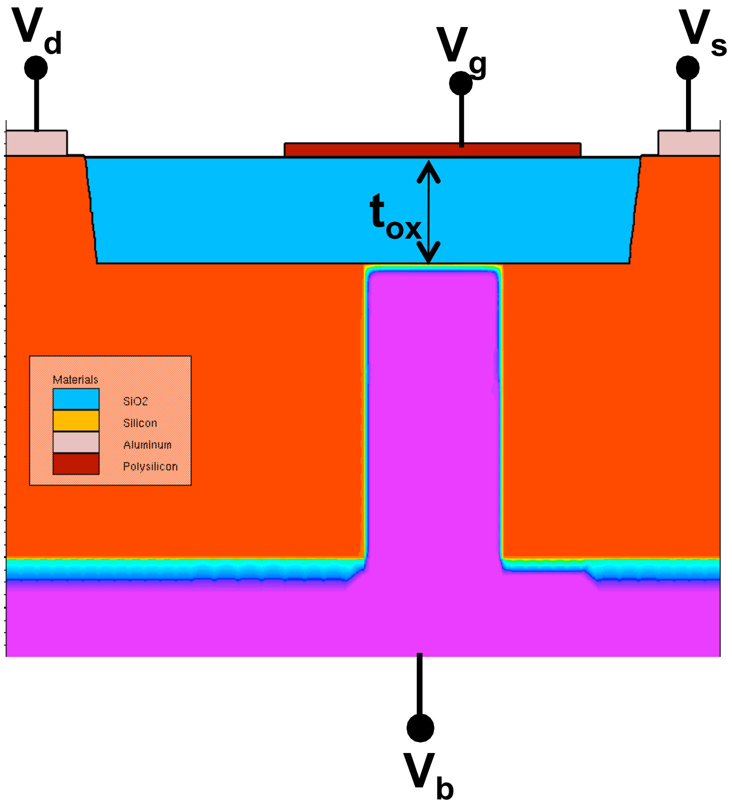
Fit w/ analytical model

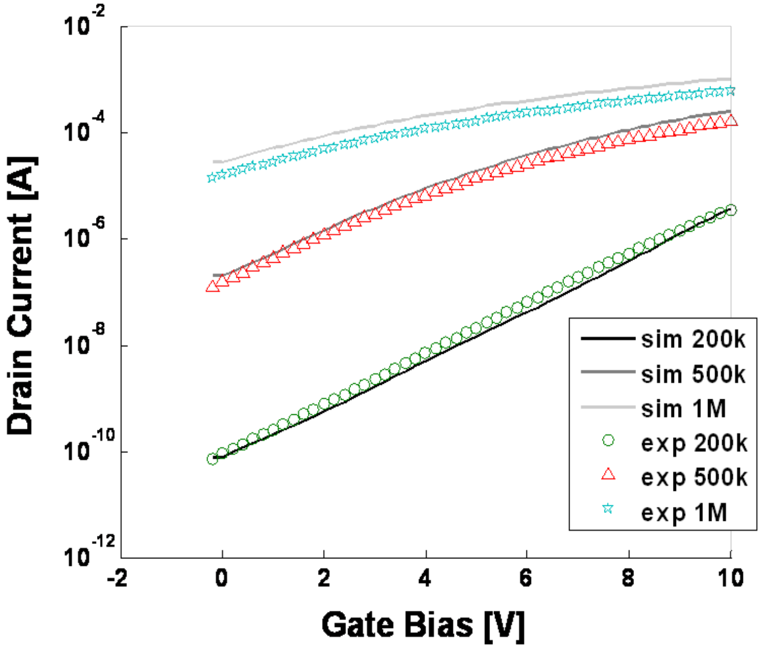
Dose [krad(Si)]	N_{ot} (cm^{-2})	D_{it}(cm^{-2}/V)
200	1.92×10^{12}	2.6×10^{11}
500	2.39×10^{12}	6.0×10^{11}
1000	2.75×10^{12}	8.0×10^{11}

Fit based on approximations for oxide thickness, body doping, workfunction, etc.

TCAD Validation

TCAD sims performed on FOXFET structure validate fit



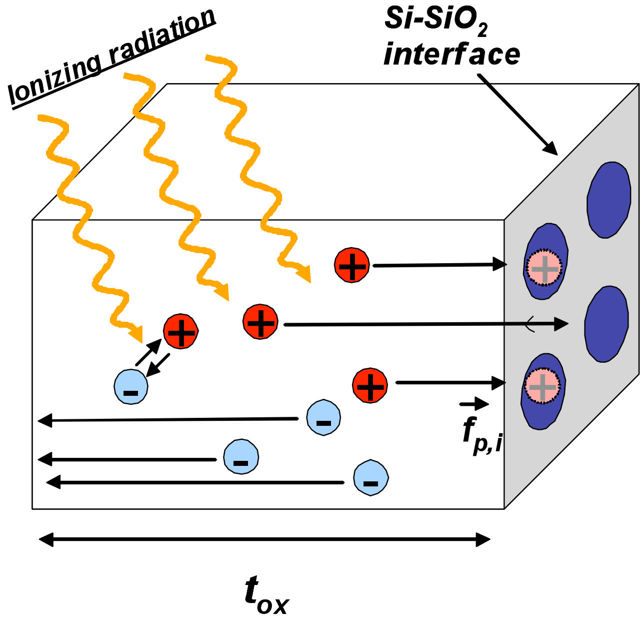


Fit w/ TCAD model

Dose [krad(Si)]	N_{ot} (cm^{-2})	D_{it}(cm^{-2}/V)
200	$1.82\text{x}10^{12}$	$2.99\text{x}10^{11}$
500	$2.29\text{x}10^{12}$	$6.89\text{x}10^{11}$
1000	$2.65\text{x}10^{12}$	$9.18\text{x}10^{11}$

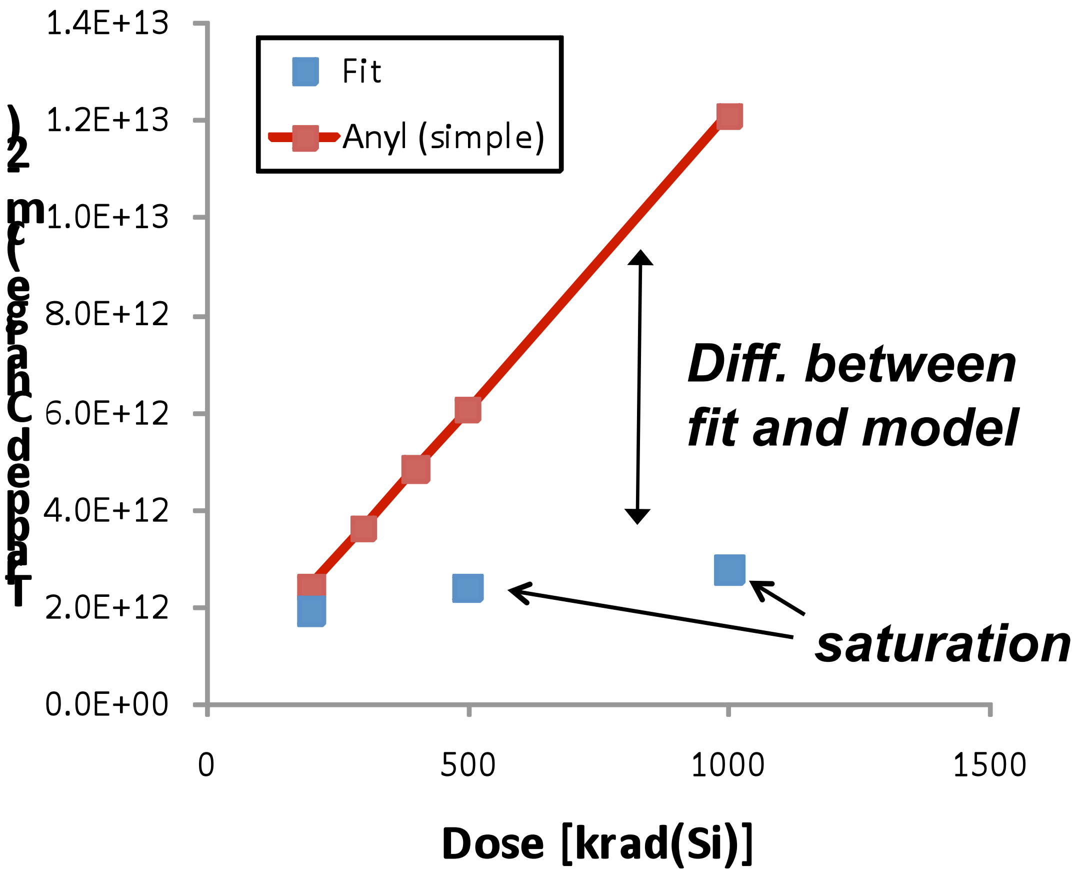
Analytical Defect Model (simplified)

Simple analytical model shows linear dependence on dose



$$\Delta N_{ot} \approx \underbrace{N_T \sigma}_{f_{ot}} \underbrace{\dot{D} \Delta t}_{D} g_o f_y t_{ox}$$

$f_{ot} = 0.45$



Diff. between fit and model

saturation

Reasons for model discrepancy

- **Simple model neglects:**
  - ○ Effect of precursor limit (saturation cannot be accurately reproduced by the model)
  - ○ Effect of trapped charge annealing (anneal rate insufficient to explain saturation)
  - ○ Effect of field inversion and electron trapping (most promising mechanism for modeling saturation)

Pre-cursor limit factor

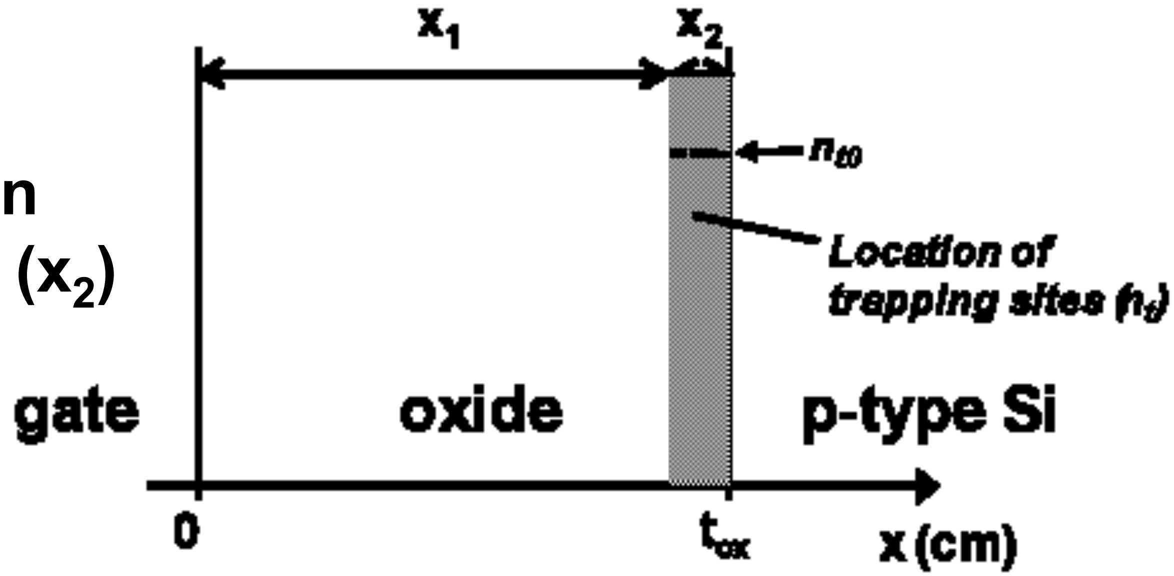
$$\frac{\partial N_{ot}}{\partial t} = \left(N_T - N_{ot}(t)\right)\sigma f_p - \frac{N_{ot}(t)}{\tau}$$

Anneal factor

basis for revised model

Revised Model Additions

- Volumetric, uniform precursor distribution (n_T) at fixed distance (x_2) from interface

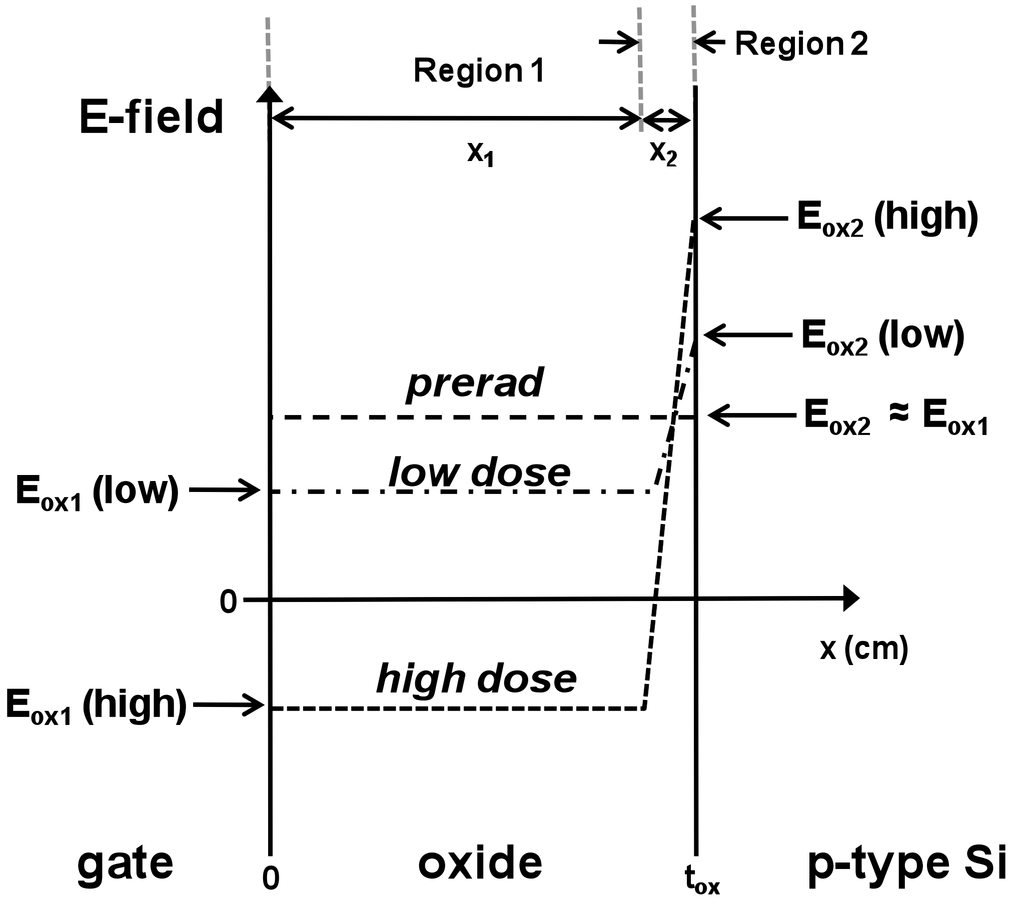


- Electron compensation term added to volumetric charge build-up model

$$\Delta n_{ot} = \dot{D}\Delta t g_0 \left(n_T \sigma_p f_{y,p} x_p - n_{ot} \sigma_n f_{y,n} x_n \right)$$

e- trapping term added

Oxide Field Inversion



- **At low TID oxide field directed toward p-Si**
- **At high TID, oxide field in reg. 1 inverts**

$$E_{ox2} = \left(V_{gb} - \varphi_{ms} - \varphi_{nt} - \psi_s\right) / t_{ox}$$

$$E_{ox2} = E_{ox1} + \frac{qn_{ot}}{\varepsilon_{ox}} x_2$$

Full Model

$$\Delta n_{ot} = \begin{cases} \dot{D}\Delta t g_0 \left(n_T \sigma_p f_y\left(E_{ox1}\right) t_{ox} - n_{ot} \sigma_n f_y\left(E_{ox3}\right) x_2\right) & E_{ox1} > 0 \\ \dot{D}\Delta t g_0 \left(n_T \sigma_p f_y\left(E_{ox3}\right) x_2 - n_{ot} \sigma_n f_y\left(E_{ox1}\right) t_{ox}\right) & E_{ox1} < 0 \end{cases}$$

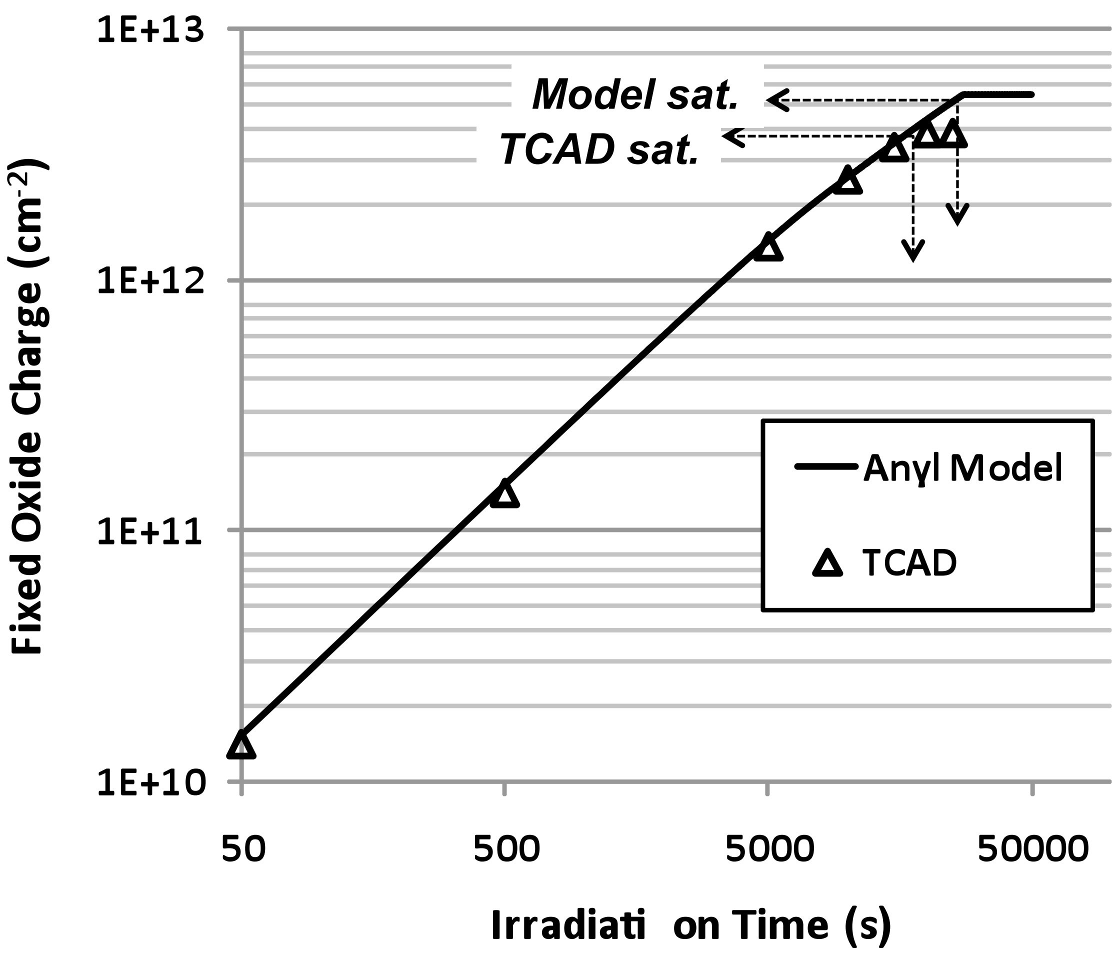
$$E_{ox3} = \frac{E_{ox1} + E_{ox1}}{2}$$

$$\Delta N_{ot} = \Delta n_{ot} \bullet x_2 \left(1 - \frac{x_2}{2t_{ox}}\right)$$

$$N_{ot}(t) = N_{ot}(t - \Delta t) + \Delta N_{ot}$$

Model computes oxide trapped charge density iteratively after specified irradiation time

Revised Analytical Model vs. TCAD

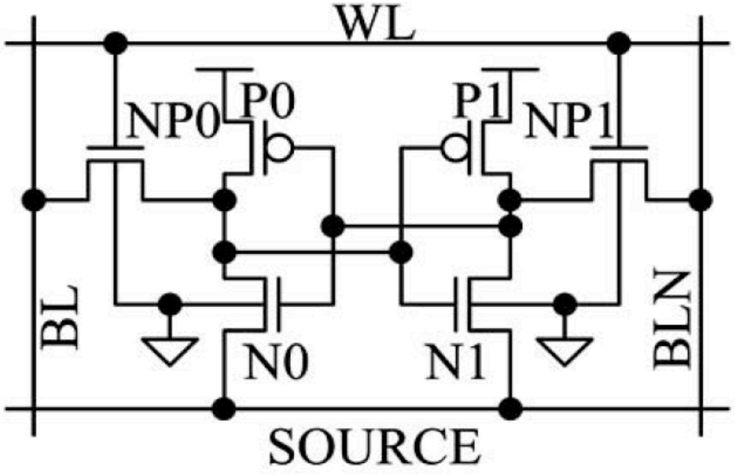


- **TCAD computes N_{ot} from REM simulator in Silvaco**
- **Model and TCAD use same parameters and function, i.e., n_T, σ_n, σ_p, and f_y**
- **Identical results except TCAD saturation occurs slightly before the model**

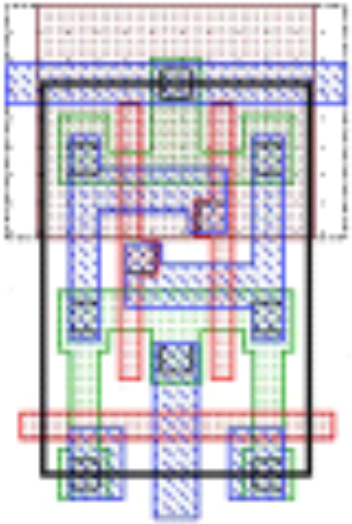
Slight discrepancy likely due to error near zero field inversion point (under investigation) … but results are very promising!

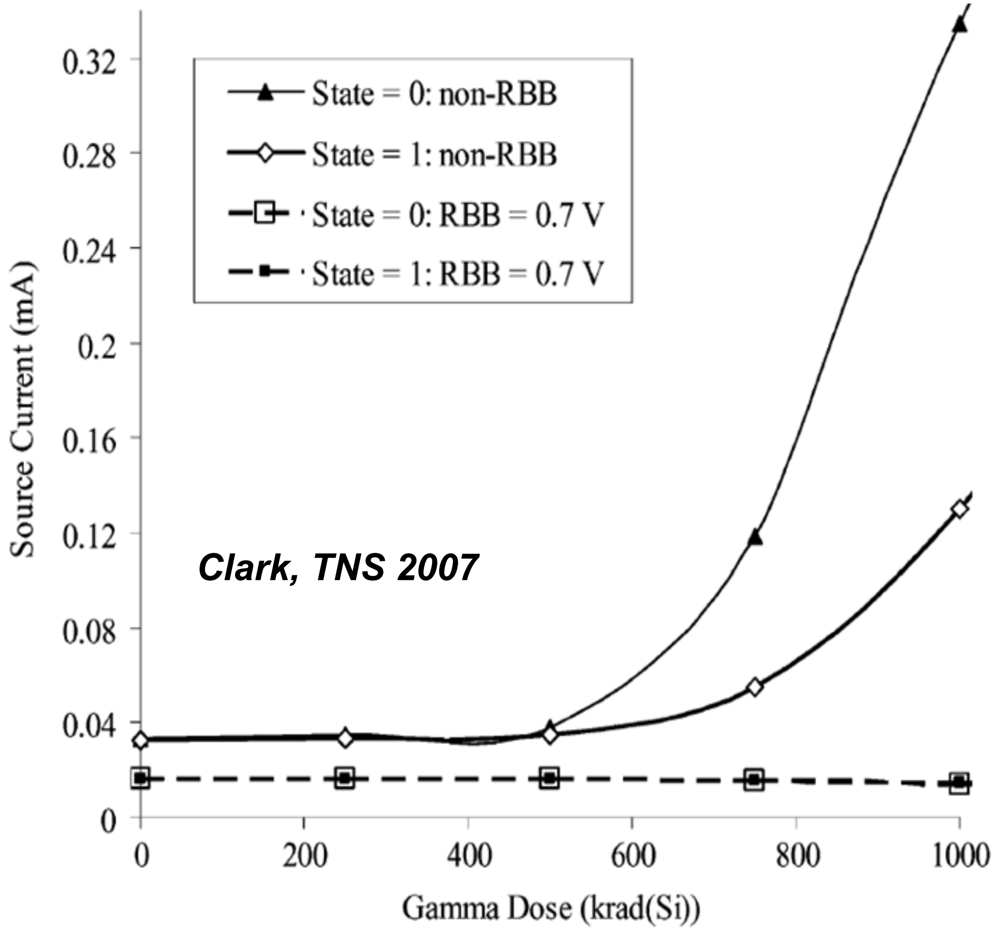
Circuit Demonstration: SRAM leakage mitigation with RBB

6T SRAM w/ nFET body control



layout



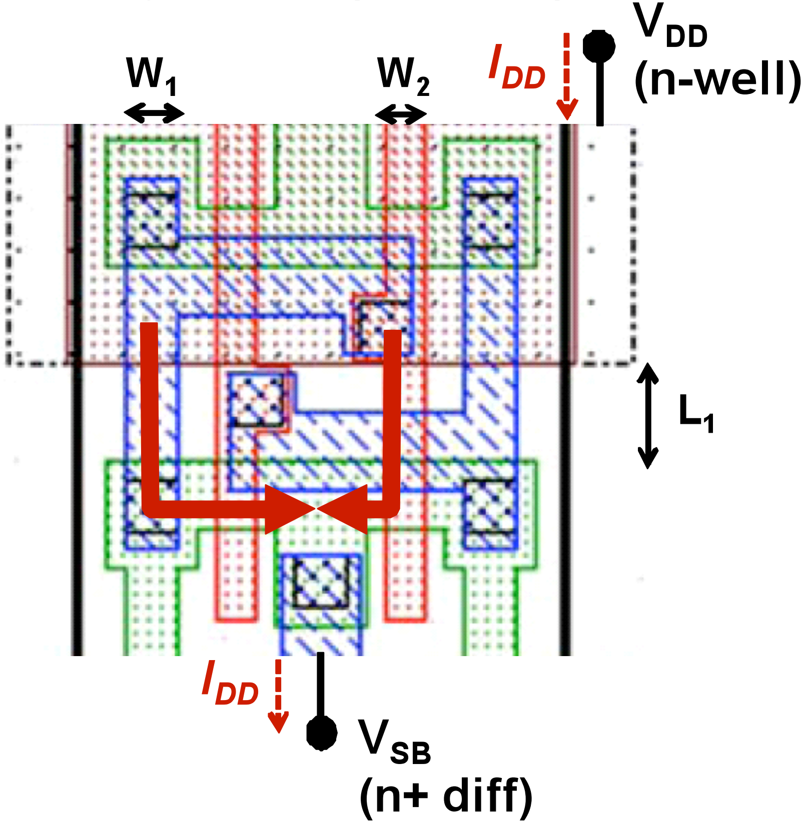


Clark, TNS 2007

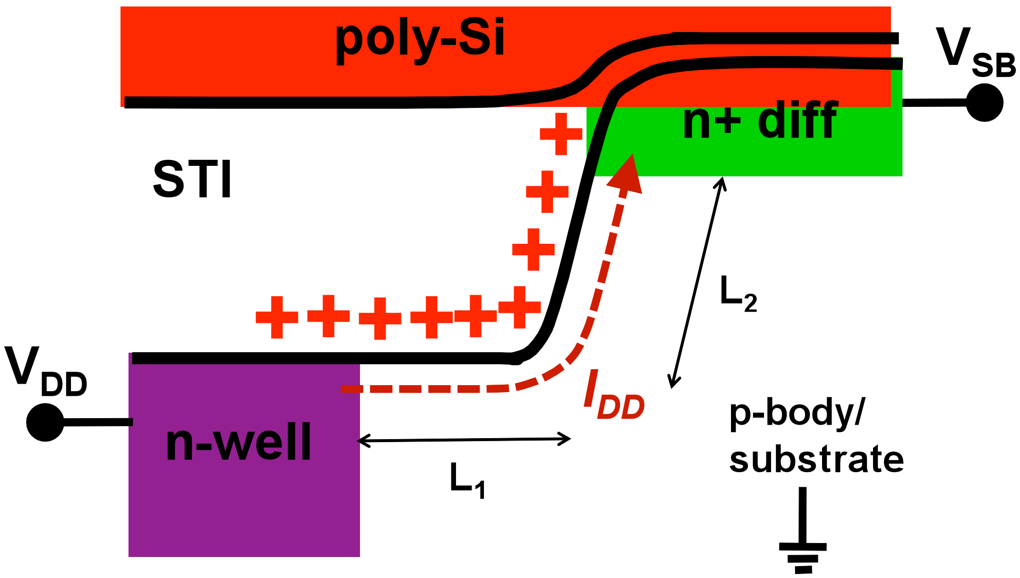
With reverse body bias (RBB), radiation-induced supply current to cell suppressed, but do we really need 0.7V RBB??

SRAM leakage mechanism: inter-device field oxide leakage

Leakage paths (top view)

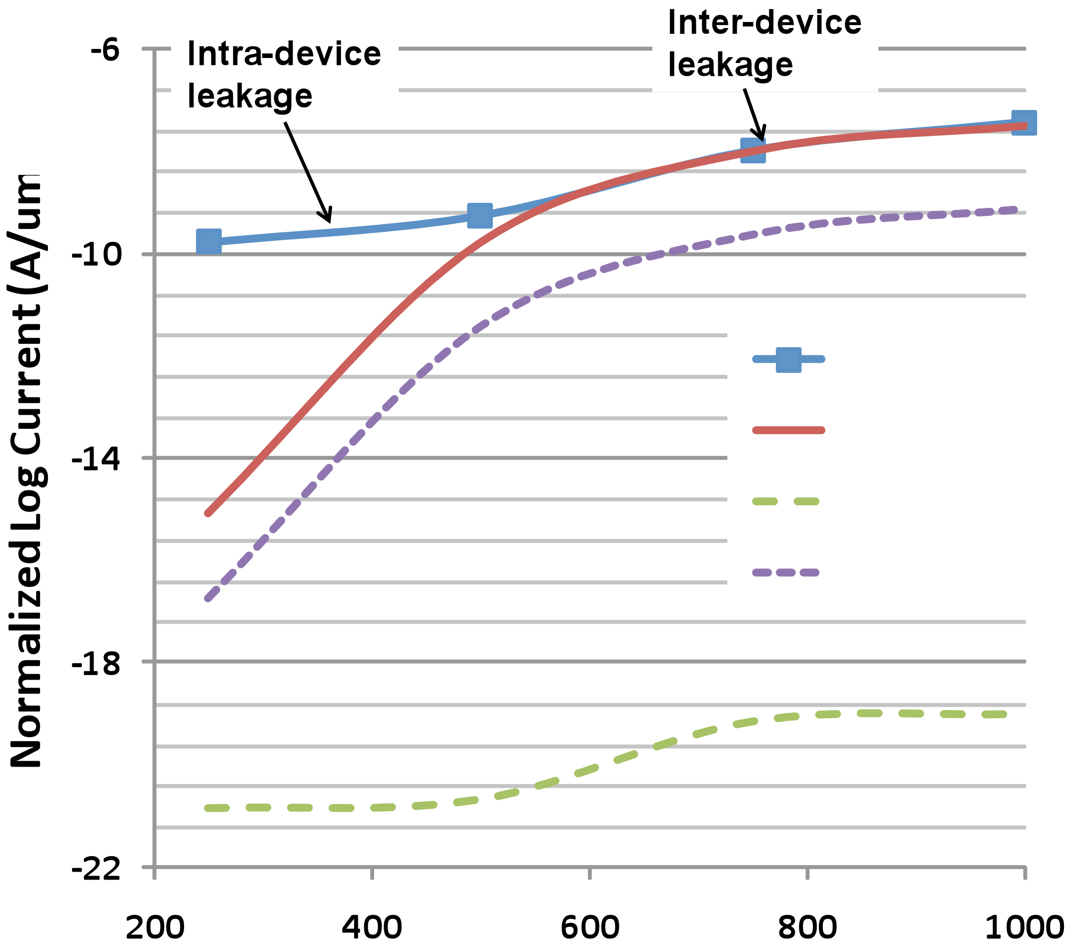


Leakage paths (x-sect)



Through analysis of SRAM response, n-well to n+ diffusion inter-device leakage identified as mechanism for increased supply current at high TID levels

TID analytical model implementation



Model enables:

- **fit to non-RBB high dose response when $V_{SB} = 0V$**
- **identification of V_{SB} sufficient to suppress field oxide leakage**

Use of model supports optimization of RHBD designs … important when considering tradeoff between RBB and SEEs!

Summary: Analytical Model

- **Discrepancies between saturated defect densities extracted from data and those calculated using simple trapping model suggest need for model revisions**

- **While charge annealing and precursor limits can cause saturation, the inclusion of field inversion with electron compensation models most effective in reproducing data**

- **Revised approach can be implemented easily as a compact model to enable estimates of circuit response to TID and support design optimization**

Recent Work (2009)

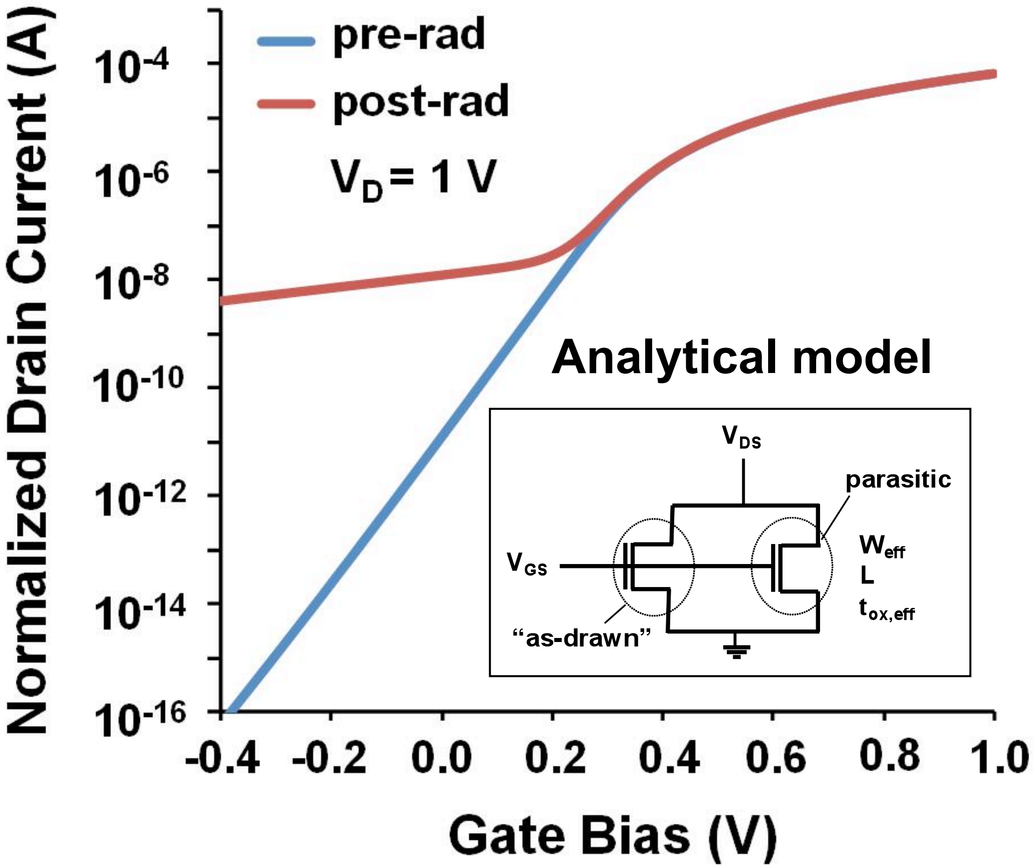
- Demonstration of analytical model of TID effects on bulk CMOS isolations oxides
  - Revised analytical model for TID defect buildup compared to FOXFET I-V and TCAD simulations
  - Demonstration of modeling approach: SRAM with reverse body bias
- **Effects of Channel Implant Variation on Edge Leakage Currents**
- Modeling TID effects in Multiple Gate FETs

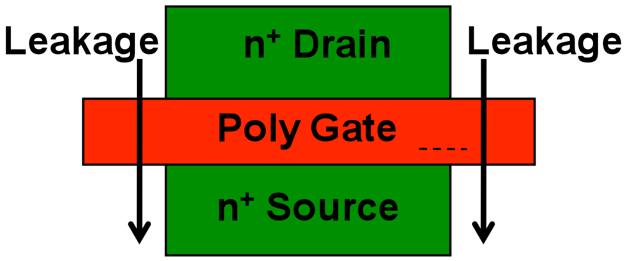
Motivation of Study

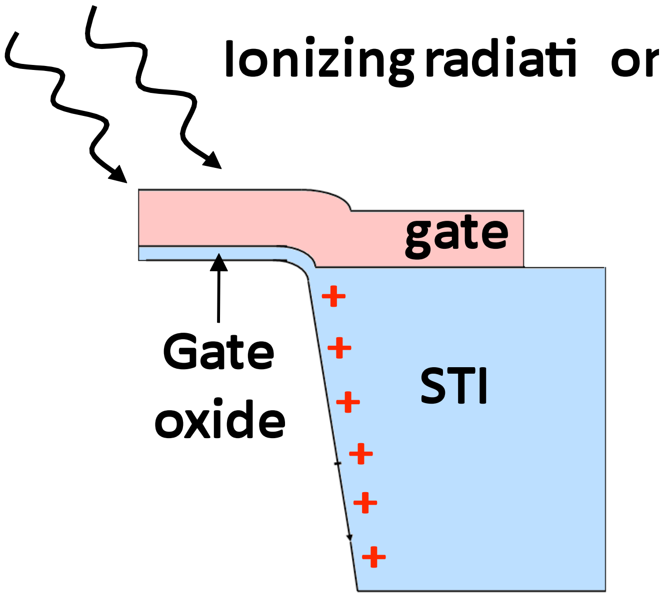
- **To model the effects of statistical variation in the dose and energy of MOSFET channel implants on radiation-induced edge parasitics**
- **90 nm commercial bulk CMOS technology**

Results show a slight variability in channel implant parameters can have a significant impact on doping levels and thus edge leakage currents

Radiation-induced edge leakage

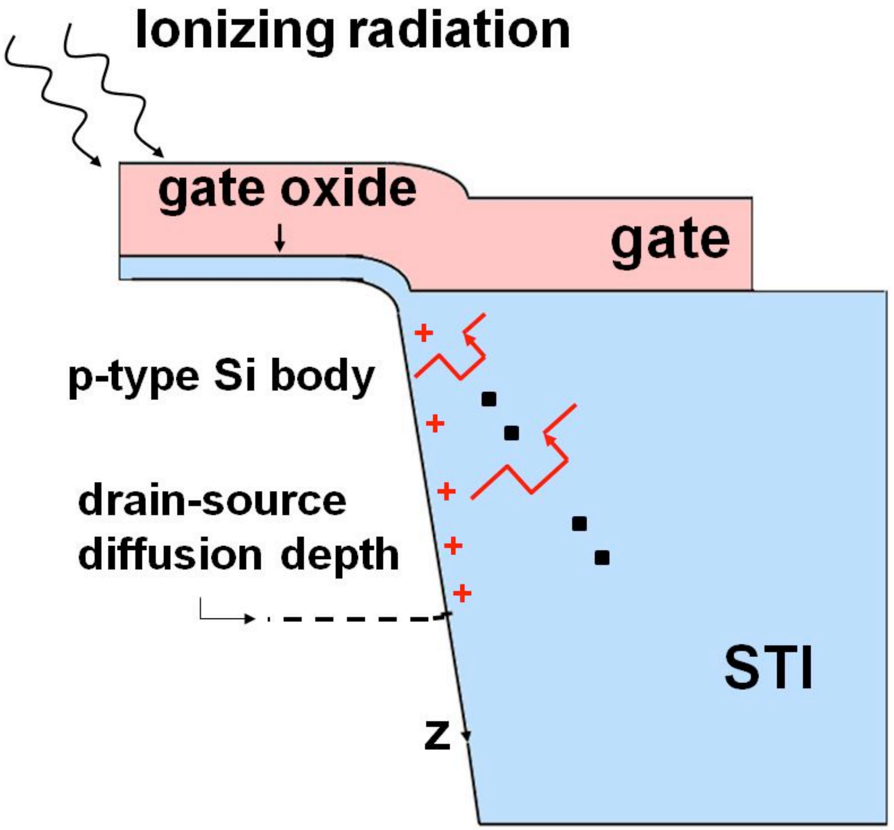


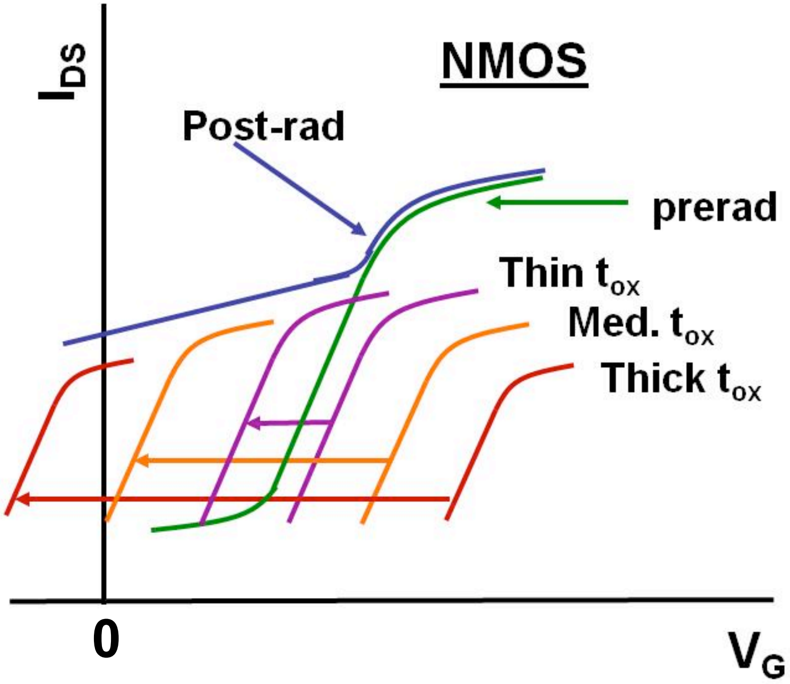




Charge buildup (N_{ot}) in the STI inverts the sidewall and induces a parasitic leakage path along the edges of the "as-drawn" transistor

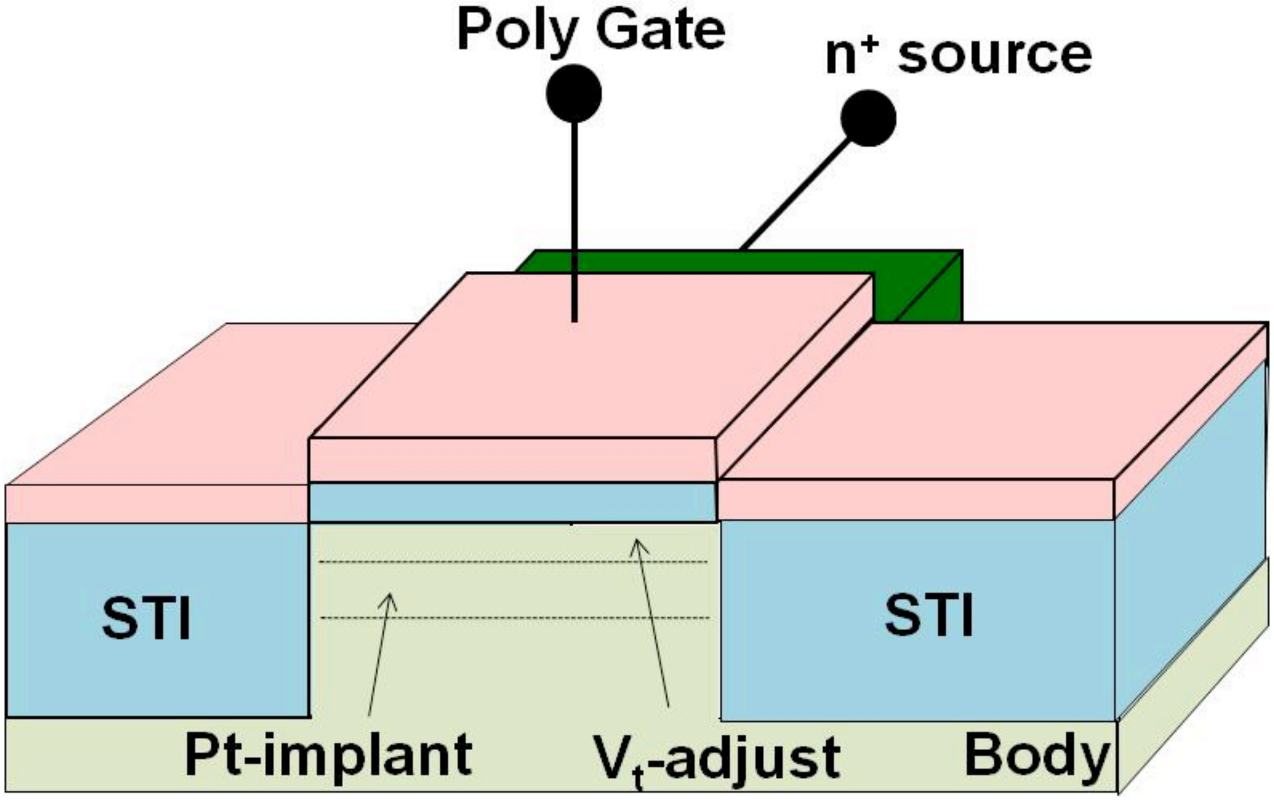
Parasitic Edge Devices





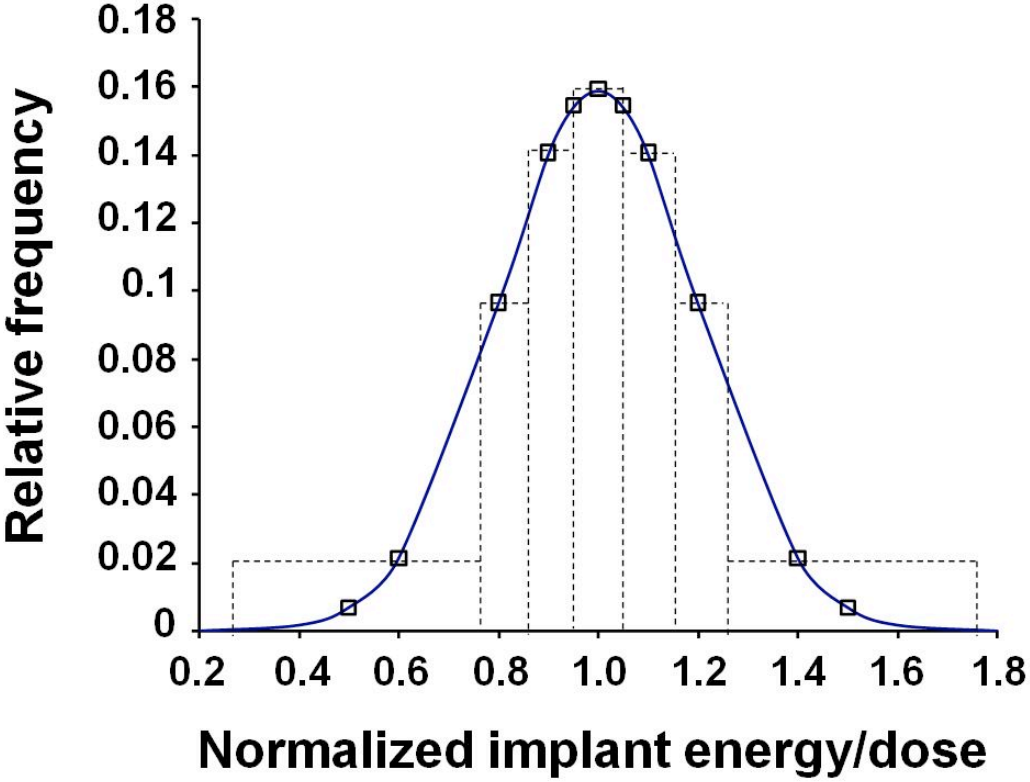
Increased exposure to TID leads to formation of parasitic edge devices (with varying t_{ox}) operating in parallel with "as-drawn" FET

MOSFET Channel Implants



Doping along sidewall is determined by dose and energy of punchthrough (Pt), threshold-adjust (V_t-adjust), and sidewall implants

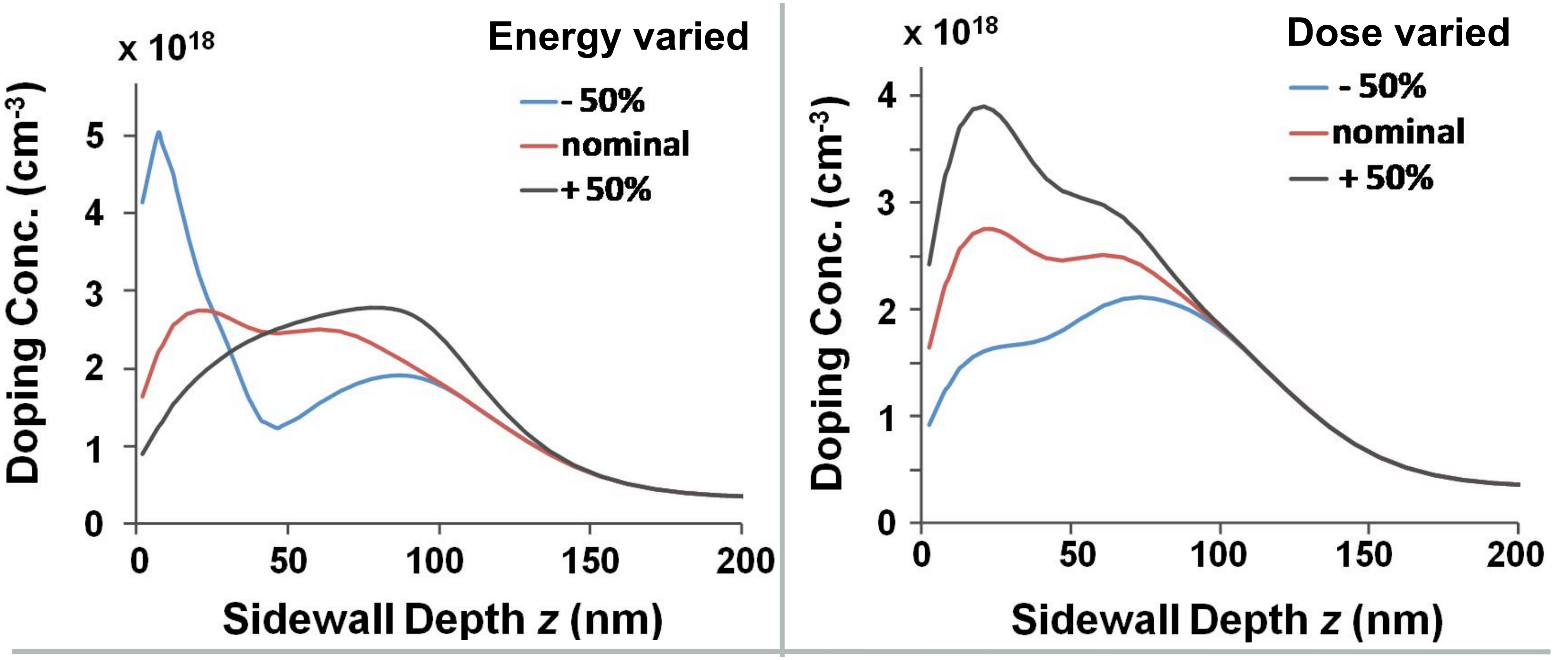
Channel Implant Variation



- **Statistical variations in dose and energy of channel implants alter doping along STI sidewall**
- **Doping profiles obtained using process simulator**
- **Nominal values for dose and energy are 1.25×10^{13} cm^{-2} and 4 keV (V_t implant)**

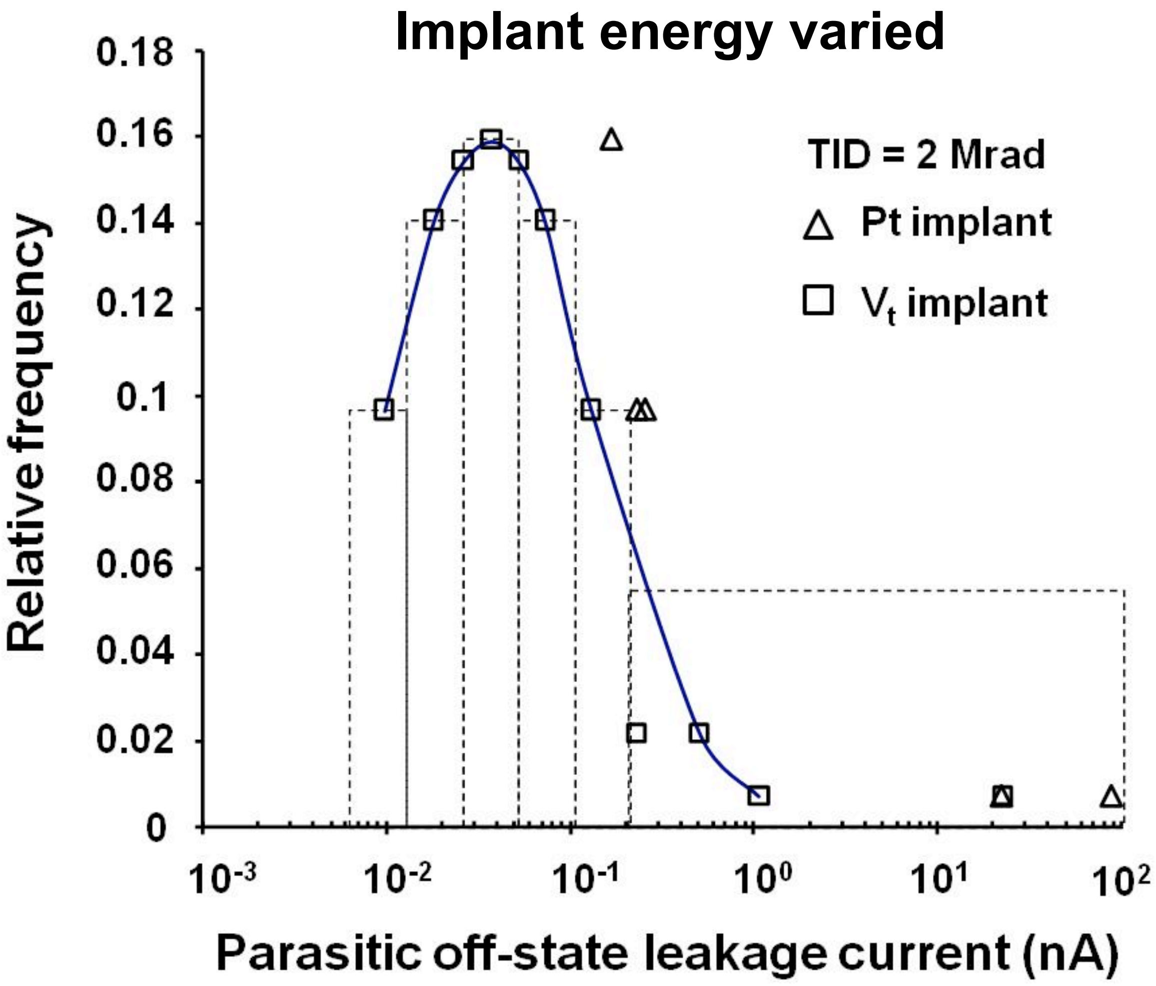
Bernstein et al., found a normal distribution in the threshold voltage when testing N number of devices (IBM J. RES. & DEV., 2006)

Impact on Doping Profile



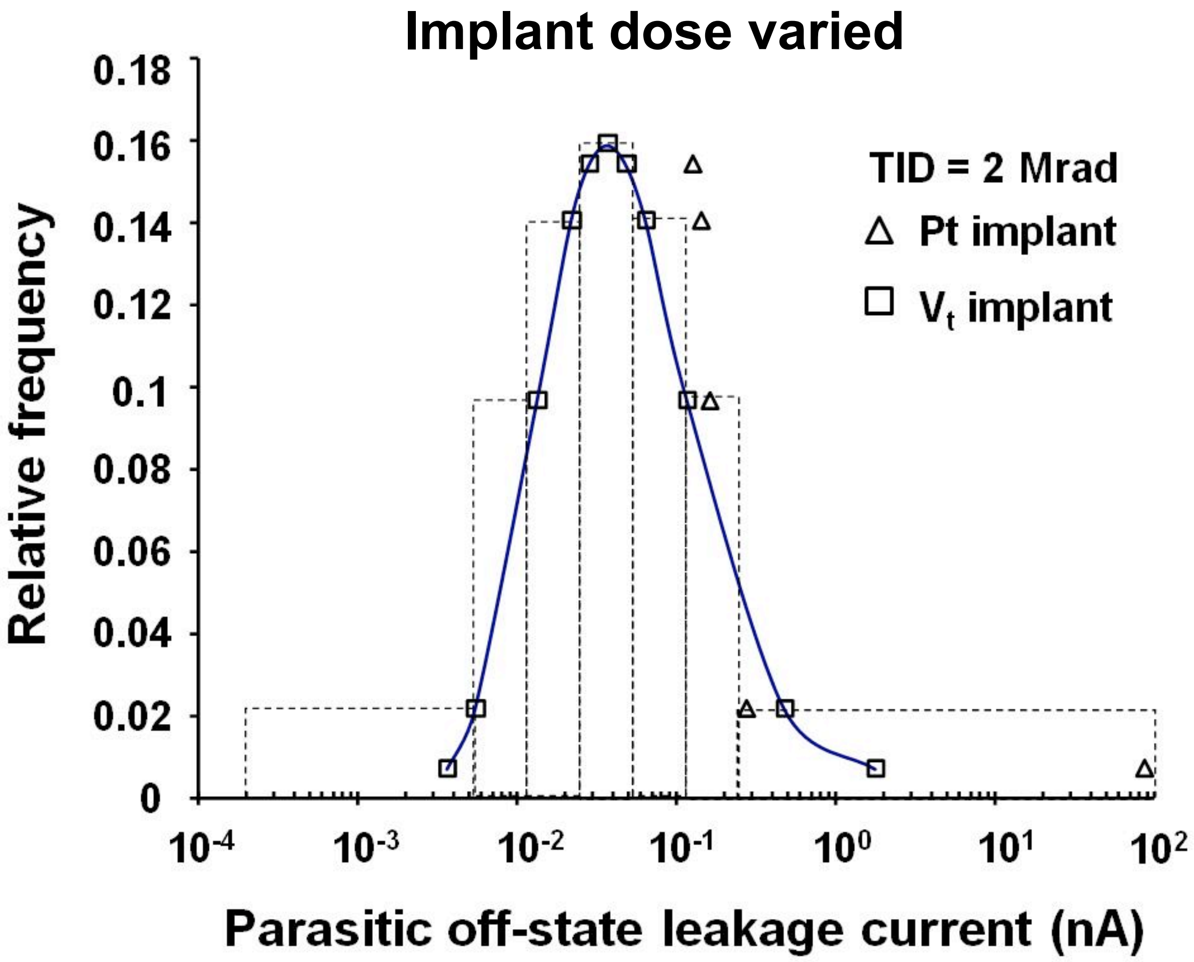
Effect of statistical variations in dose and energy of the V_t-adjust implant on doping profiles along STI sidewall

Off-state Leakage Current



- **Off-state leakage is I_D @ $V_G = 0$ V**
- **Distribution in rad-induced edge leakage currents for variations in the energy of the V_t-adjust and Pt implants**

Off-state Leakage Current



- **Off-state leakage is I_D @ V_G = 0 V**
- **Lognormal distribution in rad-induced leakage currents for variations in the implant dose of the V_t and Pt implants**

Summary: Implant Variation Effects

- **Statistical variations in dose and energy of MOSFET channel implants impact doping along STI sidewall and thus amount of edge leakage current**
- **Results demonstrate large spread in leakage currents from a fairly tight normal distribution in process parameters**

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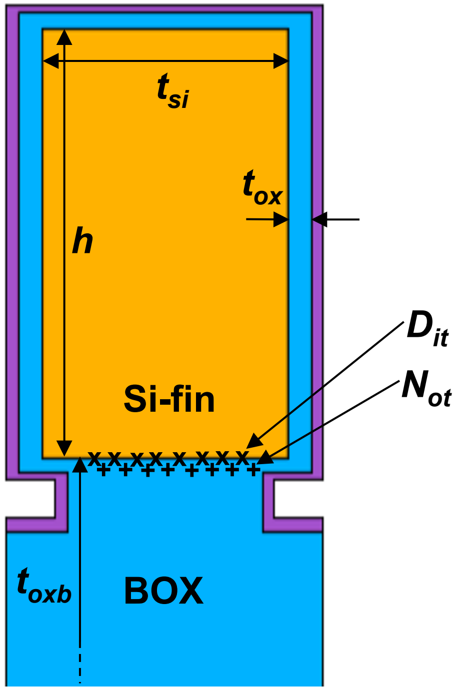
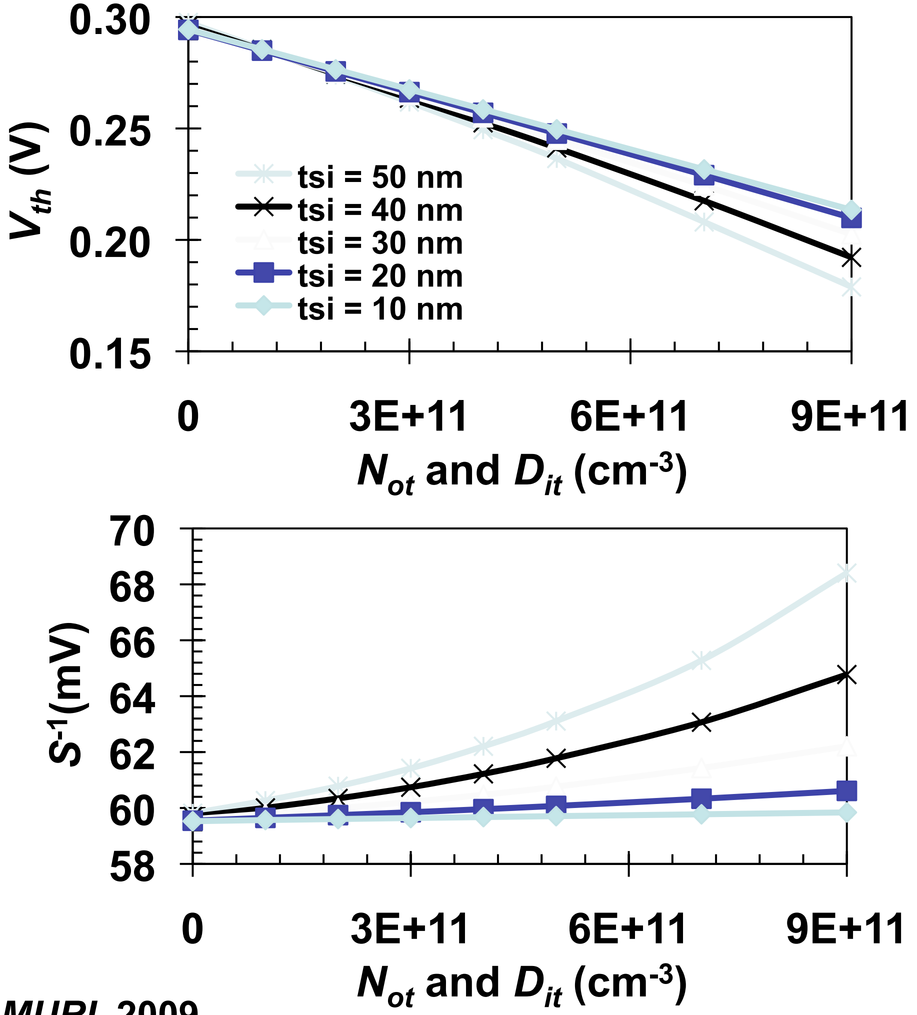
TID effects in MuGFET SOI devices



Devices with narrower fins exhibit less degradation with TID as observed by ΔV_{th} and ΔS^{-1} as a function of N_{ot} and D_{it}

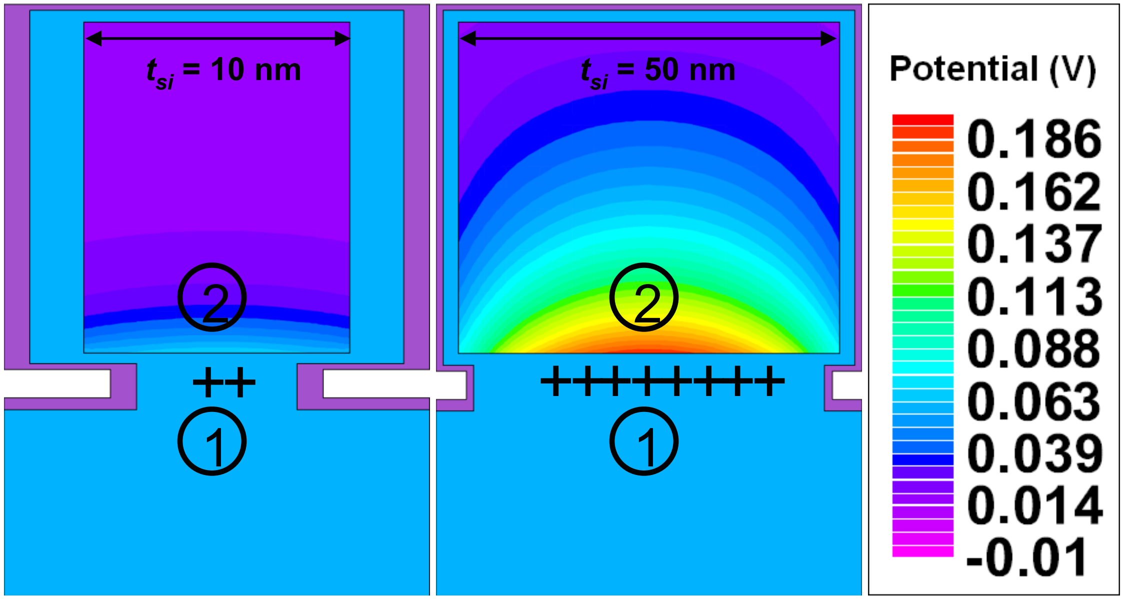
Simulation results



Why narrow fins are harder

1. Electric field near fin-BOX interface of device with narrow fins is reduced by influence of the lateral gates. This reduces the charge yield

2. Devices with narrow fins have an improved control over the electrostatic potential inside the fin due to the lateral gates



MuGFET TID Model

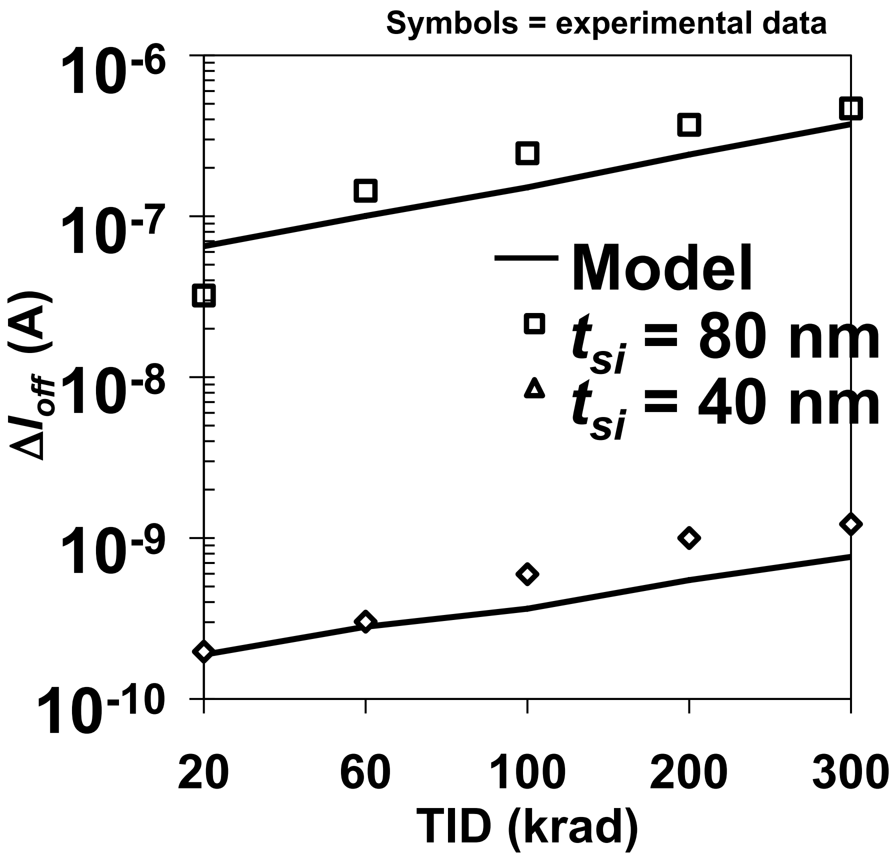
- I_d-V_{gs} degradation modeled analytically to predict ΔI_{off} as function of TID and t_{si}.

- Radiation-induced degradation parameters enter model through defect potential ϕ_{nt} which is a function of t_{si}.

$$\phi_{nt}(t_{si}) = \phi_{nt0}[1 - \mathrm{DG}(t_{si})]$$

$$\phi_{nt0} = \frac{q}{C_{oxf}}\left[N_{ot} - D_{it}\left(\psi_b - \phi_f\right)\right]$$

- Parameters extracted to describe $\mathrm{DG}(t_{si})$ making the analytical model adaptable to different technologies.



Summary: TID effects in MugFETs

- **Modeling results support data (El-Mamouni)**
- **Thinner fins in MugFETs lead to less defect buildup in BOX and increased charge masking from lateral gates (i.e. thinner fins = harder parts)**
- **Surface potential based model can accurately reproduce experimental date**