Modeling Total Ionizing Dose Effects in Deep Submicron Bulk CMOS Technologies

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Acknowledgements

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Motivation

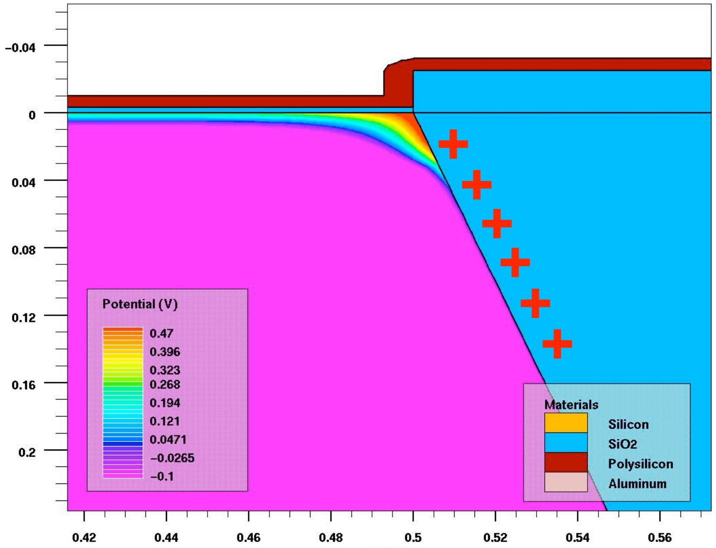
- Characterize and model radiation damage effects in modern CMOS device technologies
- Technologies:
  - deep submicron bulk CMOS,
  - silicon on insulator (El-Mamouni)

Previous Research

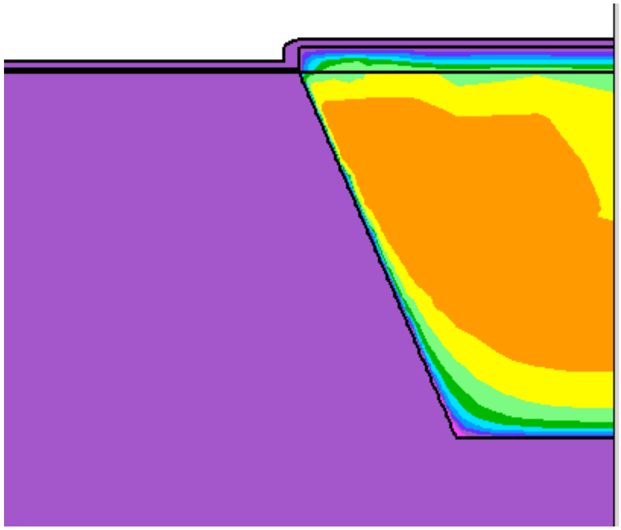
- May 2005 - “Device-level Radiation Effects Modeling”

  Overview of numerical (TCAD) simulation approaches to modeling radiation effects in CMOS devices

Sheet Charge



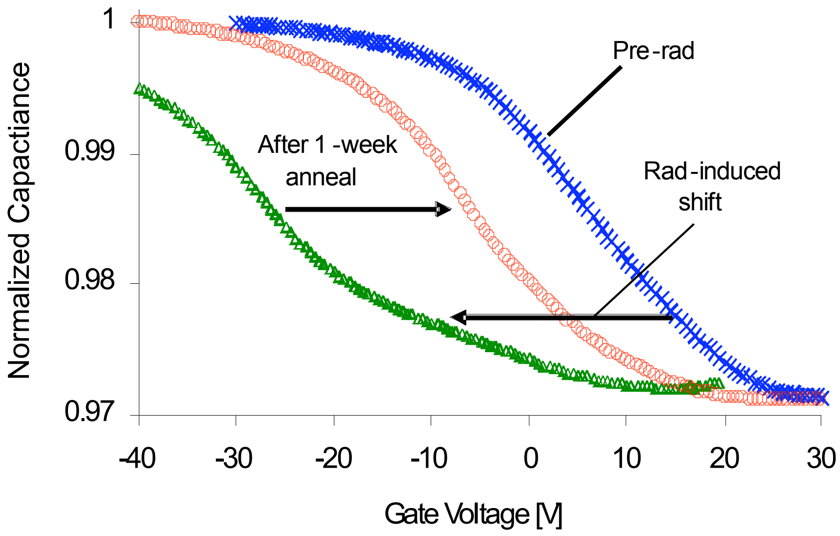
Trapped Charge vol. distribution

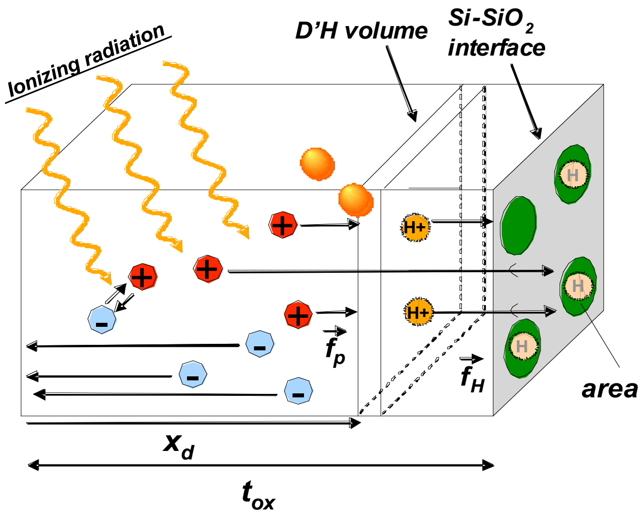


Previous Research

- June 2006 - “Total Ionizing Dose Effects in Bulk Technologies and Devices”

  Characterize, parameterize TID effects. Formalize closed form analytical expressions for TID effects in devices (130nm CMOS).





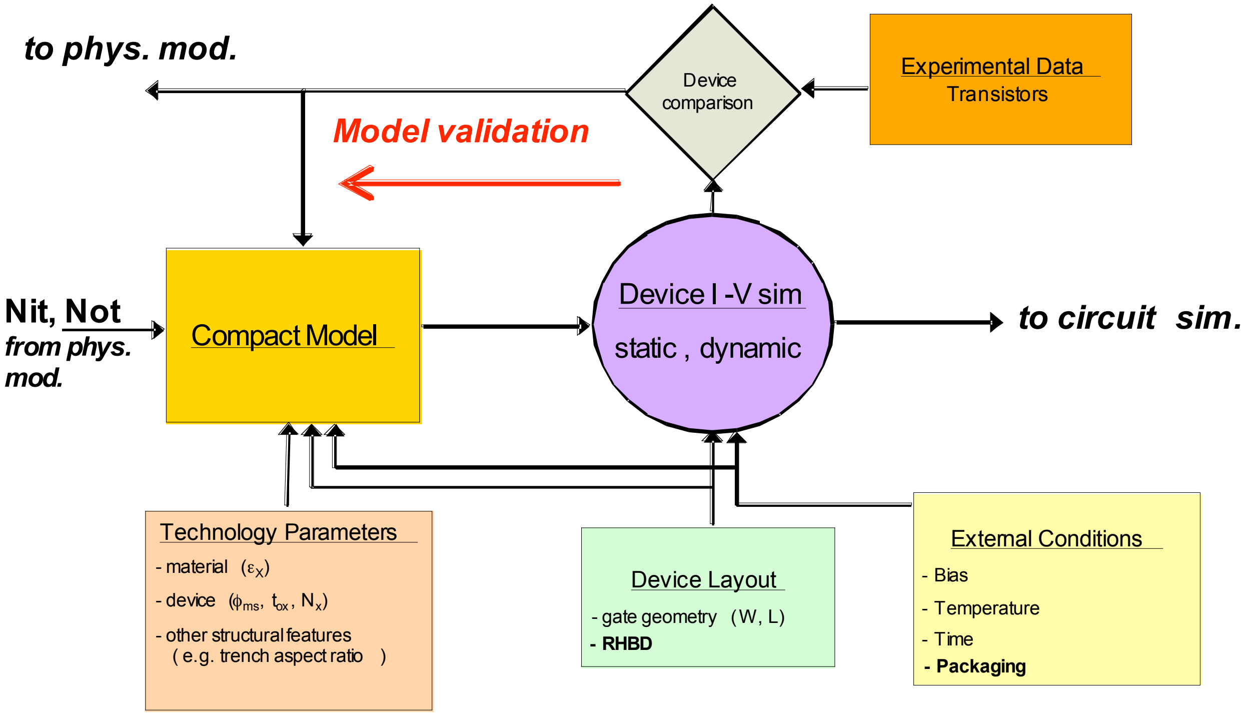
$$\ddot{A}N_{ot} \approx Dk_g f_y(\vec{\tilde{a}}) f_{ot}(\vec{\tilde{a}}) t_{ox}$$

$$\ddot{A}N_{it} \approx Dk_g f_y(\vec{\tilde{a}}) f_{DH} f_{it} t_{ox}$$

Previous Research

- June 2007 - “Modeling Total Ionizing Dose Effects in Deep Submicron Bulk CMOS technologies”

Description and initial validation of radiation-enabled compact modeling approach for CMOS technologies (≥ 90nm CMOS).



to phys. mod.

Device comparison

Experimental Data
Transistors

Model validation

Nit, Not
from phys. mod.

Compact Model

Device I -V sim
static , dynamic

to circuit sim.

Technology Parameters
- material (ε_X)
- device (ϕ_{ms}, t_{ox}, N_x)
- other structural features
  (e.g. trench aspect ratio)

Device Layout
- gate geometry (W, L)
- **RHBD**

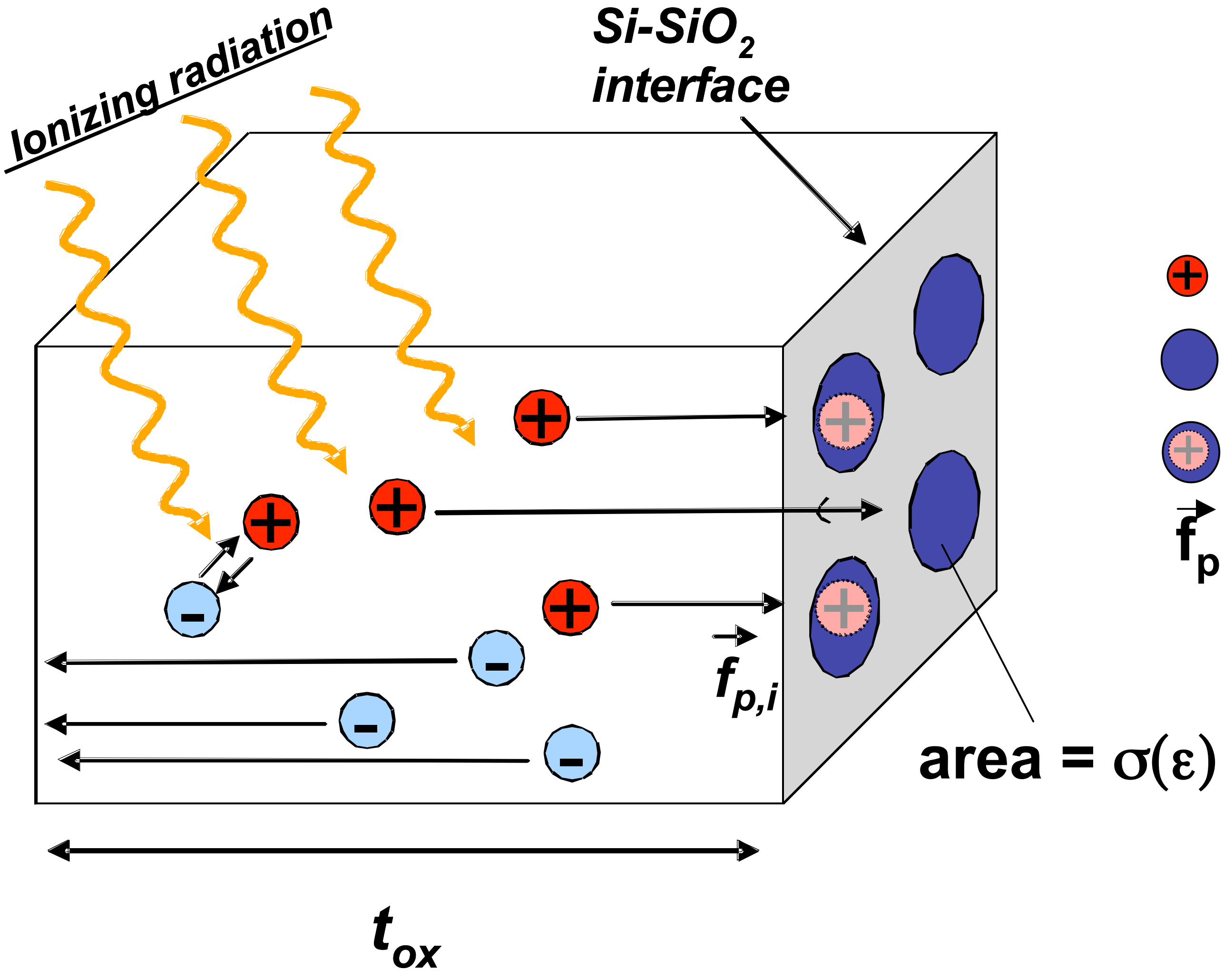
External Conditions
- Bias
- Temperature
- Time
- **Packaging**

Recent Work (2008)

- **Full analytical model of TID effects on bulk CMOS isolations oxides**
  - **Analytical model for TID defect buildup**
  - **Effects on sidewall surface potential**
  - **Radiation-induced edge leakage model and validation**
- **New data and analysis of effects on 90 nm field oxides and multi-fingered transistors (additional material)**

Ionization Damage in Silicon Dioxide

Hole trapping process



Ionizing radiation

Si-SiO$_2$ interface

$\vec{f}_{p,i}$

area = $\sigma(\varepsilon)$

t_{ox}

⊕ - *surviving hole (p)*

● - *hole trap (N$_T$)*

⊕ - *trappped hole (N$_{OT}$)*

$\vec{f}_p$ - *hole flux*

Oxide trapped charge formation

$$\frac{\partial f_p}{\partial x} = -\frac{\partial p}{\partial t} + \dot{D} g_o f_y - R_p$$

$$\approx \dot{D} g_o f_y$$

(steady state)

$$\Rightarrow \quad f_{p,i} \approx \dot{D} g_o f_y t_{ox}$$

($f_p > 0$ for all x)

$$\frac{\partial N_{ot}}{\partial t} = \left(N_T - N_{ot}(t)\right)\sigma f_p - \frac{N_{ot}(t)}{\tau}$$

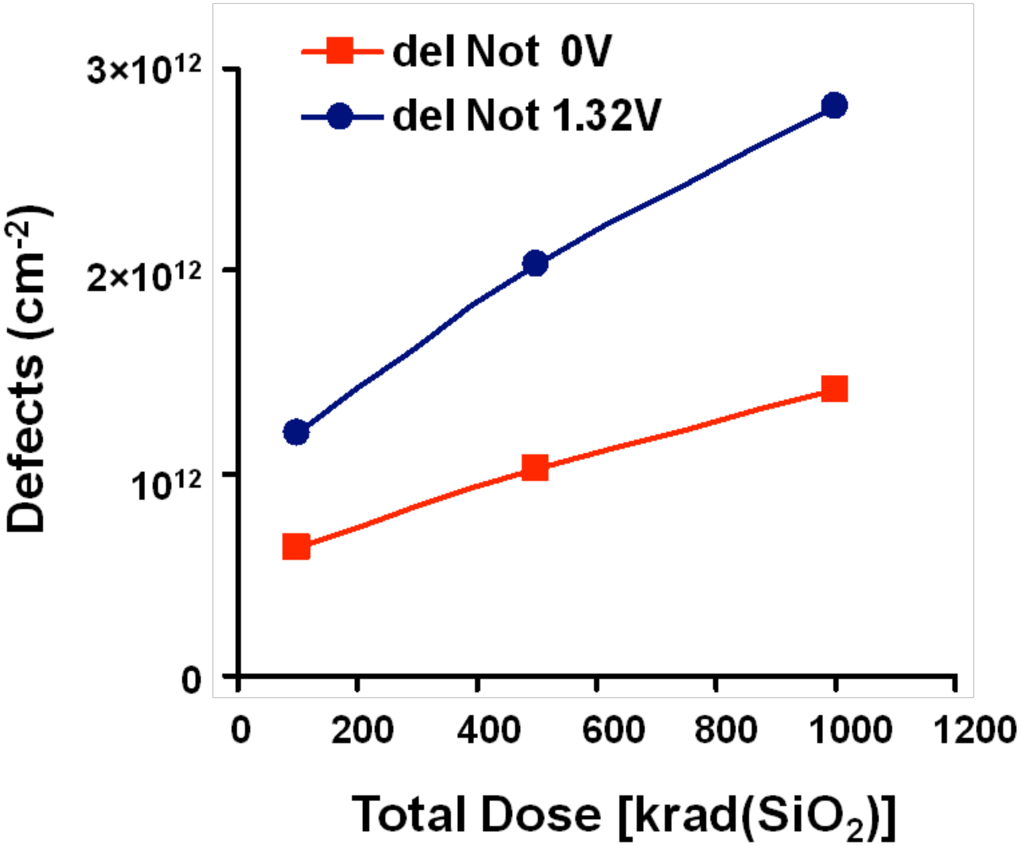
$$\approx N_T \sigma f_{p,i}$$

$$\Rightarrow \quad \Delta N_{ot} \approx \underbrace{N_T \sigma}_{f_{ot}} \underbrace{\dot{D} \Delta t}_{D} g_o f_y t_{ox}$$

(Assume no saturation or annealing and sheet densities at interface)

(After Rashkeev et al. TNS 2002)

Defect buildup: N_{ot}



130 nm data

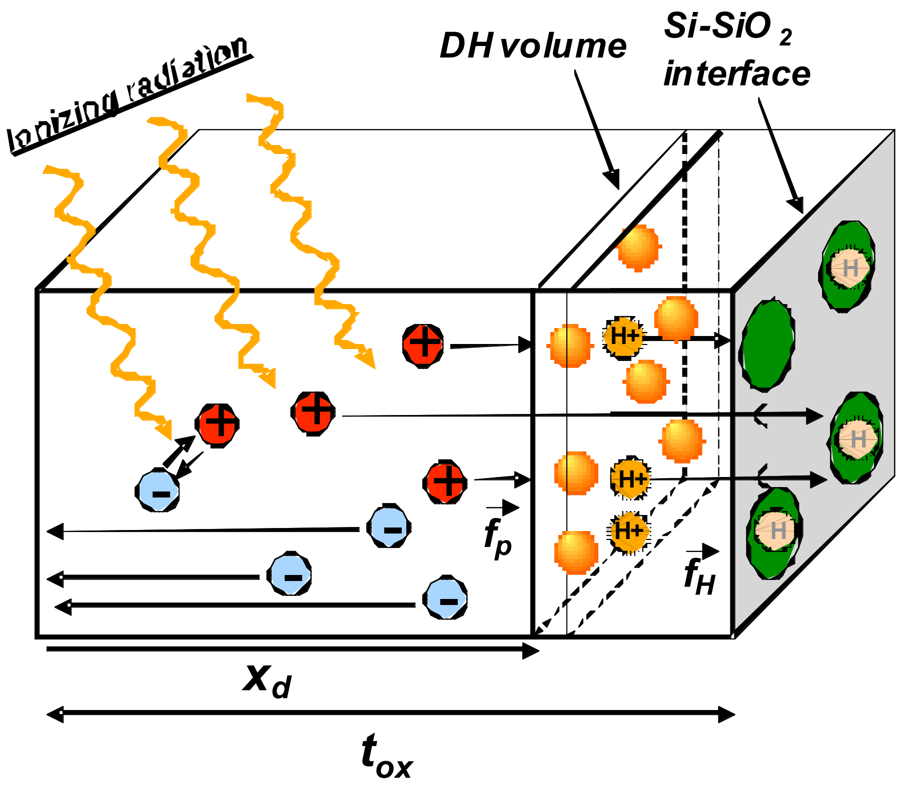
Defect buildup is:

1. **Greater for higher oxide fields (consistent w/ f_y)**
2. **Linear with dose (no saturation … yet)**

Data obtained from measurements on STI field oxide capacitors

Interface trap formation

Two Stage Hydrogen model



● - hydrogen defect (D'H)

● - protons

● - Si-H (N_{SiH})

● - dangling bond (N_{it})

f_H - proton flux

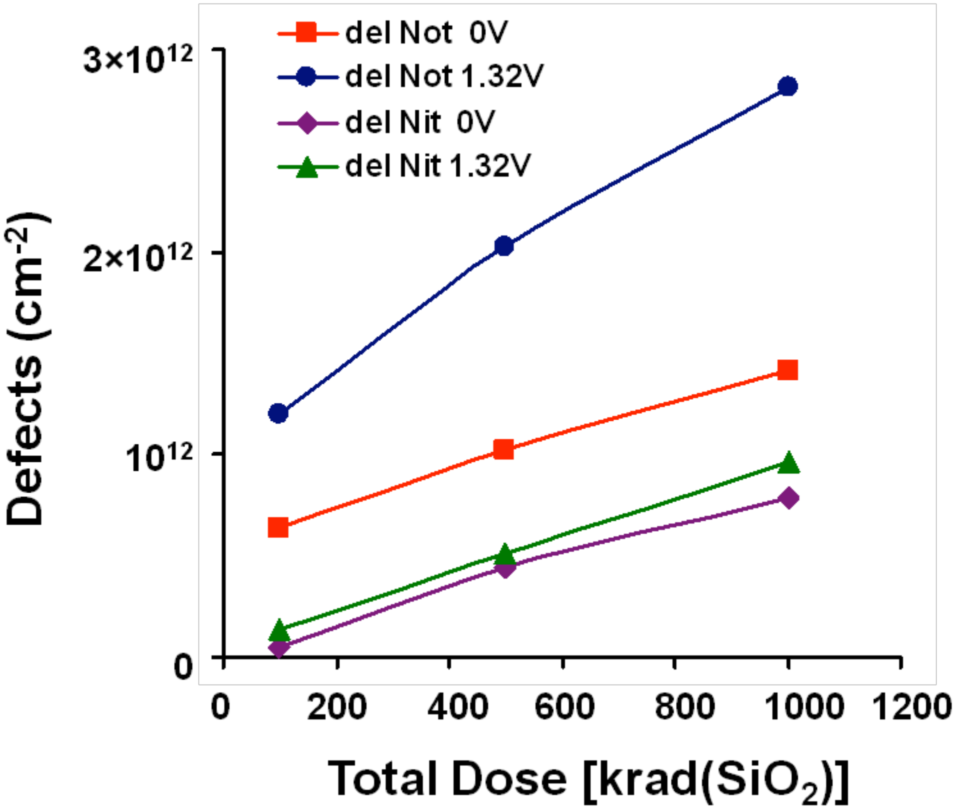
$$SiH + H^+ \Rightarrow Si^+ + H_2$$

$$\frac{\partial N_{H^+}}{\partial t} = N_{DH}\sigma_{DH} f_p - \frac{\partial f_{H^+}}{\partial x}$$

$$\frac{\partial N_{it}(t)}{\partial t} = \sigma_{gen} N_{SiH} f_{H^+} - \sigma_{pass} N_{it}(t) f_{H_2}$$

(After Rashkeev et al. TNS 2002)

Defect buildup: N_{it}



<u>**130 nm data**</u>

N_{it} defect buildup is:

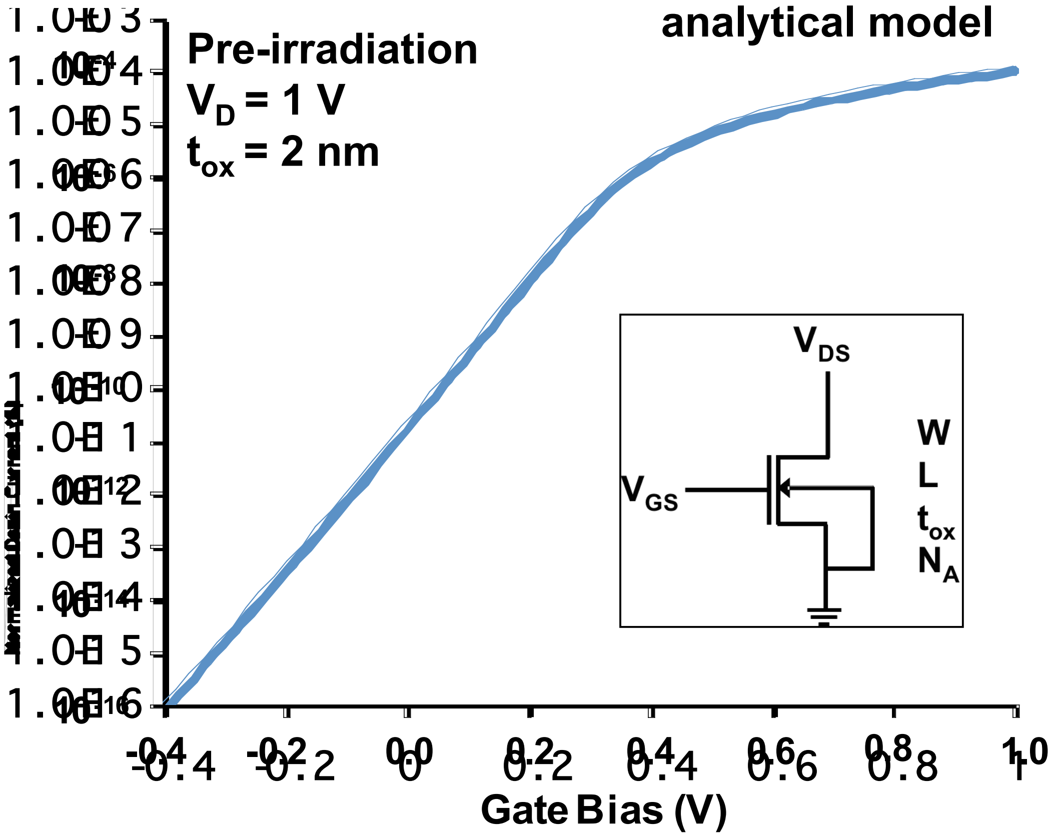
1. **Greater for higher oxide fields (consistent w/ f_y)**
2. **Linear with dose (no saturation … yet)**
3. **Less than N_{ot} buildup**

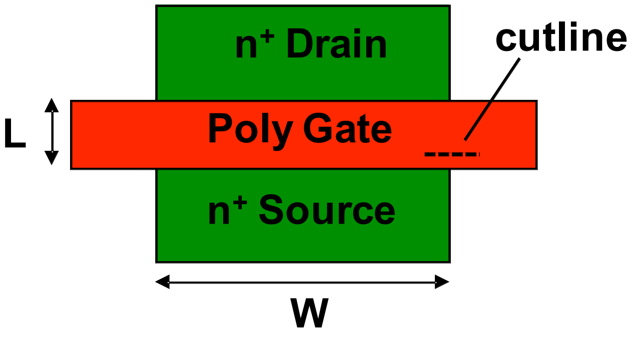
Data obtained from measurements on STI field oxide capacitors

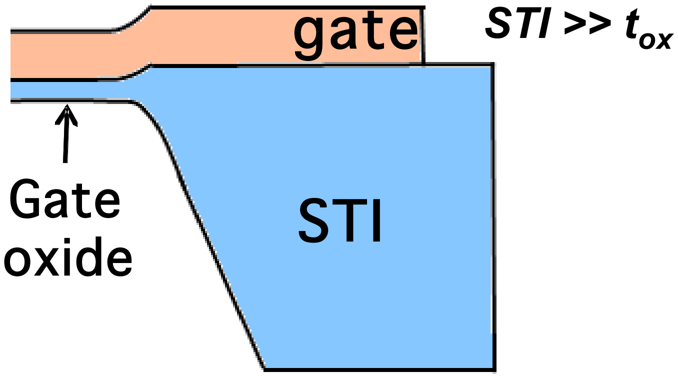
Modeling Radiation Effects on Devices

Pre-irradiation behavior

Surface potential based analytical model

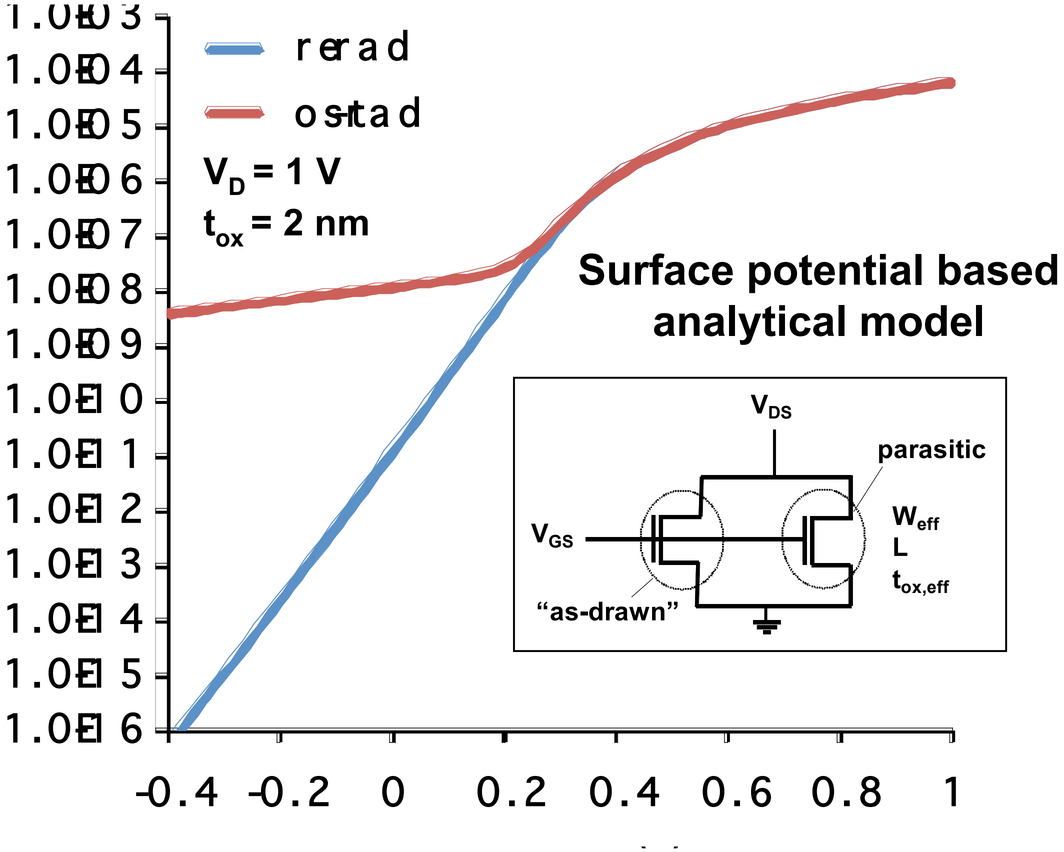




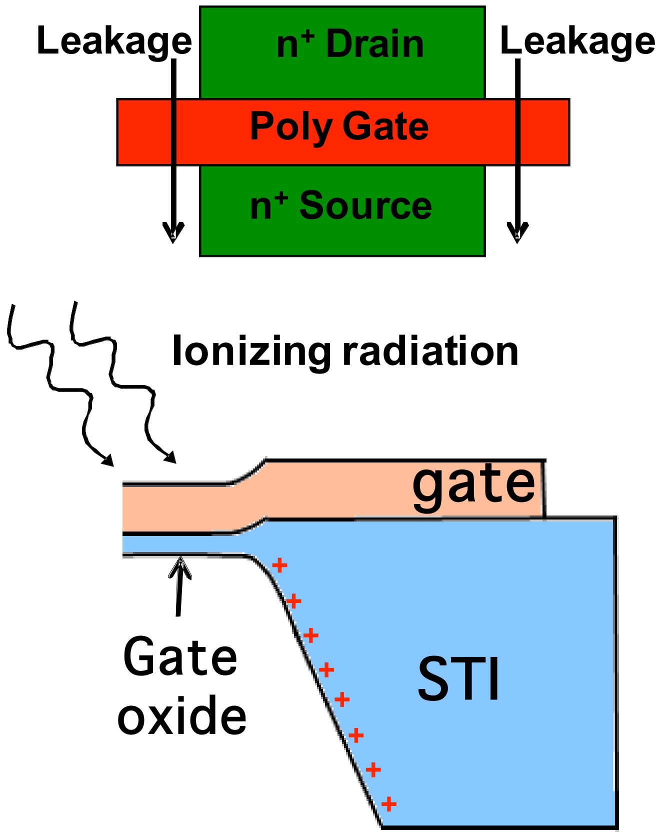


Potential applied to the gate controls the flow of carries (electrons) from source to drain in the channel

Radiation-induced leakage

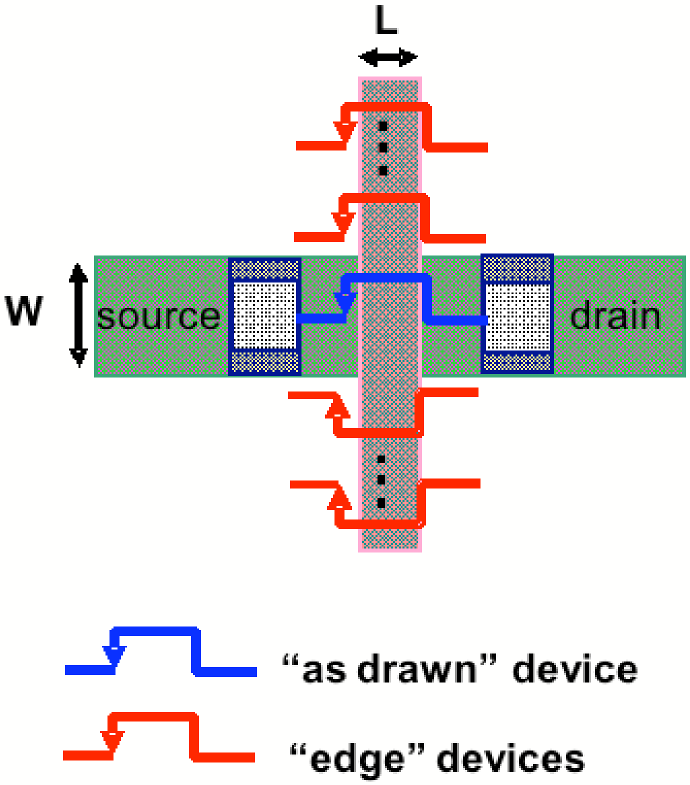


Surface potential based analytical model

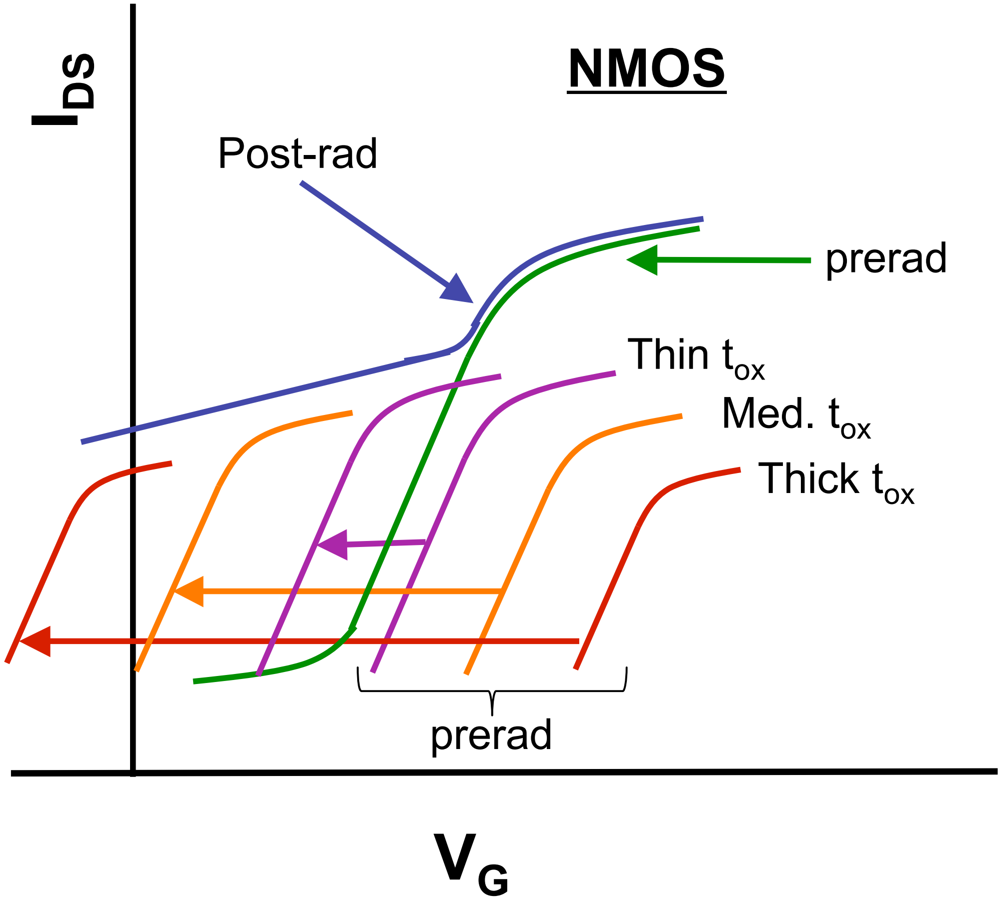


Charge buildup (N_{ot}) in the STI inverts the sidewall and induces a parasitic leakage path along the edges of the “as-drawn” transistor

Parasitic leakage model

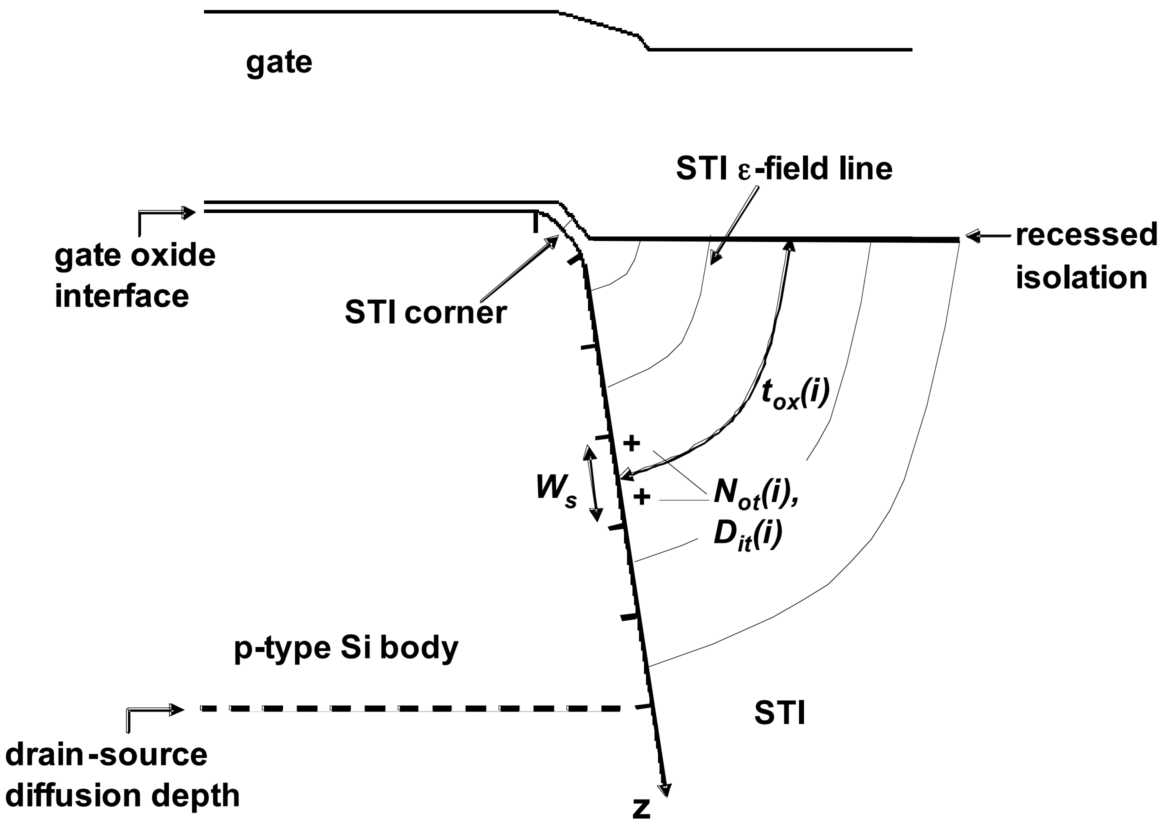


Edge parameters
$W(z)$, $t_{ox}(z)$, $N_A(z)$
$N_{ot}(z)$, $D_{it}(z)$



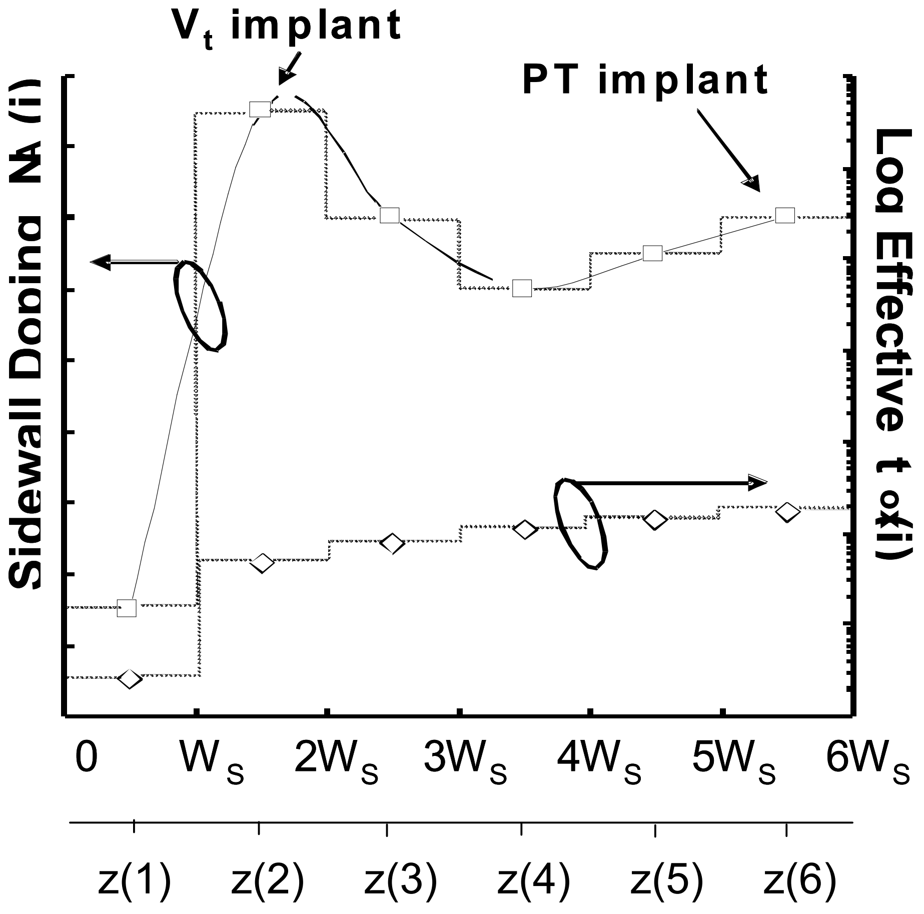
Parasitic "edge" device modeled as several thin, medium, and thick nFETs operating in parallel with "as drawn" FET

Parasitic device description



- "Edge" devices represent distinct subdivisions of conducting sidewall
- The number (n) of "edge" devices balance need for simulation accuracy with computational efficiency
- Defect generation and effects of defects on *surface potential* modeled analytically for each device

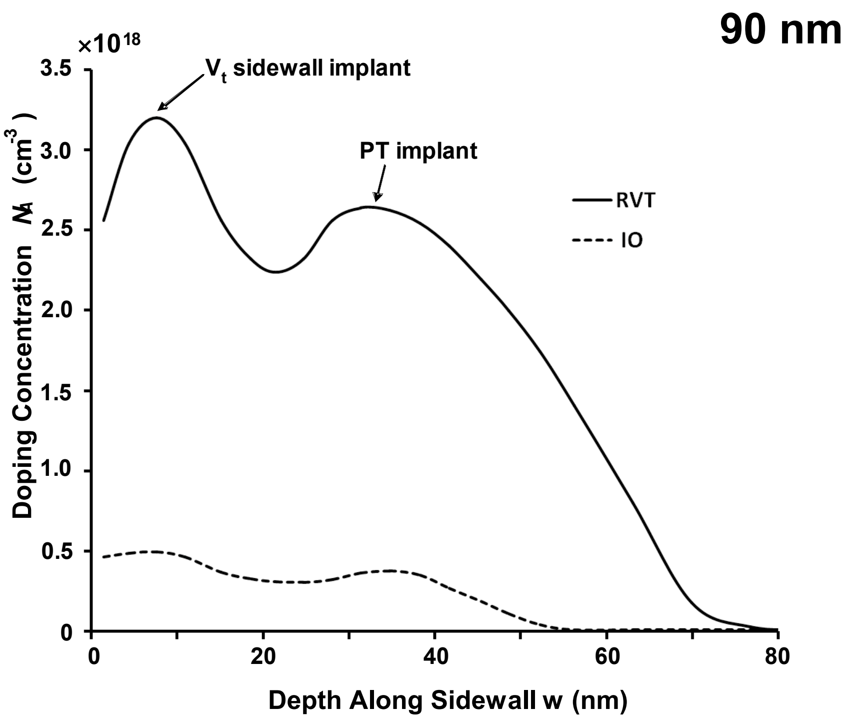
Doping, t_{ox} vs. sidewall depth

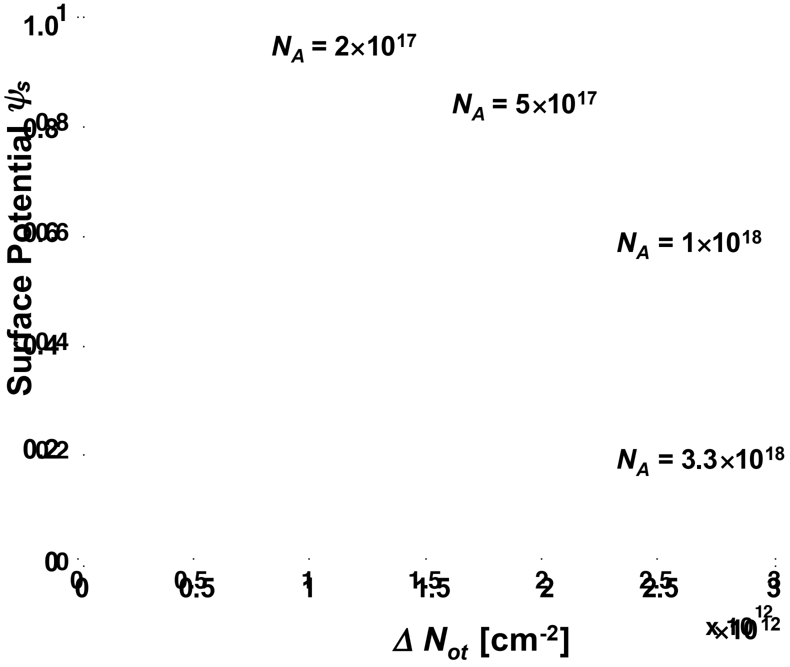


- **Model requires estimates along sidewall**
  - **doping concentration (primary fitting parameter)**
  - **effective oxide thickness**

$$t_{ox}(i) \approx \frac{\partial}{2} z(i)$$

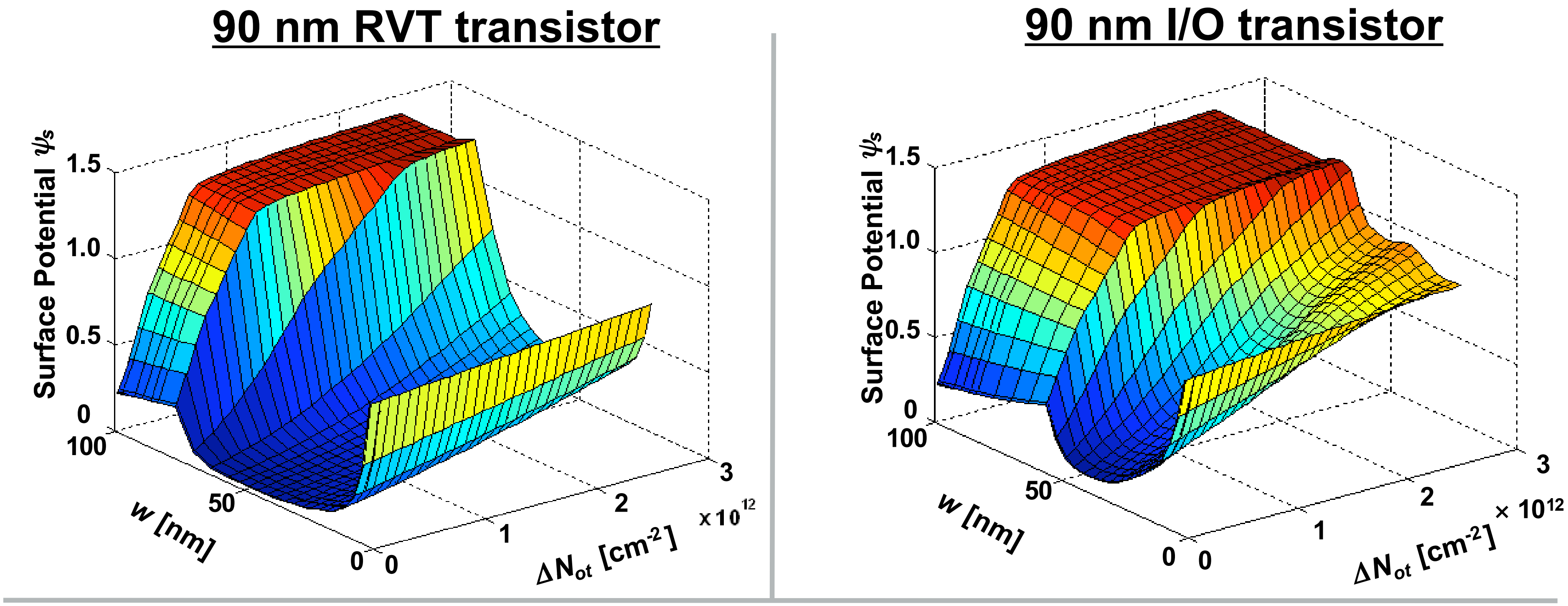
Effect of doping on ψ_s





- ***Increased doping near the top edge of the STI sidewall reduces the impact of the sidewall parasitic transistors***
- ***Lower doping values translate to a higher surface potential for a given N_{ot} buildup and oxide thickness***

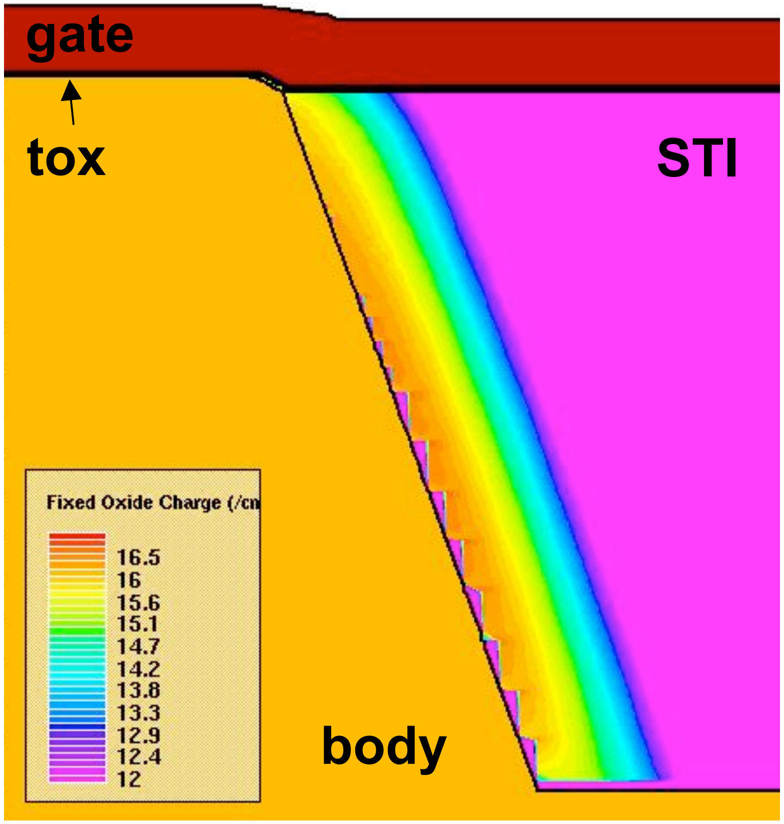
Effect of doping on ψ_s (cont.)



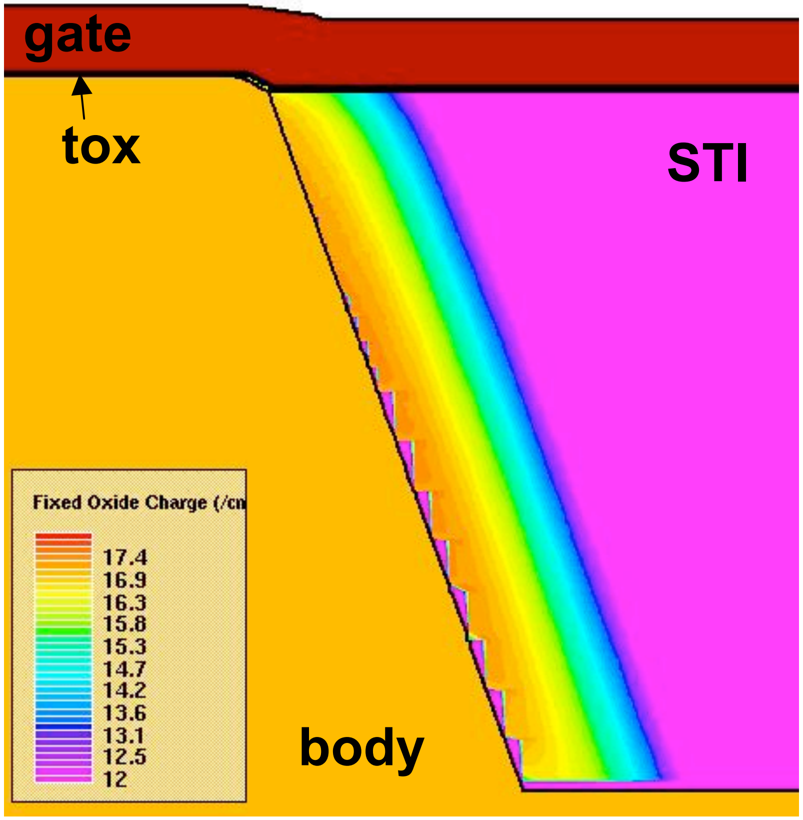
- As N_A is increased, there is a decrease in surface potential (i.e., a valley with respect to *w*)
- If $N_A > 1\times10^{18}$ cm^{-3}, fluctuations in the doping profile will have a negligible impact on ψ_s
- if $N_A < 1\times10^{17}$ cm^{-3}, non-uniformities in the profile will strongly affect ψ_s

TCAD Calculation of N_{ot} distribution

2-D device simulations using radiation enabled module in Silvaco Atlas approximate N_{ot} buildup along sidewall

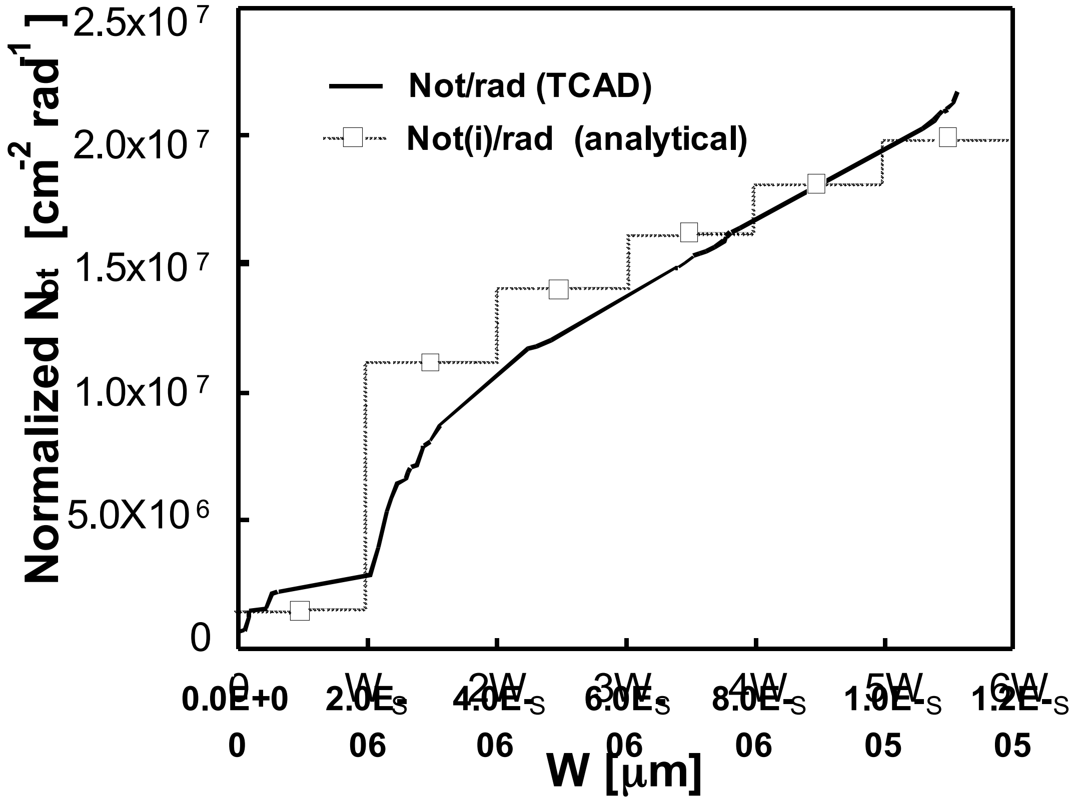


1 krad



10 krad

Model for defect generation (N_{ot})



$$t_{ox}(i)$$

$$\varepsilon_{ox}(i) \approx \frac{V_{gb}}{t_{ox}(i)}$$

$$f_y(i) \approx \frac{å_{ox}(i)}{å_{ox}(i) + å_0}$$

$$ÄN_{ot}(i) \approx N_T óDg_o f_y(i) t_{ox}(i)$$

Effects on surface potential

Calculations of trapped charge and interface traps used in defect potential expression for ith device

bulk potential (doping)

$$\text{ö}_{nt}(i) = \frac{q}{C_{ox}}\left(N_{ot}(i) - D_{it}(i)\cdot\left(\text{ø}_{s}(i) - \text{ö}_{b}(i)\right)\right)$$

surface potential

Implicit equation for surface potential solved iteratively for ith device

$$\left(V_{gb} - \text{ö}_{ms}(i) + \text{ö}_{nt}(i) - \text{ø}_{s}(i)\right)^{2} = \tilde{a}_{i}^{\,2}\cdot \text{ö}_{t} H_{i}(u)$$

Normalized e-field function

(After C. McAndrew, TED, 2002)

Model for drain current response

Surface potential responses (at both source and drain ends) can be calculated iteratively for each elementary transistor as a function of V_{gb} and inserted into drain current equations

$$I_1 = (V_{gb} - V_{fb})(\psi_{sd} - \psi_{ss}) - \frac{1}{2}(\psi_{sd}^2 - \psi_{ss}^2) - 2\frac{\gamma}{3}\left[(\psi_{sd} - \phi_t)^{3/2} - (\psi_{ss} - \phi_t)^{3/2}\right]$$

$$I_2 = \phi_t\left(\psi_{sd} - \psi_{ss} + \gamma\left(\sqrt{\psi_{sd} - \phi_t} - \sqrt{\psi_{ss} - \phi_t}\right)\right)$$

$$I_{d,i} = \mu_n \frac{W_s}{L} C_{ox}(I_1 + I_2) \qquad I_d = \sum_{i=1}^{N} I_{d,i}$$

ψ_{sd} → ψ_s at drain

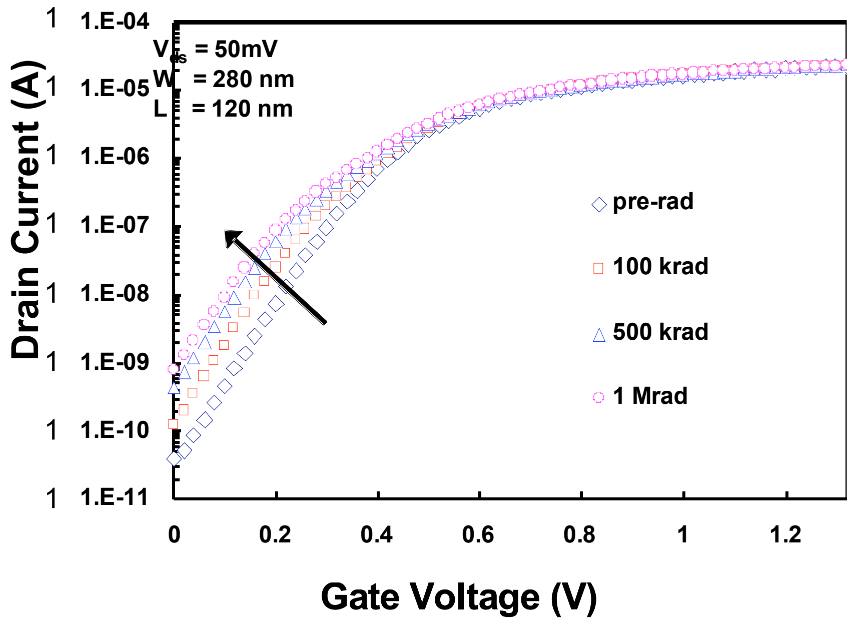
ψ_{ss} → ψ_s at source

I_1 → **Drift Component**

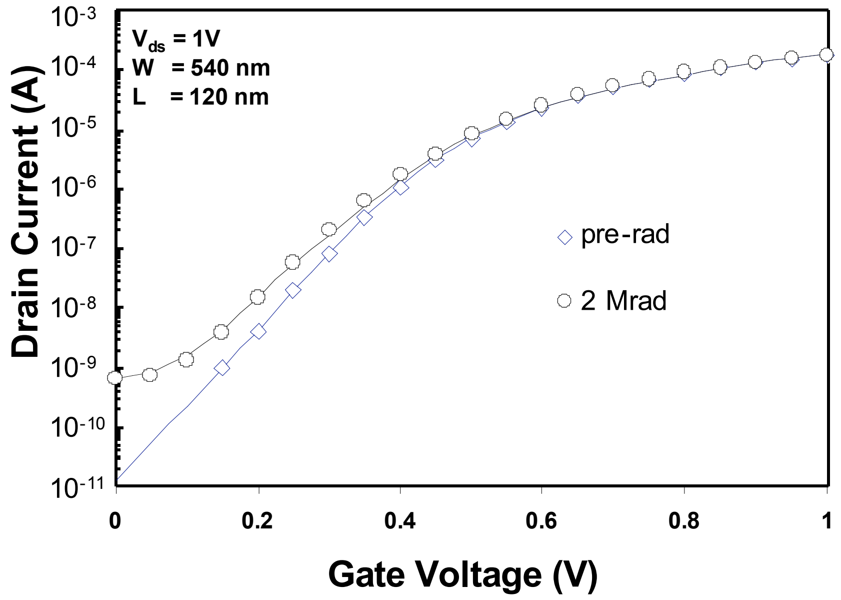
I_2 → **Diffusion Component**

Comparison of data and model

130 nm data



90 nm data



Comparison of measured pre- and post-irradiation data (symbols) with modeled radiation response characteristics (solid lines) for single stripe nFETs in 130 and 90 nm technologies

Summary

eed for accurate radiation-enabled models (e.g., edge leakage) that can be implemented in circuit simulators is growing

odel based on new technique which calculates non-uniform defect distributions and surface potential responses along the STI sidewall to model the parasitics

imulated results using the model compare well to experimental data obtained on 130 nm and 90 nm devices

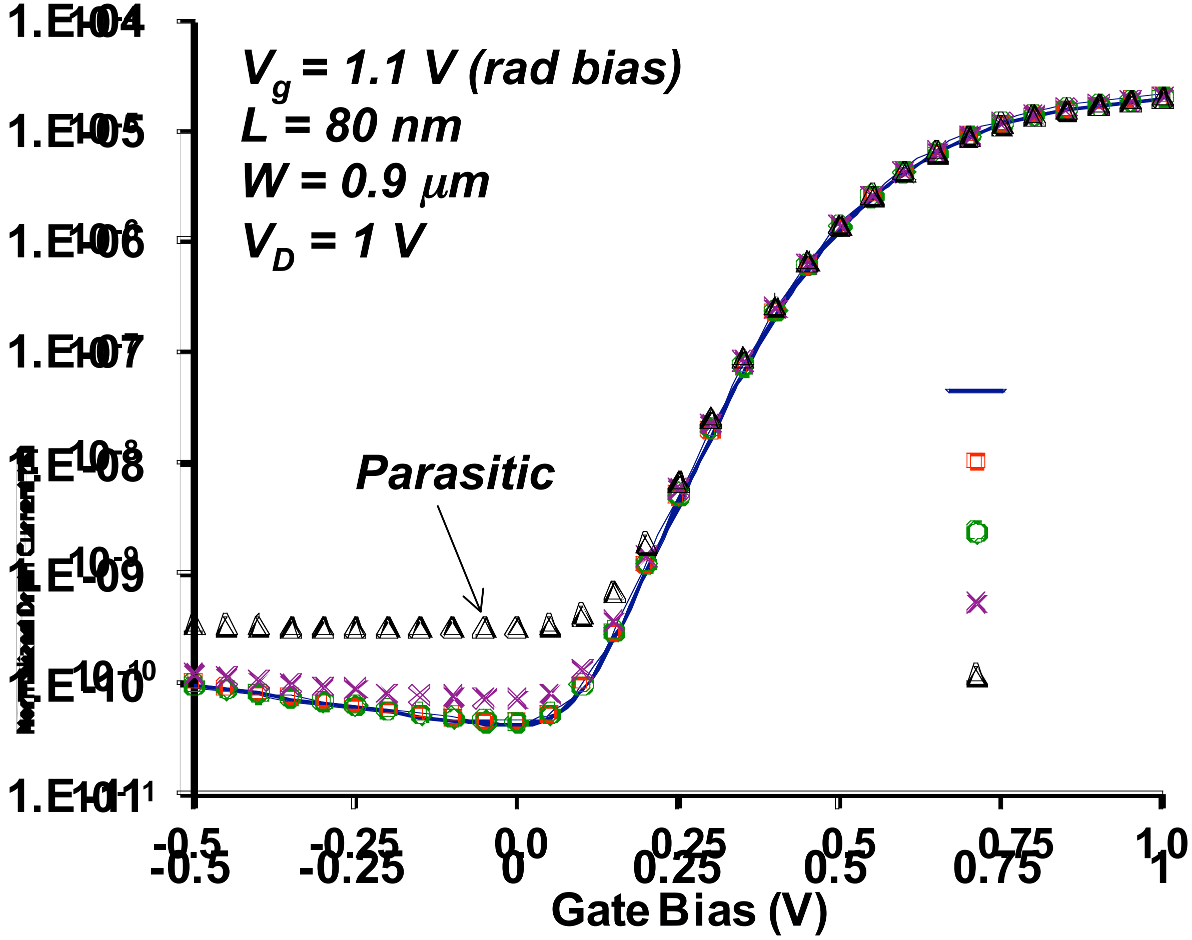
odel predicts that in deep-submicron technologies, the doping concentration near the sidewall corner has a significant impact on the radiation response

Additional Material

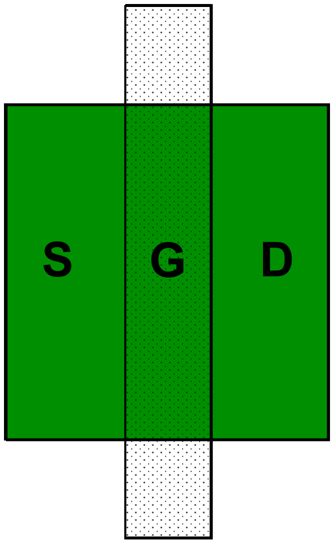
Single and Multi-Finger Devices

Experimental results: *W* < 1 μm

Single stripe 90 nm device is fairly radiation tolerant to TID

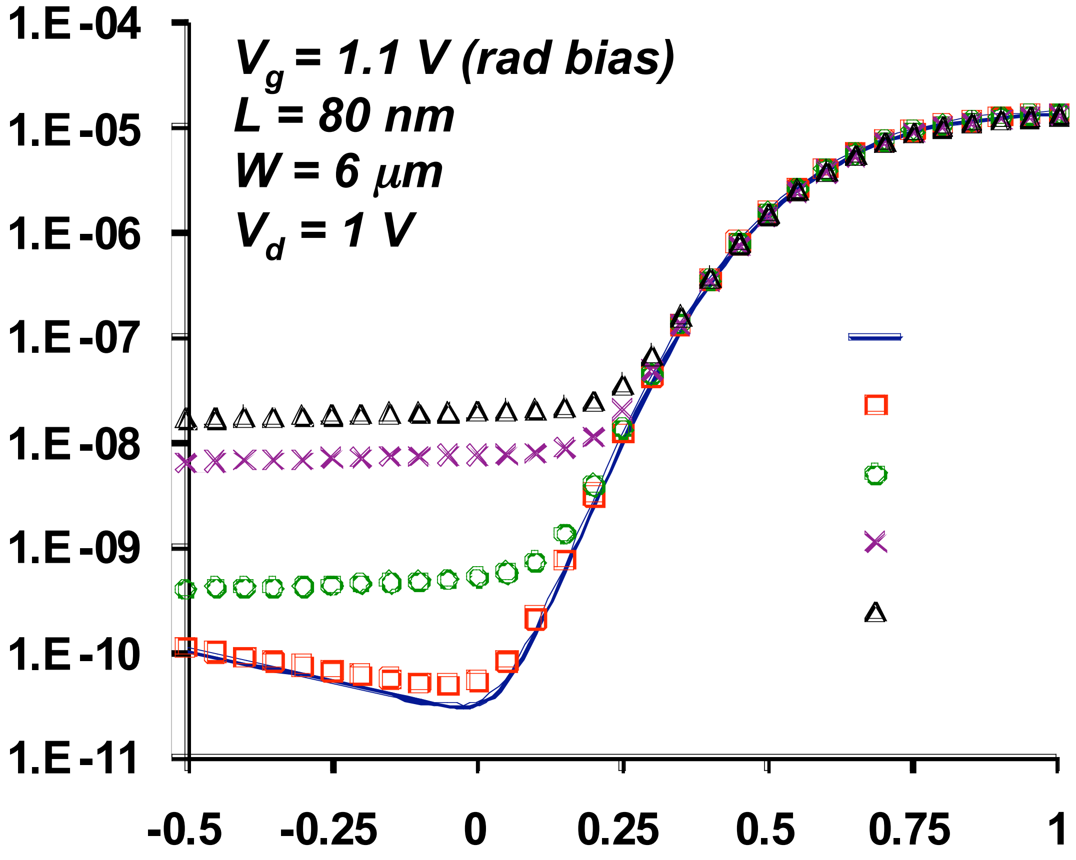


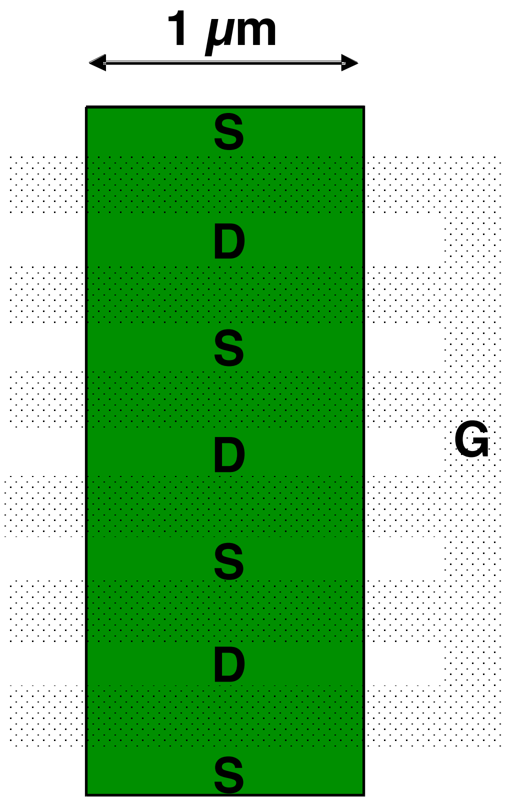
Data suggests that "as-drawn" device in parallel with parasitic device in strong inversion



Experimental results: $W > 1\ \mu\text{m}$

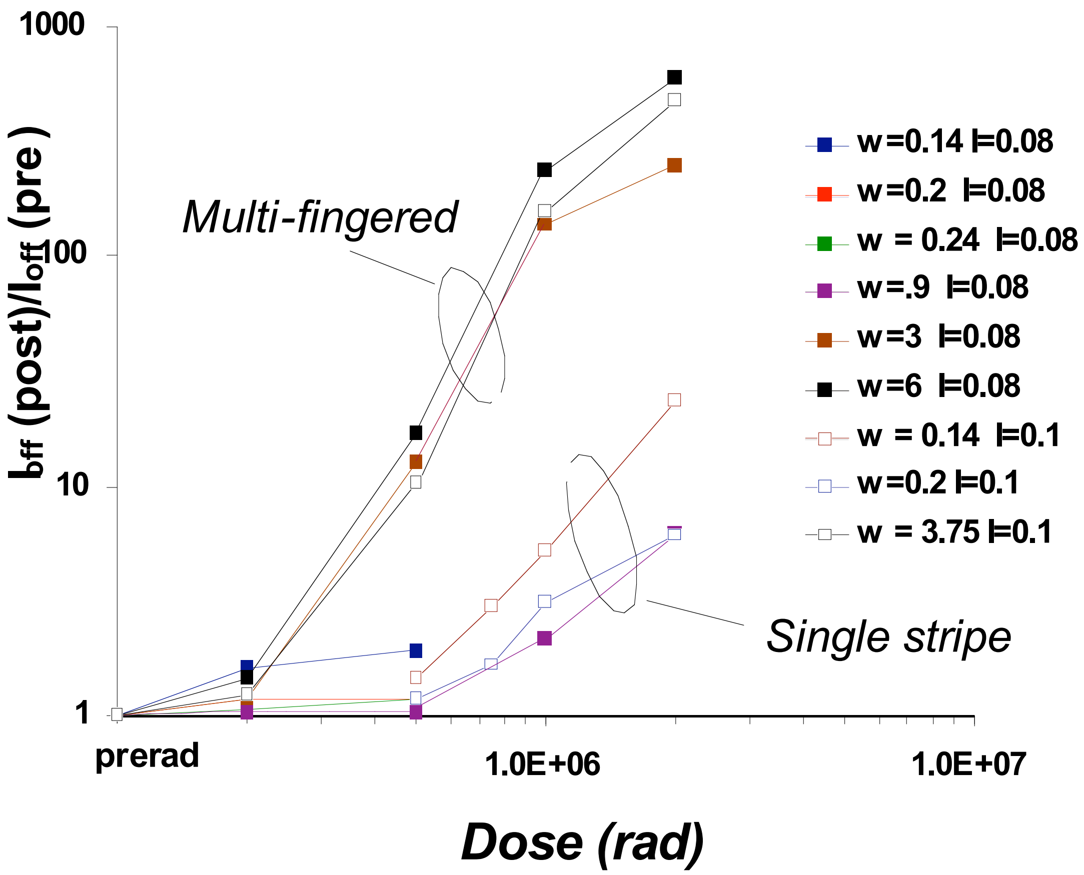
Radiation response for multi-fingered 90 nm device shows increased susceptibility to ionizing radiation





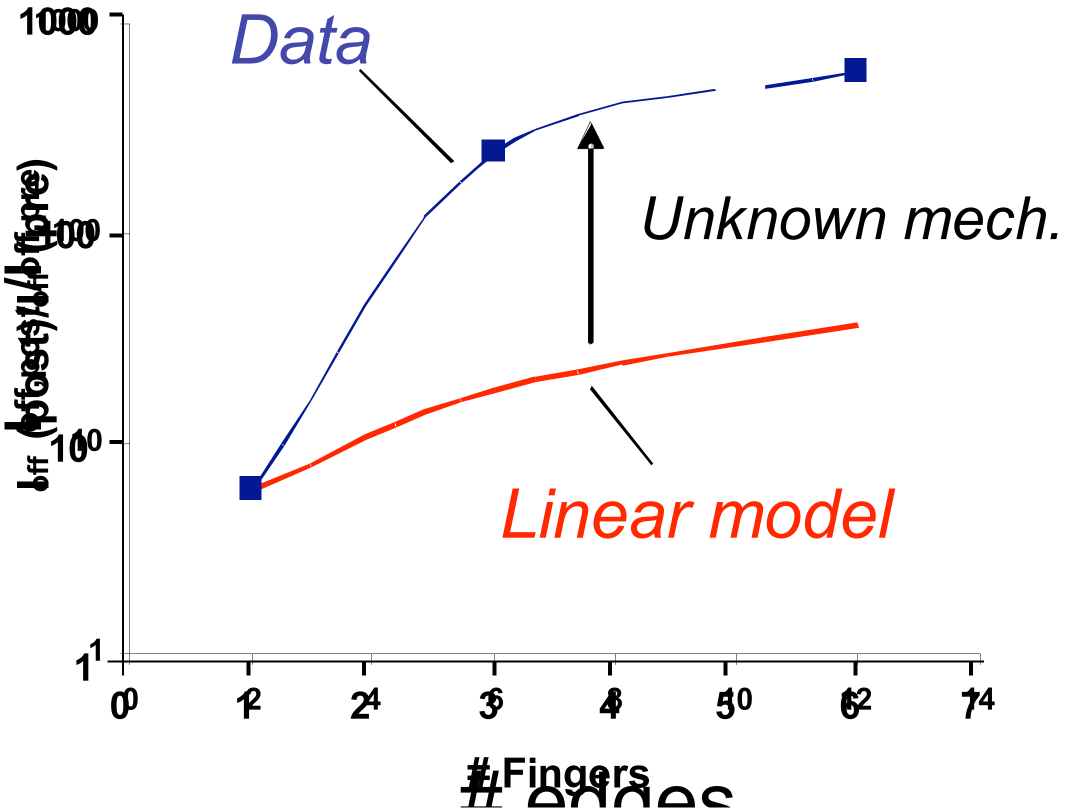
Comparison of devices

Offstate leakage current (I_{off}) ratio



- I_{off} defined as current at V_g= 0 V
- Data shows that as gate width increases, *offstate leakage ratio* significantly increases
- Multi-fingered devices significantly more susceptible to TID than single stripe devices

Failure of linear model



- **Linear model predicts**

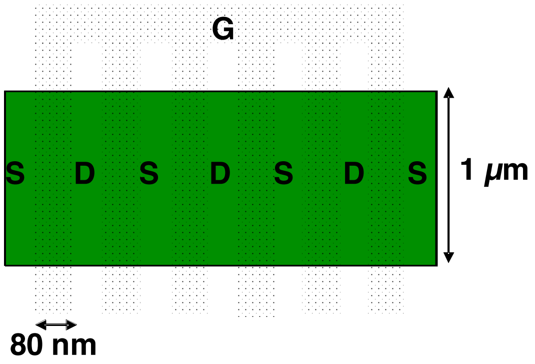
$$I_{off}\ (m=n) = n*I_{off}\ (m=1)$$

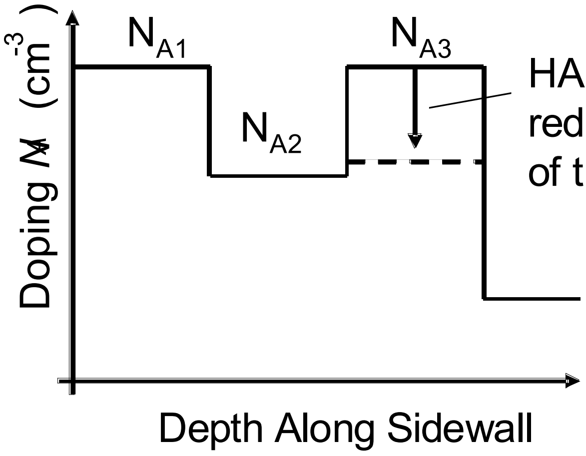
n = # fingers

- **Data shows super-linear increase in TID sensitivity**
- **Discrepancy suggests secondary cause needed to explain multi-finger response**

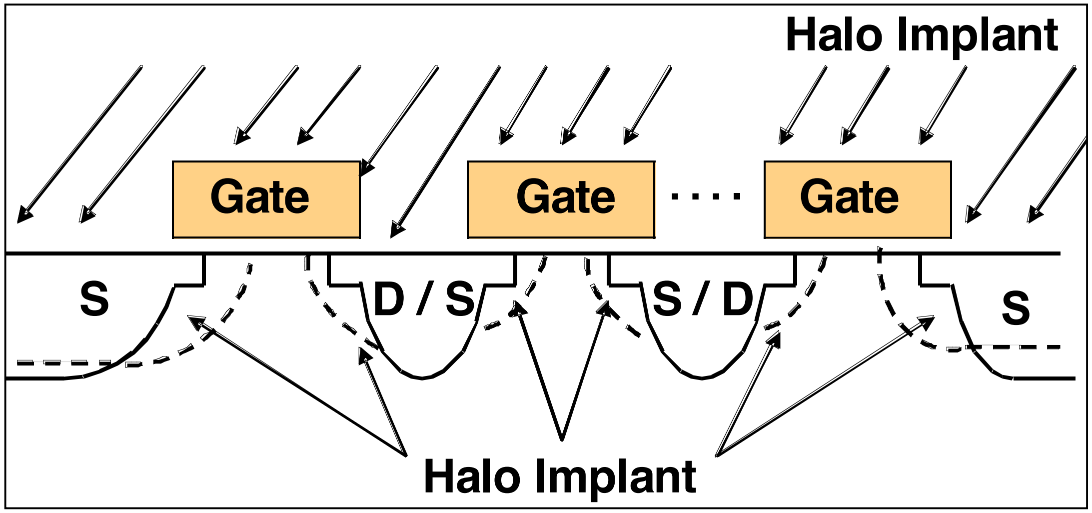
Potential Cause

Halo Implant Masking





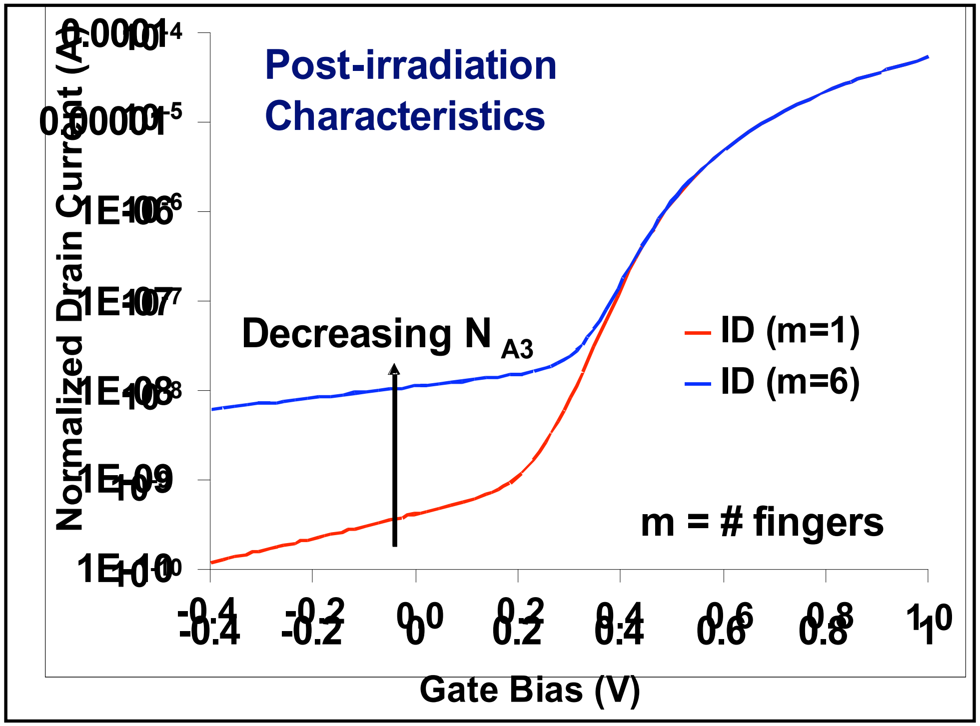
HALO masking reduces doping of thick parasitic



Outer poly gate fingers may block halo implant on inner fingers

Effect of lower doping

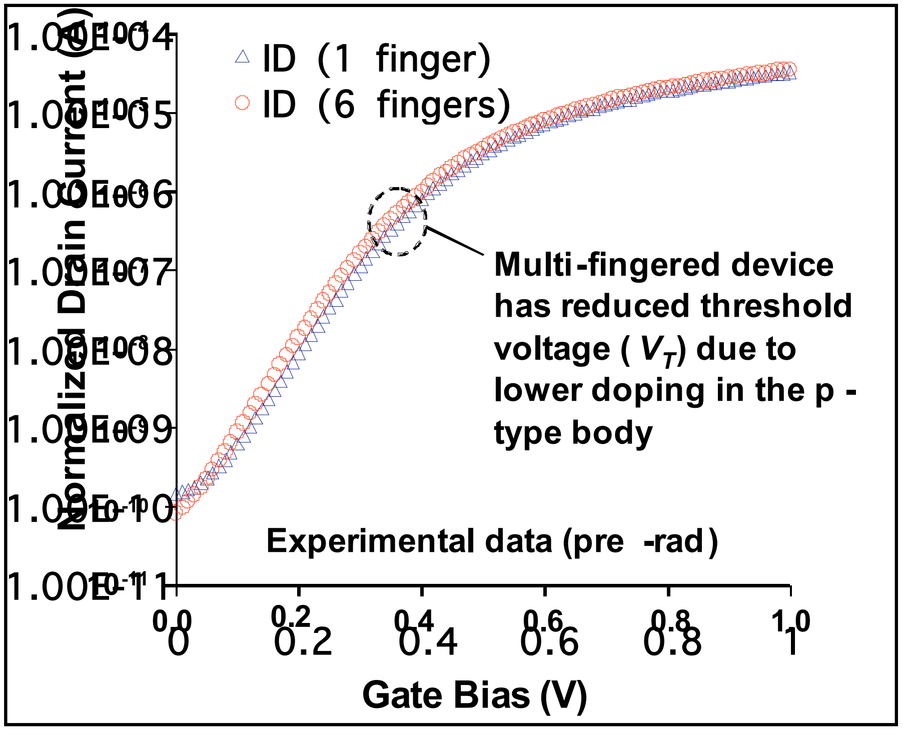
N_{A3} (single stripe) ≈ 1.25 × N_{A3} (multi-finger)



Post-irradiation Characteristics

Decreasing N_{A3}

m = # fingers



Multi-fingered device has reduced threshold voltage (V_T) due to lower doping in the p-type body

Experimental data (pre-rad)

Pre-irradiation experimental data used to approximate doping difference (lower doping explains increased sensitivity to TID)

Single and multi-finger device summary

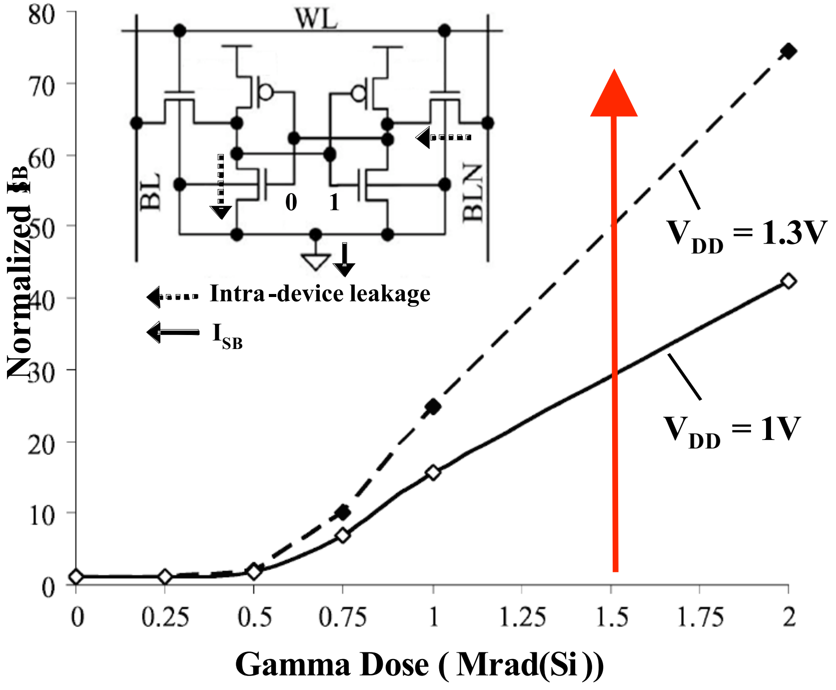
- Multi-fingered devices show a super linear increase in TID sensitivity
- Potential cause for increased susceptibility is halo implant masking (lower effective p-type body doping)
- Increased TID susceptibility in multi-fingered devices could have circuit design implications in this technology

Field Oxide Leakage

SRAM vs. Device 90nm comparison

4T SRAM

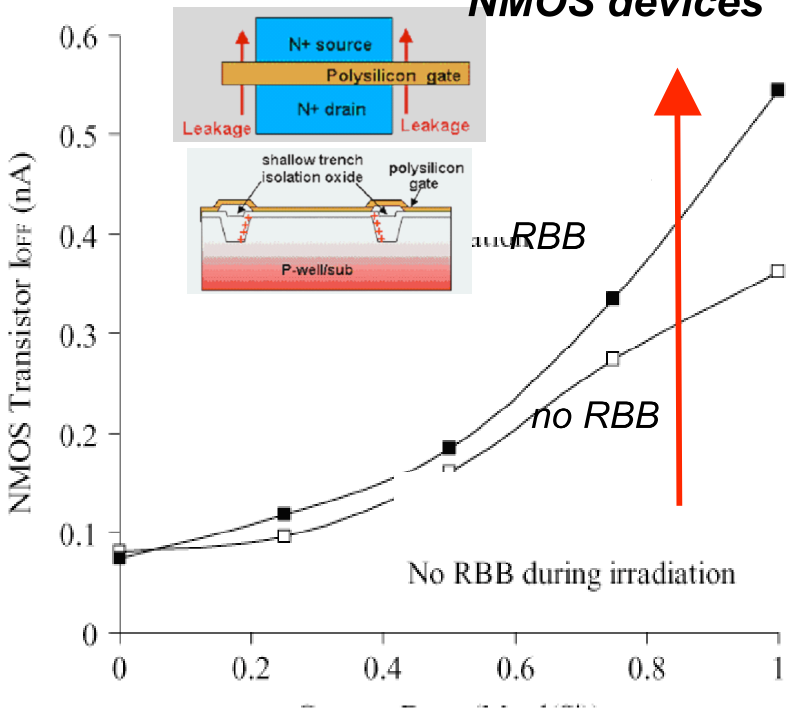
> 100X increase in static supply current in SRAM array



After Clark TNS 2007

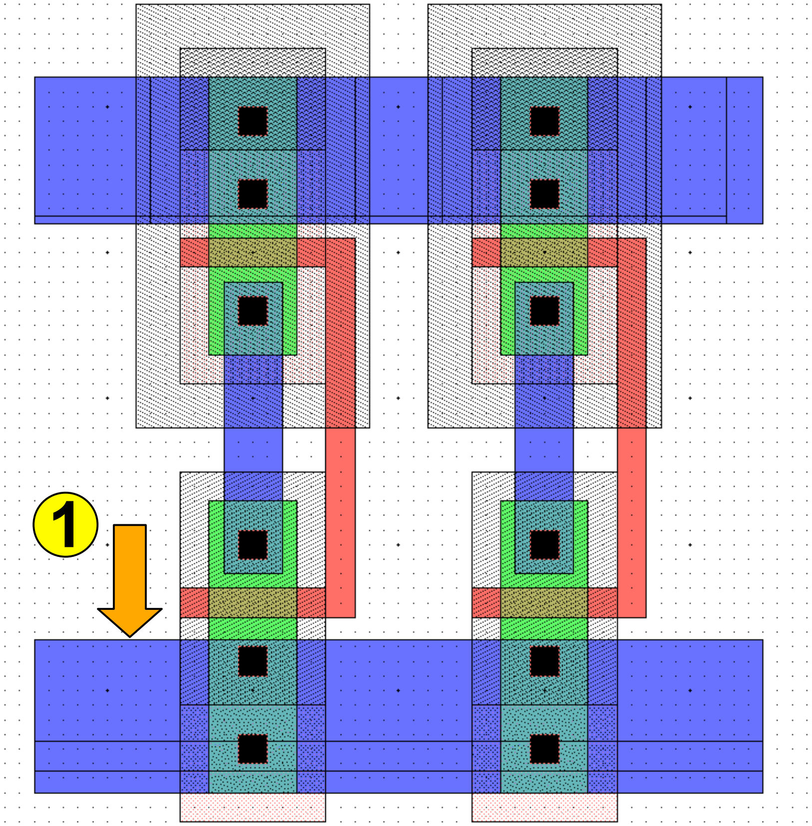
NMOS XSTOR

< 10X increase in off-state leakage in NMOS devices

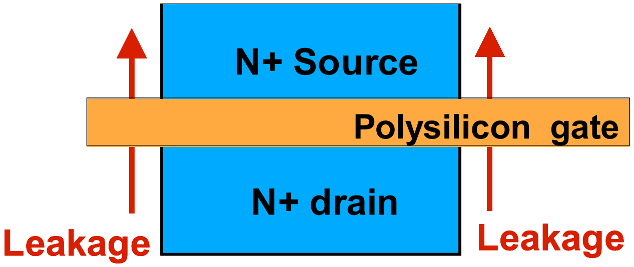


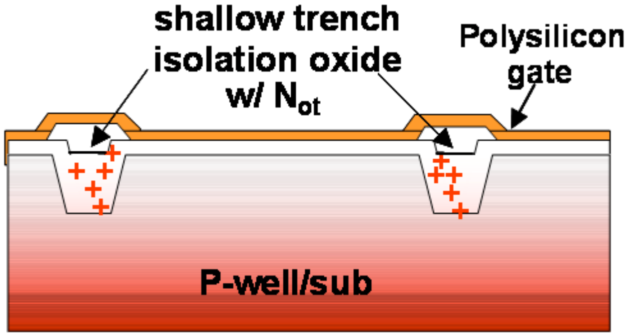
Lack of correlation between circuit and device response suggests inter- device and/or inter-cell leakage due to <u>field oxide leakage</u>

Leakage paths

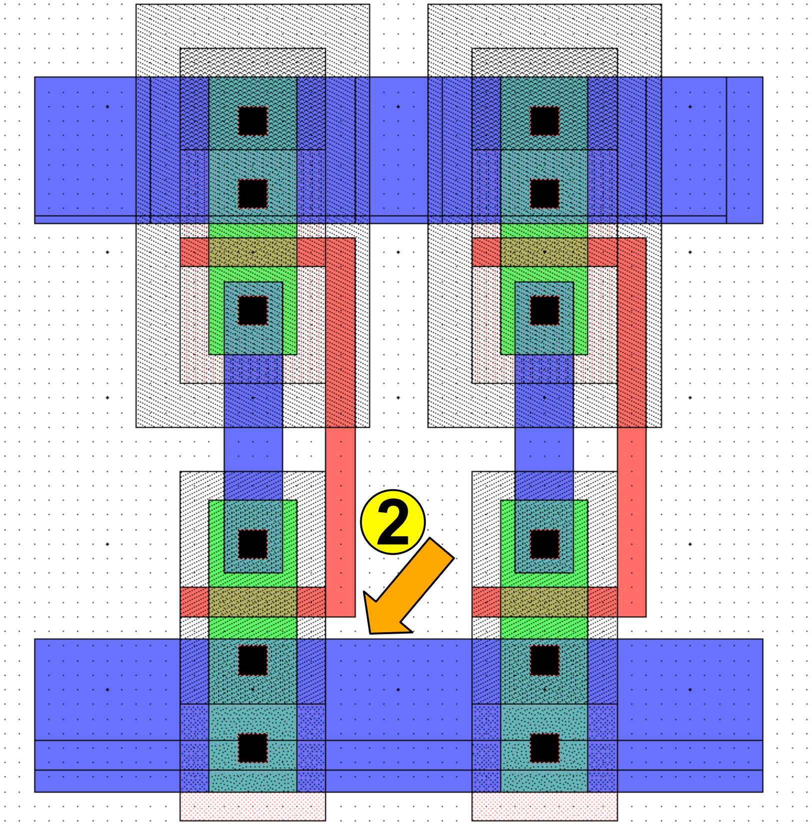


① NMOS Drain-to-Source

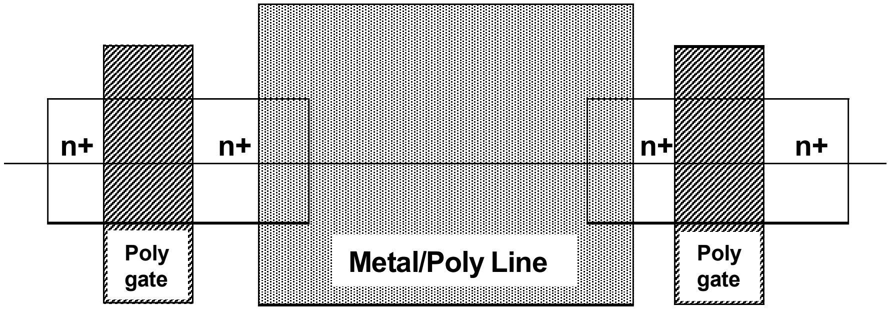


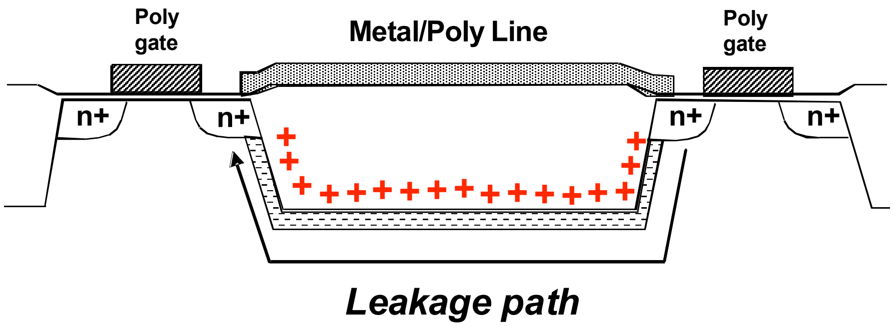


Leakage paths

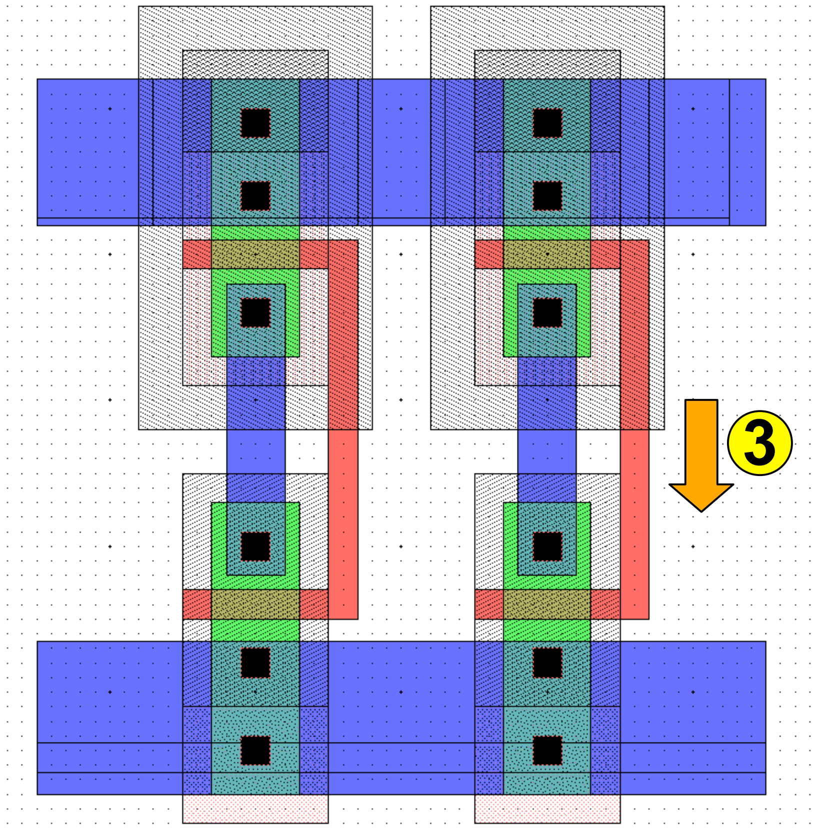


② NMOS D/S to NMOS S/D

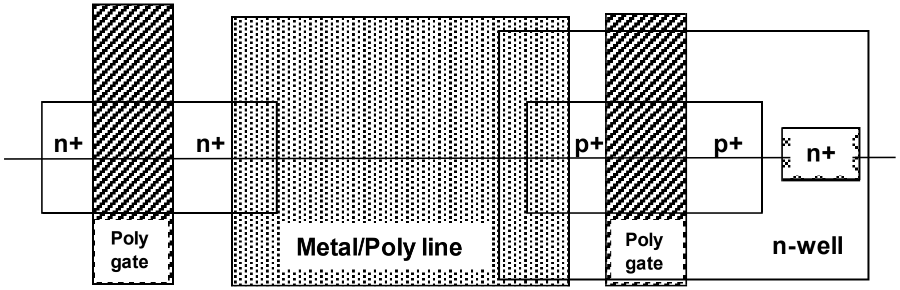


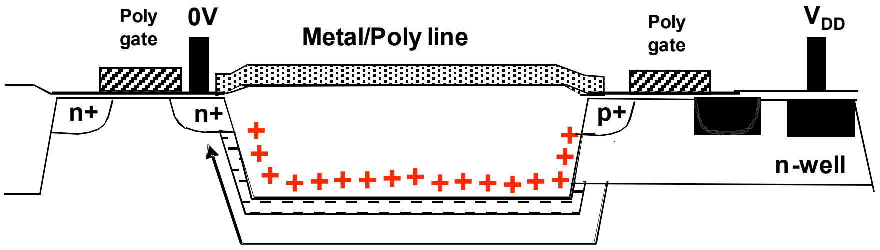


Leakage paths



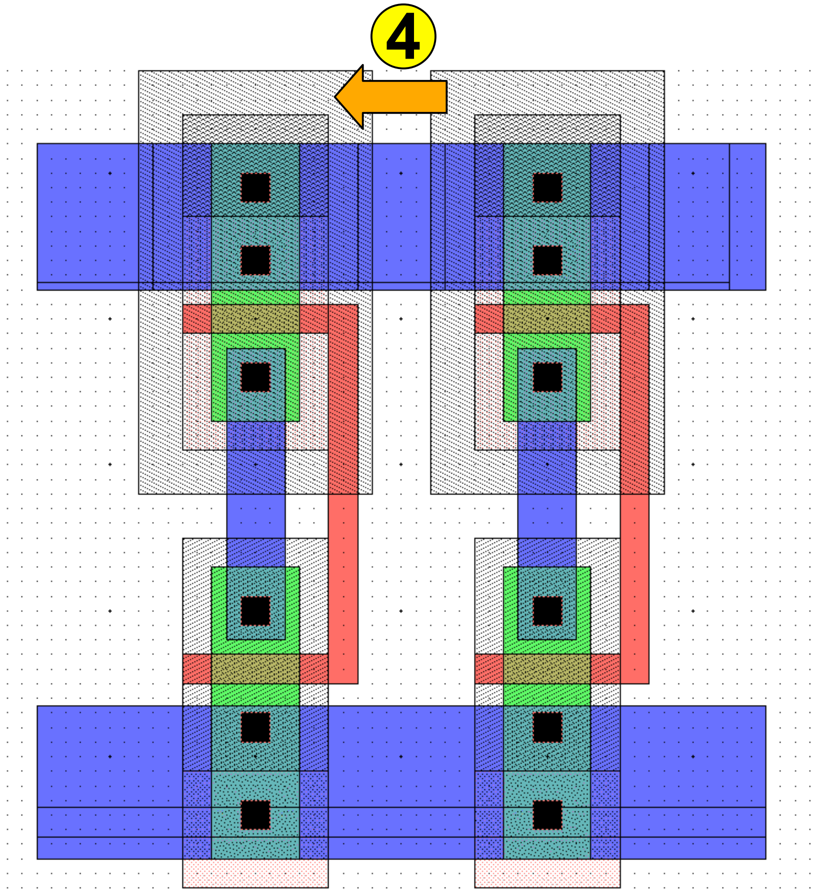
③ NMOS D/S to NWELL





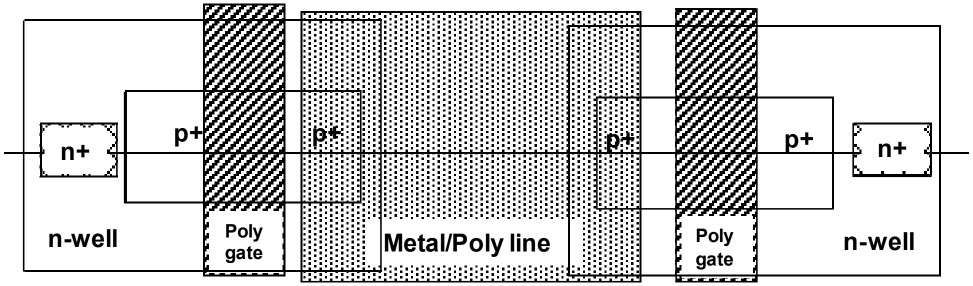
Leakage path

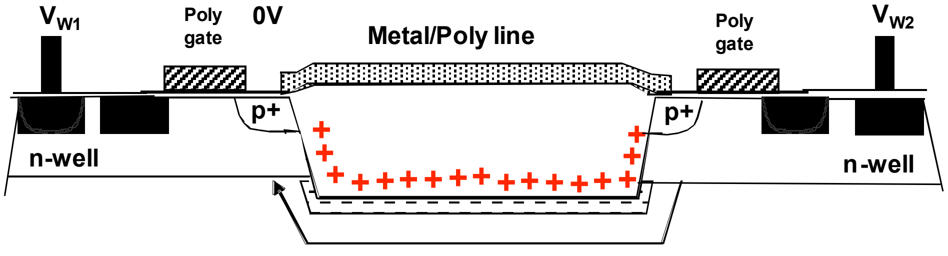
Leakage paths



④ NMOS NWELL to NWELL

(only if wells at different potential – rare in SRAM)





Leakage path

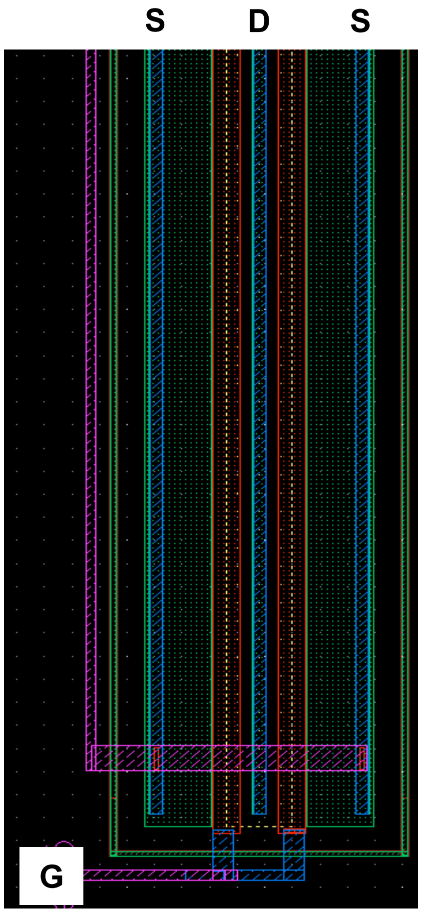
Test structures

FOXFET variants

- 3 n+-to-n+ w/ metal gate
  - w/ GB (L = 0.5 μm)
  - w/o GB (L = 0.5 μm and L = 0.14 μm)
- 3 n+-to-nwell w/ metal gate
  - w/ GB (L = 0.55 μm)
  - w/o GB (L = 0.55 μm and L = 0.21 μm)
- 1 n+-to-n+ w/ poly gate (L = 0.2 μm)
- 1 n+-to-nwell w/ poly gate (L = 0.28 μm)
- 2 nwell-to-nwell w/ poly gate (L = 1.5 μm and L = 0.9 μm)

All FOXFETs designed with 200 μm gate width

Example: N+ to Nwell w/ poly gate

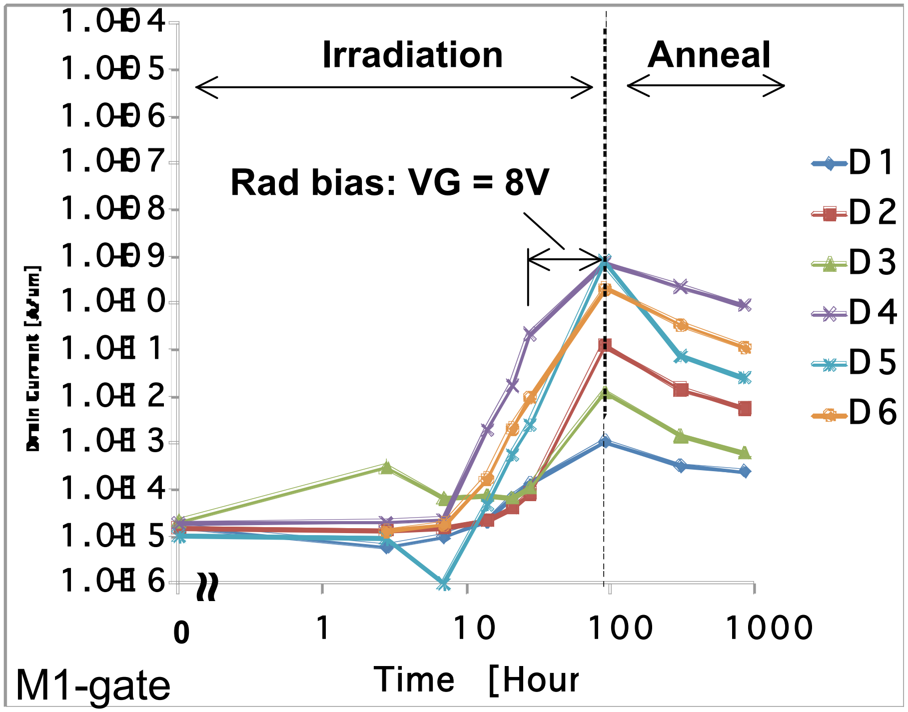


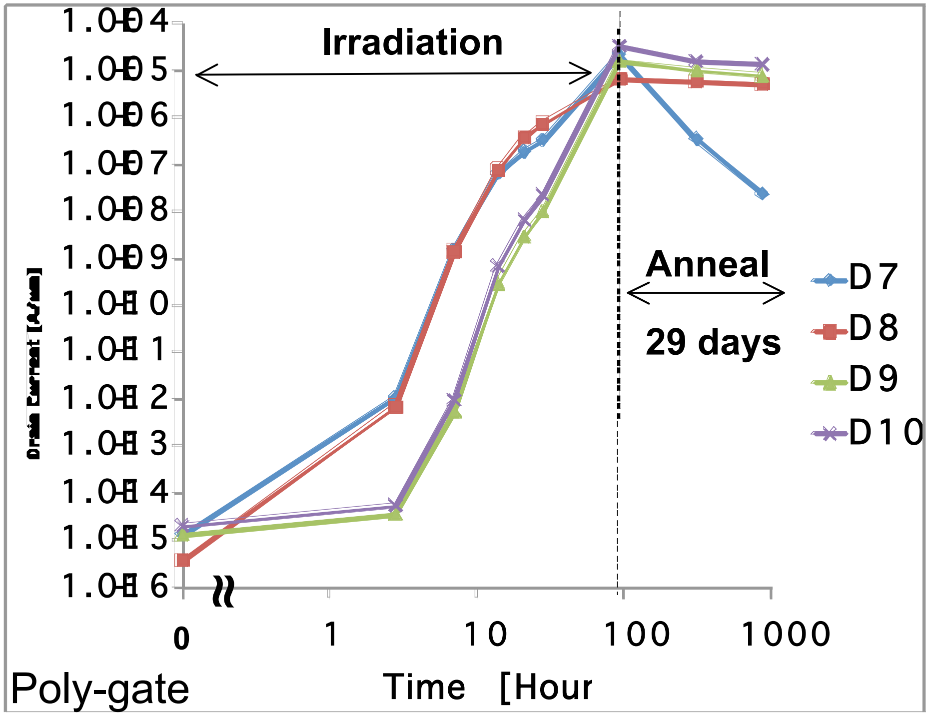
Legend

	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
Gate	M1	M1	M1	M1	M1	M1	Poly	Poly	Poly	Poly
Drain	n^+	n-well	n^+	n-well	n-well	n^+	n-well	n-well	n-well	n^+
Source	n^+	n^+	n^+	n^+	n^+	n^+	n-well	n-well	n^+	n^+
Guardband	yes	no	no	yes	no	no	no	no	no	no
Length, L (μm)	0.5	0.55	0.5	0.5	0.21	0.14	1.5	0.9	0.28	0.2

TID Results (LP)

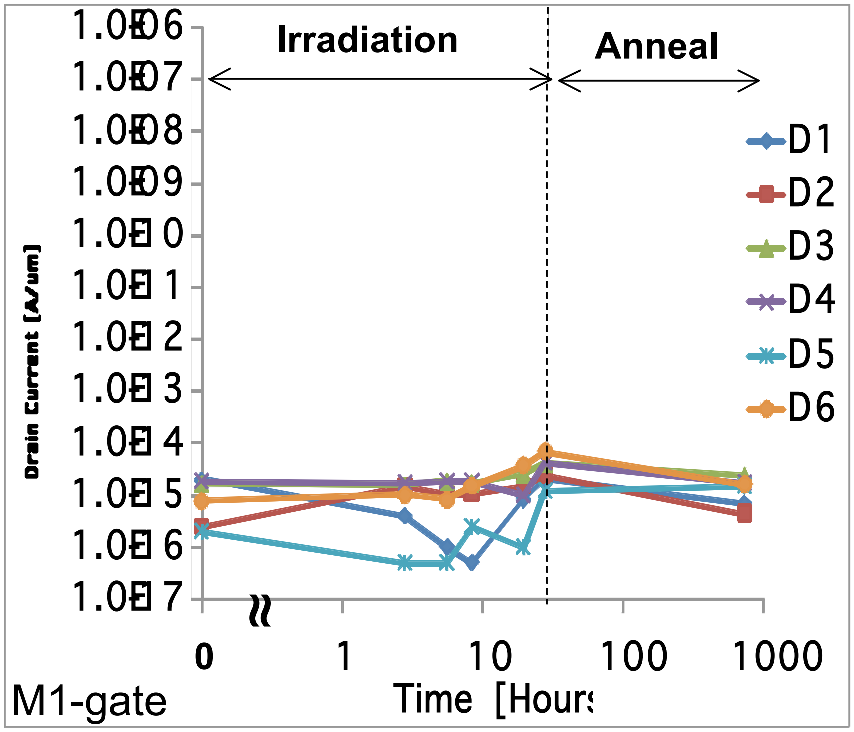
- During irradiation, $V_g = 1.2$ V for $0 < t < 30$ and $V_g = 8$ V for $30 < t < 90$
- Measurement bias: $V_g = 1$ V, $V_d = 1$ V, $V_s = V_b = 0$ V
- 7-9 magnitude increase in poly-gate devices
- < 4 magnitude increase in M1-gate devices
- Slight length effect

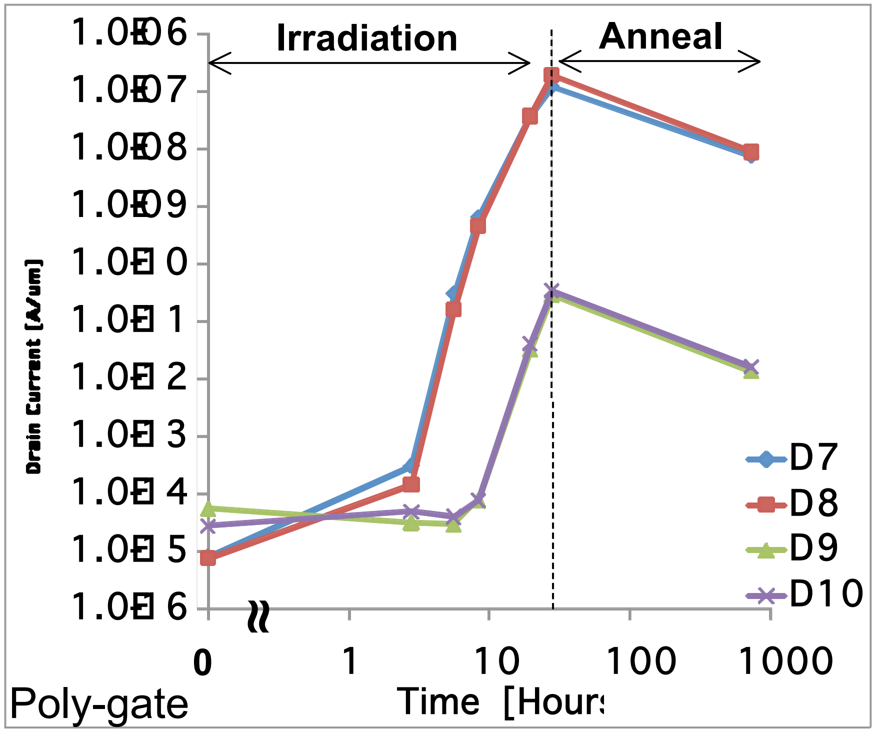




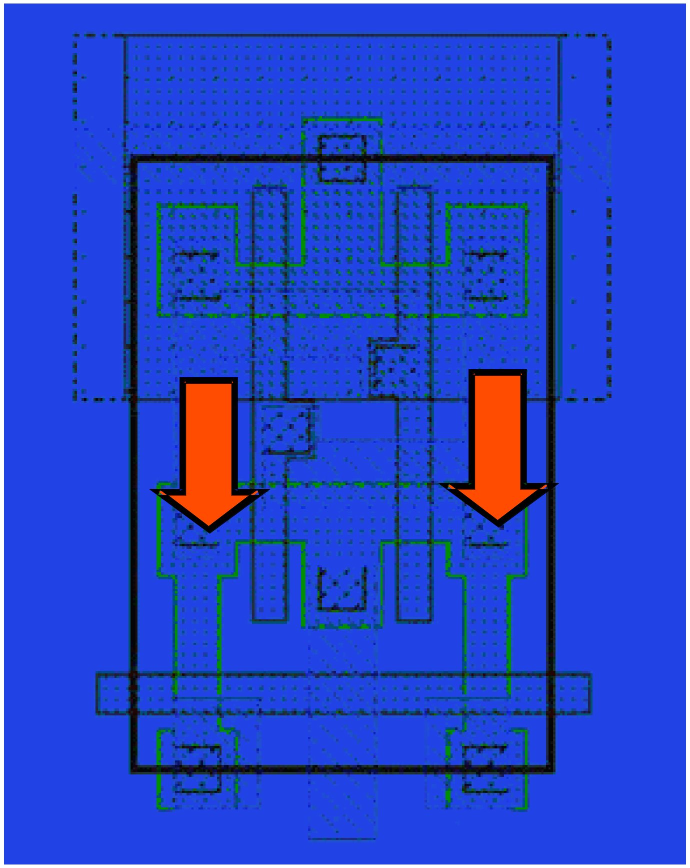
TID Results (SF_1)

- Measurement bias: V_g = 1 V, V_d = 1 V, V_s = V_b = 0 V
- 4-8 magnitude increase with poly-gate (much harder than LP)
- No TID threat in SF field path with metal overlap
- Slight length effect

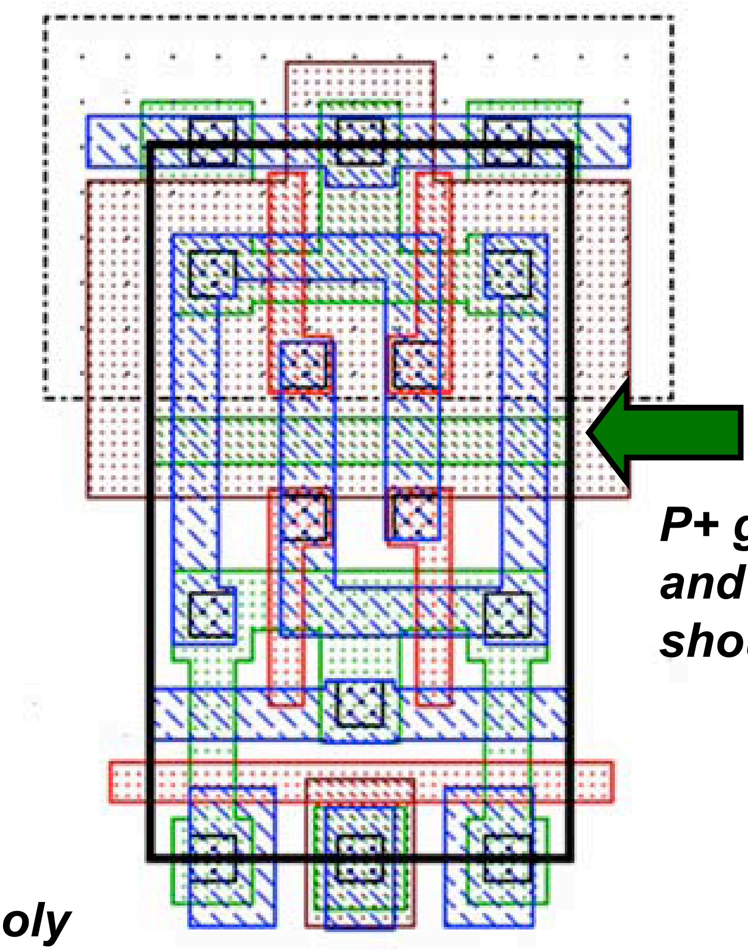




Design implications

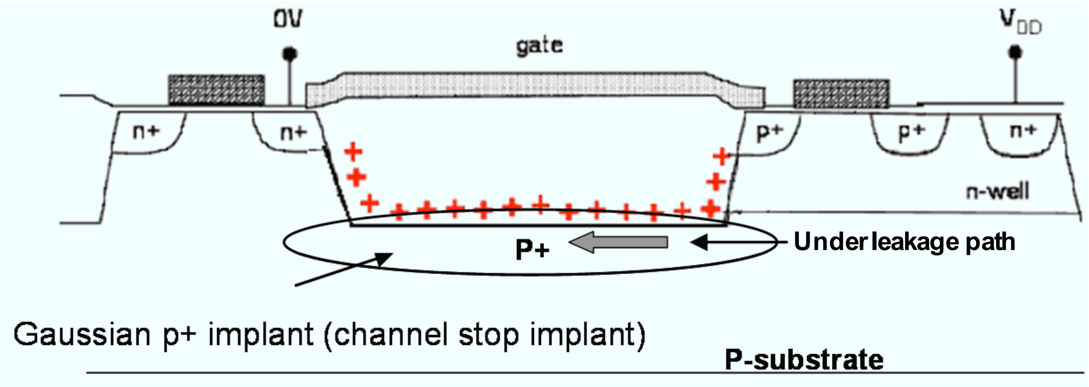


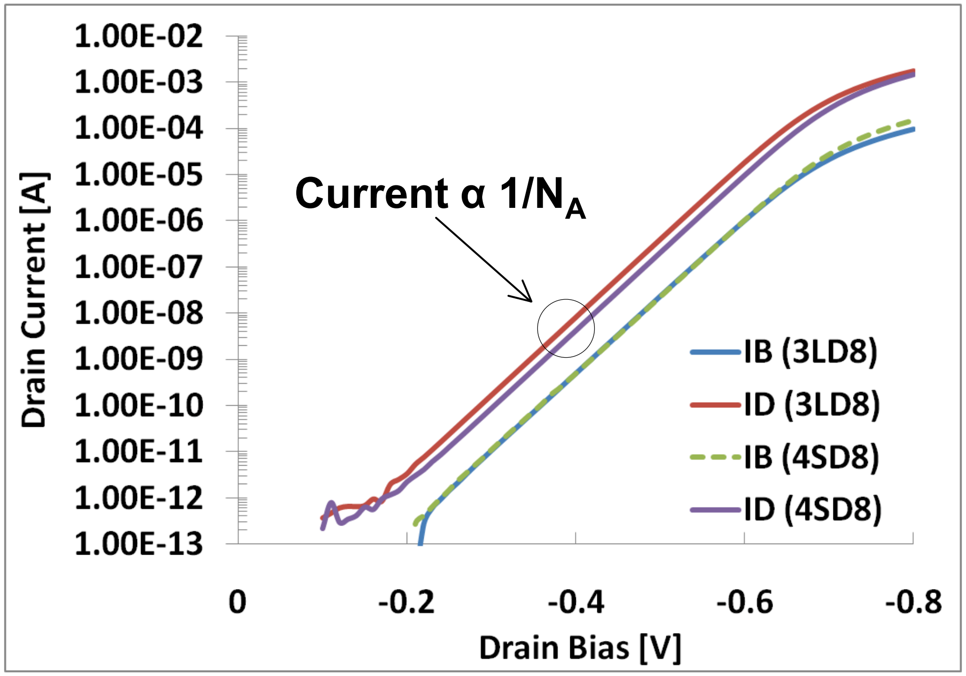
N-well to n+ drain leakage under poly could be problem in standard SRAM

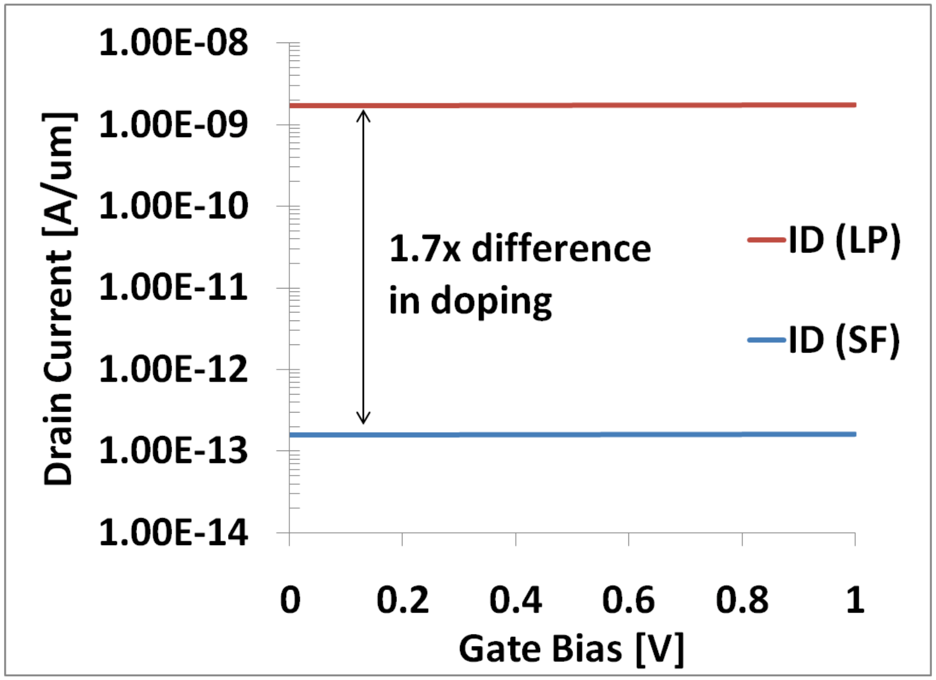


P+ guard-band and metal route should help

SF vs LP – A doping effect







FOXFETs results summary

- All FOXFET variants in LP and SF technologies were tested up to 2 Mrad
- Results showed significant degradation in poly-gated n-well to n-well devices (not a large concern for most designs)
- Measurable degradation in n+ to n-well and n+ to n+ poly gated parts
  - Could be cause of unaccounted for leakage in SRAM and other ICs
- Reverse body bias will mitigate leakage
- Annealing looks fairly normal, but biased anneals should be run
- Metal gated devices were much harder than poly-gate devices (impact of oxide efield on charge yield on defect buildup in FOX)
- LP was considerably softer than SF (effect of lower doping in body)