#### Multiple-Bit Upset in 130 nm CMOS Technology



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### MBU increases with IC scaling

- Reliability
  - Memory design
  - Testing
- MBU has been shown to increase for smaller technologies



Proton-Induced MBU

from Seifert, et. al, Intel. IRPS, 2006.

# Soft technology

130 nm **CMOS** 

• IBM 8RF

- High density **CMOS SRAM**
- Low upset threshold ~ 2 MeV-cm<sup>2</sup>/mg



# Modeling methodology

V

- Sensitive volume
  - Depth
  - Lateral dimensions
- Physical model
- Simulation MRED
- Energy deposition cross section  $\sigma_{\rm ED}({\rm E})$
- Correlate  $\sigma_{\text{ED}}(\text{E})$  to MBU



 Ion Beam Induced Charge Collection (IBICC)
36 MeV Oxygen
7 MeV-cm<sup>2</sup>/mg
~ 0.07 pC/ μm



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![](_page_9_Figure_1.jpeg)

### Sensitive volume definition

![](_page_10_Picture_1.jpeg)

- Depth
  - From IBICC
  - $-1 \ \mu m$
- Lateral area
  - Process specific
  - 0.4  $\mu m$  x 0.4  $\mu m$
- Spacing

![](_page_10_Figure_9.jpeg)

![](_page_10_Figure_10.jpeg)

![](_page_11_Figure_1.jpeg)

- Equivalent

- 63 MeV Protons
- Radiative Energy Deposition (**MRED**)

# Simulation

Monte Carlo

 204 sensitive volumes

![](_page_11_Picture_6.jpeg)

![](_page_11_Figure_7.jpeg)

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# Energy deposition cross section

![](_page_12_Figure_1.jpeg)

# Single volume $\sigma_{\text{ED}}$

![](_page_13_Figure_1.jpeg)

![](_page_13_Figure_2.jpeg)

# Multiple volume $\sigma_{\rm M}$

![](_page_14_Figure_1.jpeg)

# Multiple volume probability

![](_page_15_Figure_1.jpeg)

![](_page_15_Figure_2.jpeg)

### Plan

- Multiple cell
  - DRAM
  - SRAM
- Multiple node
  - DICE latch
  - CVSL logic
- Device simulation
- Rate prediction

![](_page_16_Figure_9.jpeg)

# Summary

![](_page_17_Picture_1.jpeg)

- MBU cross section from energy deposition cross section calculation
- Single volume cross section angular dependence
  - Decreases with increasing angle
  - Aspect ratio
- Multiple volume angular dependence
  - Increases with increasing angle
  - Forward scattering
- Multiple volume probability increases with angle