Final Report
“Advanced Modeling and Test Methods for Radiation Effects on Microelectronic Devices”

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02/29/2008

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Abstract/summary:

The safety of human and robotic missions depends critically upon the reliability of electronic systems. Space radiation effects are among the greatest environmental threats to the safety of manned and robotic missions. Take, for example, life support electronics. While the crew on a manned mission may be well protected from radiation hazards, the critical life support electronics may be near the skin of the craft and relatively unprotected. Radiation effects in electronics range from loss of data to catastrophic failure. In advanced electronics, effects caused by the passage of a single energetic particle through a sensitive device are the most serious problem; while many different electrical effects have been observed, these phenomena are collectively described as single-event effects (SEEs).

Radiation effects data from newer devices, including such essential components as fiber optic systems and state-of-the art digital/mixed signal electronics, have demonstrated that existing models have significant errors. For example, using CREME96 for optocouplers underestimates single event rates, overestimating survivability. Standard models also produce inaccurate estimates for single event rates in SiGe, CMOS technologies and low-dose-rate degradation of bipolar linear ICs.

The safety and reliability of forthcoming long-duration missions will depend critically on using the most advanced electronics available and providing radiation/fault-tolerant system design. Advances in microelectronic technologies have created a situation in which time-tested methodologies for radiation-hard electronic design, validation, and verification can no longer assure the safety of electronic parts and systems used for space exploration. Therefore, a new tool is needed so that the reliability and safety of space systems can be assessed. This tool must be based upon first-principles physics computations so that engineers can predict accurately the radiation tolerance of emerging technologies in the space environment.

The objective of the current proposal is to continue to develop new technology modeling approaches for radiation induced Single Event Transients (SETs) in photodetectors and advance CMOS devices and Single Event Upsets (SEUs) in Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) and advanced CMOS devices. We will continue to develop a technology model testbed that integrates detailed transport physics models with device physics models and approximation models. This testbed will be extendable to many other technologies.

Background

NASA and DOD spaceflight missions often rely on system level solutions to mitigate the impact of a single microelectronic component failure due to exposure to the space radiation environment. This has proven to be a very effective and useful approach. These techniques range from the use of error correction techniques for data memory to redundant subsystems. In some drastic cases, system engineers have opted to power down subsystems during times when the radiation environment is severe—preventing data collection or posing significant risk to the subsystem. An example of the latter is the NICMOS instrument on the Hubble Space Telescope; radiation events in a microelectronic device require instrument operation to be discontinued while passing through the South Atlantic Anomaly region of the earth trapped radiation

environment[1]. A detailed understanding of the reliability/survivability of microelectronic devices when exposed to the space radiation environment is critical for sound system engineering decisions.

The success of a system engineering approach to radiation-effects analysis depends on the following factors: 1) A conservative model of the radiation environment for evaluating the extent to which radiation threats may compromise mission goals. 2) Measurements of component responses to terrestrial radiation sources for bounding on-orbit device performance. 3) A comprehensive physical model to predict the energy deposited in the semiconductor by terrestrial and space radiation sources. 4) Physics-based component response models to predict and analyze electrical performance degradation.

The success of such analysis depends critically on the models used for the interaction and transport of radiation through spacecraft structures and semiconductor materials. These models serve as a bridge between ground-based laboratory data and prediction of on-orbit radiation performance. They also provide guidance as to the test methods and laboratory measurements needed for such predictions.

Advances in microelectronic technologies and economic pressure to use commercial electronic parts have created a new situation in which time-tested methodologies for radiation-hard electronic design, validation, and verification can no longer assure the safety (as defined in NFS 1852.223-70) of electronic parts and systems used for space exploration. In particular, several recent developments[2] suggest that it may be appropriate to revisit the methods and models used in predicting on-orbit radiation response of modern electronics and advanced sensors. Recent radiation effects experiments on these modern technologies show trends inconsistent with current models: 1) SiGe HBTs, 2) large scale photodetectors, 3) SOI/SOS CMOS, 4) IR Focal Plane Arrays (FPAs), 5) CCDs, and 6) advanced CMOS. In particular the existing models have the following shortcomings:

- Exclude combined effects from direct and indirect ionization by incident particles
- Do not account for the angular dependence of the recoiling nuclei produced by proton-induced spallation reactions or elastic collisions
- Exclude the charge collection by diffusion
- Have limited capability to analyze detailed geometrical effects, i.e., edge effects, isolation trenches, buried oxides
- Have no method for modeling effects associated with the complex spatial variation of charge deposited by individual ion strikes.

The simple truth is that the existing techniques, developed circa 1980, fail to provide accurate reliability/survivability estimates for most modern technologies. Mature technologies have been scaled to dimensions where new phenomena challenge some of the basic simplifying assumptions of radiation effects models, which were developed for technologies fabricated in the late 70's early 80's. Some recent results suggest that current methods could yield predictions that overestimate or underestimate on-orbit error rates by an order of magnitude or more.

Technical Approach

Our approach is focused on the end goal of developing a fully-automated first-principles predictive tool that is based on the best available physics for radiation transport and microelectronic device performance. This is a Monte Carlo approach that combines three distinct concepts: 1) transport of the radiation environment though the component and relevant surrounding materials, 2) first-order approximation to estimate the response of the technology to

radiation exposure, and 3) deterministic simulation of the detailed component response to radiation exposure.

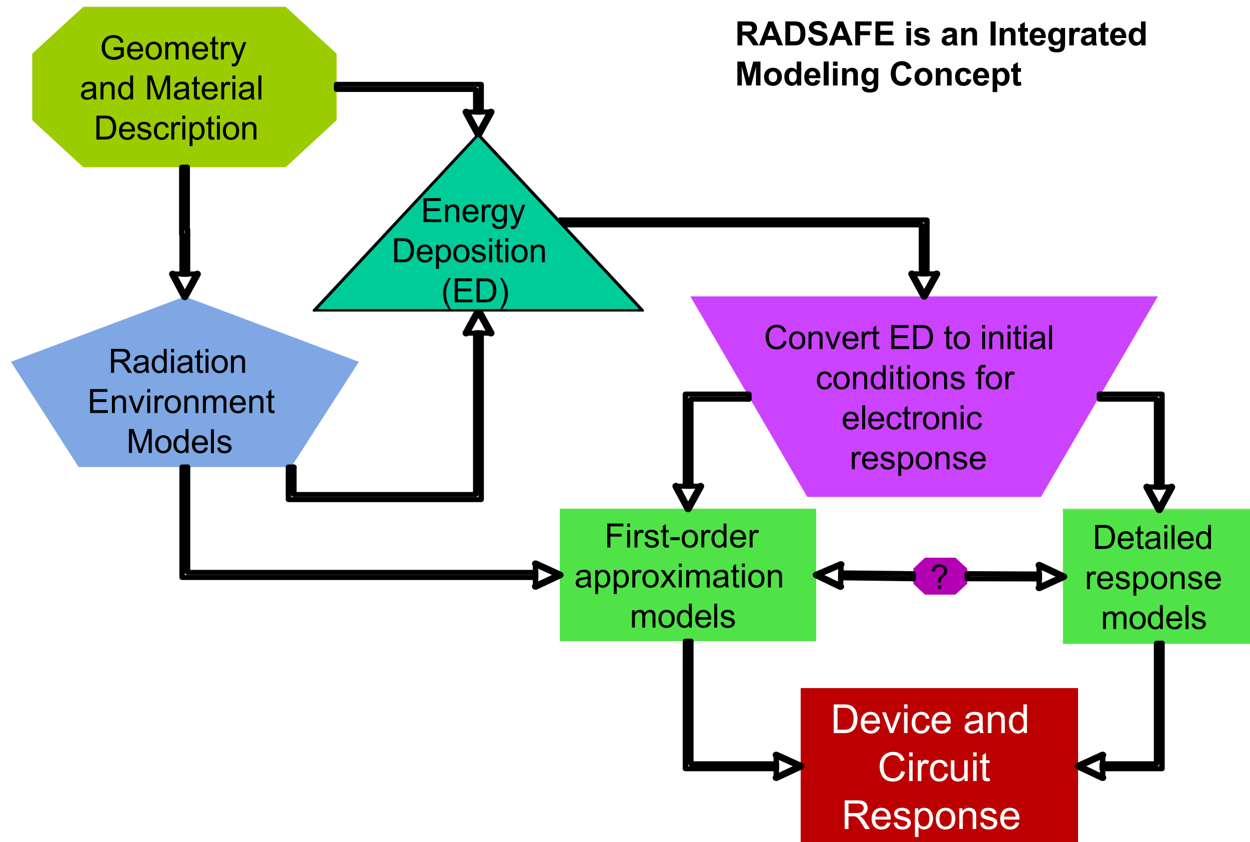

Figure 3: Conceptual diagram of the technology modeling approach

The first segment builds on existing, reliable, and well-calibrated computational physics models for the transport of radiation through matter (e.g., Geant4). Geant4 is a set of c++ class libraries for building high-energy physics detector simulation codes. Its development is coordinated by the European Laboratory for Particle Physics, CERN, in Switzerland, and is supported by the Stanford Linear Accelerator Center (SLAC), the European Space Agency (ESA), the medical physics community, and others. The stated objective for Geant4 is that it will encompass all that is known about the interactions of radiation with matter, and to do it in an extensible and flexible implementation. Because of its wide acceptance by users, who provide validation in many ways, the large and active development community, and available source code, it is an ideal component for this program. A major component of our work will be to validate the Geant4 routines for application to radiation effects in microelectronics.

The second segment is accomplished by first uncovering the basic mechanisms for the device/circuit SEE response using detailed device physics simulators (e.g., ISE's DESSIS software or Silvaco's ATLAS software) and ground based experimental data. From this understanding, we develop a first-order Quasi-Device Physics (QDeP) model for the response. QDeP models are technology dependent, can either be analytical or Monte Carlo models, account for both the energy deposition in semiconductor by the radiation event and the device response to this event, and must always over estimate the effects of radiation. The QDeP estimate allows for timely and accurate computational analysis of the device response using the

third segment by selecting only those events that have a high probability of causing an effect. (Note: Once fully developed the QDeP model for each technology can be used in a system level on-orbit predictive tool development. This new QDeP models will replace the classical models like those used in the CREME96 routines for heavy ion effects.)

The third segment applies TCAD tools like DESSIS (DEvice Simulation for Smart Integrated Systems) from Integrated Systems Engineering (ISE) to deterministically predict the device response to the radiation event. The approach is to build a Geant4 module for generating selected events in simple planar structures that are similar to the structures used to build the device in DESSIS. The energy deposition is computed in detail and the device response is predicted by full 3D mixed mode simulations.

The development of appropriate QDeP technology model will be dynamic feedback from the third segment. The results of the third segment will be used to improve the QDeP models. This will be done manually at first. However, it is obvious that techniques can be developed to automate this procedure for developing more accurate QDeP models.

Full automation and integration of each segment with the others is an area of active research. Integration cannot be completed during this grant's period of performance. However, we will develop an implementation plan for this integration.

Tasks

Task #1. Validation of Geant4 radiation transport model for space applications CMOS

The physical processes modeled by Geant4 are well calibrated against experimental data collected with the interests of developing a better understand of high-energy physics. These models should be applicable to the species and energies of interest when studying radiation effects in microelectronics. However there are certain modeling and particle tracking routines that that must be validated for application to radiation effects in microelectronics.

This past two years we complete the following research:

- We will perform a literature search to uncover published experimental results describing electronic and nuclear interactions of ions in matter that is consistent with space radiation effects on microelectronics
- We will collect certain experimental validation data as needed
- We will perform detailed Geant4 simulations that are consistent with the experiments setups and compare our results to the experimental data
- We will report findings to the Geant4 development team (SLAC and ESA) and support them to improve models were needed

Technical Reports and Presentations:

1. R. A. Reed, R. A. Weller, M. H. Mendenhall, J.-M. Lauenstein, K. M. Warren, J. A. Pellish, R. D. Schrimpf, B. D. Sierawski, L. W. Massengill, P. E. Dodd, M. R. Shaneyfelt, J. A. Felix, J. R. Schwank, N. F. Haddad, R. K. Lawrence, J. H. Bowman, R. Conde, "Impact of Ion Energy and Species on Single Event Effects Analysis," IEEE Trans. Nuc. Sci., vol. 54, no. 6, pp. 2312 - 2321, 2007.
2. J. A. Pellish, R. A. Reed, A. K. Sutton, R. A. Weller, M. A. Carts, P. W. Marshall, C. J. Marshall, R. Krithivasan, J. D. Cressler, M. H. Mendenhall, R. D. Schrimpf, K. M. Warren, B. D. Sierawski, G. F. Niu, "A Generalized SiGe HBT Single-Event Effects Model for On-Orbit Event Rate Calculations," IEEE Trans. Nuc. Sci., vol. 54, no. 6, pp. 2322 - 2329, 2007.

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While not directly funded by NEPP, this work was enabled by the validation and development of our Geant4 application MRED:

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2. K. M. Warren, J. D. Wilkinson, S. Morrison, R. A. Weller, M. E. Porter, B. D. Sierawski, R. A. Reed, M. H. Mendenhall, R. D. Schrimpf, and L. W. Massengill, "Modeling Alpha and Neutron Induced Soft Errors in Static Random Access Memories," in Proc. IEEE International Conference on Integrated Circuit Design and Technology, 2007, pp. 217-220.
3. J. Wilkinson, M. Porter, S. Morrison, R. A. Reed, B. Sierawski, K. Warren, R. Weller, and M. Medenhall, “Ion Microprobe Measurements of Sensitive Volumes in a 0.25μm CMOS Flip-flop”, presented at the 2nd Workshop on System. Effects of Logic Soft Errors, Urbana-Champaign, Ill, April 13-14, 2007.

Task #2. Radiation Effects in Texas Instruments CMOS Devices

The effects of ion-induced charge collection in ultra-scaled CMOS technologies (130 nm and below) can be investigated by combining two research techniques: 1) measurement and modeling of single-event charge liberation via Ion Beam Induced Charge Collection (IBICC) and/or Laser Induced Charge Collection (LICC) on simple structures (e.g., transistors, diodes, inverters) or 2) single event effect measurement and modeling of ring oscillators (RO) fabricated in those advanced technologies. The first method gives a method for a detailed understanding of the basic charge collection mechanisms. The second method will allow for an understanding of the sensitivity of the technology in a real circuit.

This past two years we complete the following research:

- Develop detail radiation transport, device physics, and QDeP models to better understand the dynamics of charge collection and circuit response to radiation.
- Note that IBICC and LICC is funded by DTRA under an MRC agreement

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2. K. M. Warren, R. A. Weller, B. Sierawski, R. A. Reed, M. H. Mendenhall, R. D. Schrimpf, L. W. Massengill, M. Porter, J. Wilkinson, K. A. LaBel, and J. Adams, "Application of RADSAFE to Model Single Event Upset Response of a 0.25 μm CMOS SRAM," IEEE Trans. Nuc. Sci., vol. 54, no. 4, pp. 898 - 903, 2007.
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4. R. A. Reed, G. Vizkelethy, J. A. Pellish, B, Sierawski, K. M. Warren, M. Porter, J. Wilkinson, P. W. Marshall, G. Niu, J. D. Cressler, R. D. Schrimpf, A. Tipton, and R. A. Weller, "Applications of Heavy Ion Microprobe for Single Event Effects Analysis," Nucl. Inst. Meth. B, vol. 261, no. 1-2, 2007, pp. 443-6.
5. A. D. Tipton, J. A. Pellish, R. A. Reed, R. D. Schrimpf, R. A. Weller, M. H. Mendenhall, B. Sierawski, A. K. Sutton, R. M. Diestelhorst, G. Espinel, J. D. Cressler, P. W. Marshall, and G. Vizkelethy, "Multiple-Bit Upset in 130 nm CMOS Technology," IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3259-3264, 2006.
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Task #3. Radiation Effects in SiGe HBTs

VU/ISDE continued to develop a basic understanding of the mechanisms for inducing SEU/SETs in HBTs,. This year we will focused our efforts on full TCAD simulation of the device and circuit response for 5HP and 8HP technologies. We also focused on experimental measurements of current pulse and charge collection.

This past two years we complete the following research:

- Finalize first-order model and test method for IBM 5HP BiCMOS technology
- Begin study to extended first-order model to 7HP and 8HP.
- Use TCAD to predict the angular response of HBT devices to all events at various locations and angles across the entire device and compare this to microbeam results.
- Begin full circuit simulations to model the angle dependence of the broadbeam cross section.
- Microbeam and broadbeam testing support

Technical Reports and Presentations:

[1] M. Varadharajaperumal, G. Niu, X. Wei, T. Zhang, J. D. Cressler, R. A. Reed, P. W. Marshall, "3-D Simulation of SEU Hardening of SiGe HBTs Using Shared Dummy Collector," IEEE Trans. Nuc. Sci., vol. 54, no. 6, pp. 2419 - 2425, 2007.

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Collection in Deep Trench Isolation Technologies," IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3298-3305, 2006.

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Task #4. Sensors

VU/ISDE supported NASA/GSFC's investigation of radiation effects in imagers by performing detail radiation transport simulation using our MRED tool. These results were used to support analysis of transient effects in Si P-I-N diode array (testing performed by AFRL with NEPP/DTRA support)

This past two years we complete the following research:

- Analysis of transient effects in Si P-I-N diode array

Technical Reports and Presentations:

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Task #1: Validation of Geant 4 Radiation Transport Model for Space Applications CMOS – related articles.

Impact of Ion Energy and Species on Single Event Effects Analysis

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***Abstract*—Experimental evidence and Monte-Carlo simulations for several technologies show that accurate SEE response predictions depend on a detailed description of the variability of radiation events (e.g., nuclear reactions), as opposed to the classical single-valued LET parameter. Rate predictions conducted with this simulation framework exhibit excellent agreement with the average observed SEU rate on NASA's MESSENGER mission to Mercury, while a prediction from the traditional IRPP method, which does not include the contribution from ion-ion reactions, falls well below the observed rate. While rate predictions depend on availability of technology information, the approach described here is sufficiently flexible that reasonably accurate results describing the response to irradiation can be obtained even in the absence of detailed information about the device geometry and fabrication process.**

***Index Terms*—Nuclear reactions, single event effects (SEE), single event effect rate.**

I. Introduction

SINGLE event effects (SEE) analysis techniques akin to the rectangular parallelepiped (RPP) model [1] have been shown to provide accurate reliability/survivability estimates for single event upsets (SEUs) in certain technologies, while for other technologies and effects the model has been shown to be inadequate. Specifically, the applicability of linear energy transfer (LET) as an engineering metric has been questioned for many years ([2]–[10] and references within). Until recently, careful analysis of experiments has shown that, for the most part, these concerns could be resolved by modifying the RPP model while maintaining use of the concepts of effective LET and effective SEU cross section (in this paper we make a careful distinction between effective LET and effective cross section, as defined in [1], and the actual ion LET and measured SEU cross section without correction for incident angle).

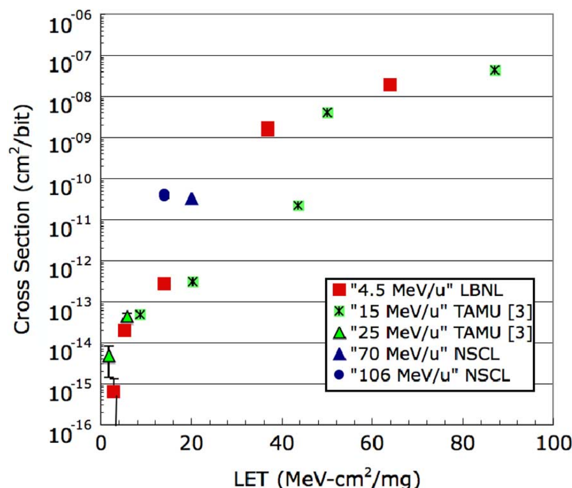

Fig. 1. Measured SEU cross section versus LET of normal incident ions at several different facilities. The data show two orders of magnitude difference at a fixed LET, depending on the ion specie and energy used for testing.

Fig. 1 displays SEU data taken on modern high-reliability, radiation-hardened SRAMs (described in [3]—in this paper we will call this "SRAM#1"). The data were taken at three different facilities, for a range of ion energies, and all ions were normally incident (we will look more closely at these data in the next section). The key point, for now, is the lack of correlation between the measured SEU cross section and ion LET; in particular, notice the large inconsistencies in the data near 14, 20, and 40 MeV-cm^2/mg—note that this is not due to anomalies that result from the concepts of effective LET and SEU cross section. In [4] and [5], Dodd *et al.* presented data showing a poor correlation of effective SEU and single event latchup (SEL) cross sections with effective LET for several SRAMs. It is impossible to use data in which there is a lack of correlation of the SEE cross section with ion LET to make reliable predictions of on-orbit SEU rates using techniques based on integral RPP (IRPP) methods.

In [3] simulations were used to predict the SEU cross section dependence on ion energy and species, as distinguished from

Manuscript received July 20, 2007; revised October 2, 2007. This work was supported in part by the NASA Electronic Parts and Packaging Program and the Defense Threat Reduction Agency Radiation Hardened Microelectronics Program. The portion of this work performed at Sandia was supported by the U.S. Department of Energy. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U.S. Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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Digital Object Identifier 10.1109/TNS.2007.909901

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LET, when nuclear reactions dominate the response. In [6] nuclear reactions were shown to contribute to heavy ion cross sections in commercial memories using low LET C ions. Nuclear reactions have also been considered in evaluating low threshold, low probability upsets in memories as a function of ion energy in [7]. The authors of [8] base their analysis of SEUs in a radiation hardened SRAM on the fact that products from Coulomb scattering events could simultaneously hit two nodes. This SRAM used an SEU mitigation scheme that requires charge collection at more than one node to upset the memory cell. Other studies have questioned the applicability of LET as a ground test metric for SEE because of the difference in the ionized electron structure of the track [9], [10].

There is mounting evidence that ion LET (particularly effective LET) is not an appropriate metric to describe the SEE response of many of today's advanced technologies. We have published several papers [2], [3], [11]–[21] that use a new approach to deal with this issue that is based on a collection of software tools that use physically based models to describe the radiation transport and event generation, and predict the device/circuit response. A key component of this technique is the MRED (Monte Carlo radiative energy deposition) simulation tool. MRED is based on Geant4 [22], which is comprised of the best available computational physics models for the transport of radiation through matter. Geant4 is a library of c++ routines for describing radiation interaction with matter assembled by a large and diverse international collaboration. MRED includes a model for screened Coulomb scattering of ions, tetrahedral geometric objects, a cross section biasing and track weighting technique for variance reduction, and a number of additional features relevant to semiconductor device applications. The Geant4 libraries contain alternative models for many physical processes, which differ in levels of detail and accuracy. Generally, MRED is structured so that all physics relevant for radiation effects applications are available and selectable at run time.

In [2], [3], and [16] it was shown that the SEU cross section could depend on ion energy and species, rather than just LET, when nuclear reactions dominate the response. In [3] we used similar arguments to suggest that the low LET upsets in Fig. 1 (collected at Texas A&M University-TAMU) were due to nuclear reactions. However, these studies lacked experimental data over a range of ion energies and species to confirm the theory. Also, the results of [3] do not address the issue of whether the nuclear reaction contribution significantly impacts the observed on-orbit event rate.

In this paper, new ground and space based experimental results and new MRED simulation results for several technologies show that accurate SEE response predictions depend on a detailed description of the variability of radiation events (e.g., nuclear reactions) as opposed to the classical single-valued LET parameter. The MRED-based event rate prediction method provided in [2] is updated based on these new results. The rate-prediction method is validated by showing excellent agreement with the average observed SEU rate on NASA's Mercury Surface, Space Environment, Geochemistry, and Ranging (MESSENGER) mission to Mercury. In contrast, a prediction based on the traditional IRPP method, which does not include the contribution from ion-ion reactions, falls well below the observed rate.

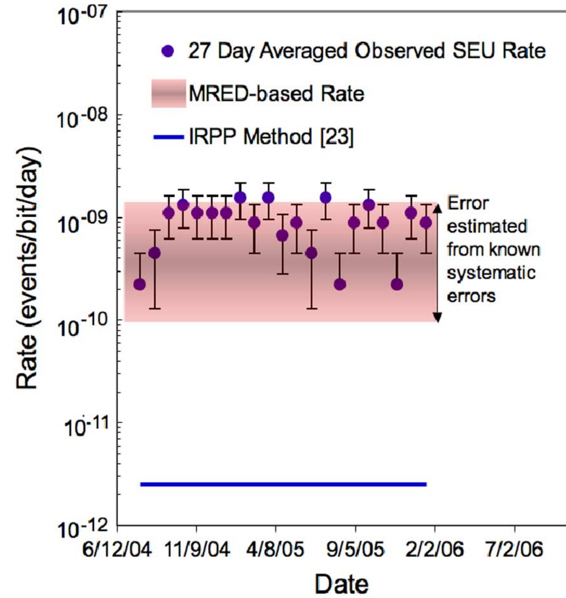

Fig. 2. Comparison of the MRED based event rate predictions for SRAM#1 to measured data on a NASA mission. Also plotted is the predict rate using IRPP [23]. We assumed 100 mils of Al shielding.

II. SEUs in High Critical Charge SRAMs

A. On-Orbit SEU Rates (Observation and Modeling)

NASA's MESSENGER mission uses 40 SRAM#1s; measured on-orbit SEU data for these parts were provided by Johns Hopkins APL. Fig. 2 shows a plot of the 27-day averaged rate for SEUs observed on MESSENGER (the data points are represented by filled circles and one-sigma counting statistics error bars are included). This figure also shows predictions from MRED (including estimated error) and the Integral RPP method [23]. The measured 27-day averaged SEU on-orbit rate is between 2.2×10^{-10} and 1.5×10^{-9} errors/bit/day.

MRED was used to compute the SEU event rate for depositing energy in the sensitive volume for the solar-quiet/solar minimum galactic cosmic ray background (see Section IV for a complete description of the rate prediction method). In [3] we determine the sensitive volume geometry for this SRAM#1 to be $2 \times 2 \times .25\ \mu\mathrm{m}^3$. The surrounding material in the simulations is consistent with the overlayers used to fabricate the SRAM (Fig. 3). The environment was predicted using the models on the CREME96 website [24]. Computations from MRED predict an event rate between 8.6×10^{-11} and 8.6×10^{-9} errors/bit/day. The upper and lower values were determined from the fit of the MRED results to data in Fig. 1 (see Section II-C), and are a result of the systematic uncertainty in Geant4 nuclear physics (see the Appendix) and the limited description of the sensitive volume and the overlayers.

The MRED prediction of the SEU rate is in excellent agreement with the average observed rate on MESSENGER. However, using the traditional IRPP approach for rate prediction yields a rate of 2.5×10^{-12} errors/bit/day, a factor of 88 to 618 lower than the rate observed on MESSENGER.

LET is defined as the mean energy lost by an ion per unit path length in collisions with electrons of the material, and is

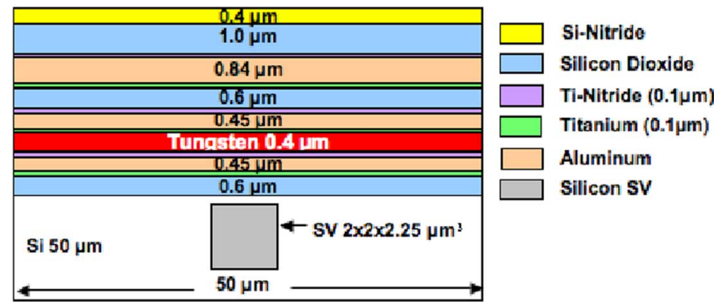

Fig. 3. Sensitive volume and overlayer used for MRED simulation of SRAM#1. The volume thickness is 2.25 μm. The sensitive volume geometry was determined in [3] using TCAD. While MRED events can be coupled directly to TCAD [15], [18], the simulation approach used in this work was to tabulate energy deposited the sensitive volume.

TABLE I
IONS USED FOR TESTING SRAM#1

Test Facility	Species-Atomic Mass	Energy (MeV)	LET (MeV-cm^2/mg)	Computation Method
LBNL	N-15	68	2.9	Full
LBNL	Ne-20	90	5.3	Full
LBNL	Ar-40	180	14	Full
LBNL	Kr-86	387	37	Full
LBNL	Xe-136	612	64	No Nuclear Reactions
TAMU	Ne-22*	523	1.8	Full
TAMU	Ar-40*	494	8.7	Full
TAMU	Ar-40*	919	5.8	Full
TAMU	Ag-109*	1200	44	No Nuclear Reactions
TAMU	Au-197*	2000	87	No Nuclear Reactions
TAMU	Cu-63*	729	20	Full
TAMU	Ag-109*	665	50	No Nuclear Reactions
NSCL	Xe-136	14416	14	None
NSCL	Xe-136	9520	20	None

* From [3]

a good quantity to characterize the energy available to produce ionization (free charge). Ionization from the primary particle is called direct ionization. Indirect ionization, induced by secondary particles from ion-ion reactions, can result in large amounts of localized energy deposited near SEE sensitive structures.

The SEU rate includes contributions from three interaction processes between the ion and the target semiconductor: 1) direct ionization induced by the primary ions, 2) indirect ionization via atomic displacements caused by Coulomb scattering between target atoms and the incident ion, and 3) indirect ionization from nuclear reaction products involving the incident ion and the target nucleus. The relative contribution of each mechanism to the overall rate depends on the number of sensitive volumes, cell critical charge, amount and location of high-Z materials, and the ion species, energy, and fluence used in the testing [2], [3], [17], [19].

To compute an event rate for the environment considered here, MRED fully simulates each of the processes defined above for an ensemble of omnidirectionally incident primary particles, applies the appropriate interaction cross sections, and records the energy loss of the primary particle and all secondary particles within a defined box (called the sensitive volume).

The traditional rate-estimation methods, like IRPP, do not include the variability of radiation events (e.g., nuclear reactions). Instead they approximate the direct ionization by assuming a single (often constant) value for the LET parameter. These older models do not include energy deposition from indirect ionization events. The MRED-calculated rate is in much better agreement with the observed on-orbit rate than that predicted by the classical method.

B. SEUs at Heavy Ion Accelerator Facilities

New SEU cross section data were collected on two radiation hardened SRAMs (called SRAM#1 and SRAM#2) at two SEE test facilities: Lawrence Berkeley National Laboratory (LNBL), and the National Superconducting Cyclotron Laboratory (NSCL). The ions used are listed in Table I. The ion energy and associated LET are also listed in Table I. Fig. 1 compares these data taken on SRAM#1 to the data given in [3]. (The details of the test setup are identical to those described in [3]). Error bars representing two standard deviations (98% confidence interval) are included; the symbols hide the error bars for the cases where they cannot be seen.

The intent of this testing was to determine the dependence of the measured SEU cross section on incident ion energy and species for normally incident ions. As stated in the introduction, the inconsistencies at several values of LET clearly show that direct ionization from the primary particle (or LET) cannot be used to describe the trends in the data completely. For example, comparing the measured cross section for ions that have a LET of 14 MeV $\cdot$ cm^2/mg, we see that the cross section using the 14.4 GeV Xe ions at NSCL (filled circle) is two orders of magnitude higher than that measured with the 180 MeV Ar ions

at LBNL (filled square), although both particles have the same LET. The high atomic mass ($\boldsymbol{A}$), high-energy ion produces a higher SEU cross section than the low $\boldsymbol{A}$, low-energy ion. The same can be said for ions with LETs of 20 MeV $\cdot$ cm^2/mg (9.25 GeV Xe ions and the 729 MeV Cu ions). However, comparing data near an LET of 40 MeV-cm^2/mg shows that using the low $\boldsymbol{A}$, low-energy ion produced a higher SEU cross section than that with the high $\boldsymbol{A}$, high-energy ion. Notice that the inconsistencies in the data disappear at high LET and at low LET. There appears to be no simple predictable trend with ion LET (even ionization track radius), species, and/or ion energy!

Finally, we note that at high LET values, where the cross section is near 4×10^{-8}cm^2, direct ionization dominates the response. At these LET values, the LBNL and TAMU results agree and are consistent with the expected sensitive volume geometry as measured by laser testing and as determined via TCAD [3]. We also note that [25] provides data that show that the dosimetry at NSCL is consistent with other radiation effects test facilities, so the trends in the data are physically meaningful and not artifacts induced by facility differences.

Similar trends in the measured cross section were observed for SRAM#2 using ions that have an LET of 14 MeV-cm^2/mg. The measured cross section at 14.4 GeV Xe ions at NSCL is 1.4×10^{-11}cm^2/bit. The measured value (1.4×10^{-13}cm^2/bit) for the 180 MeV Ar ions at LBNL is two orders of magnitude lower than that measured at NSCL. Again, the high $\boldsymbol{A}$, high-energy ion produces a higher SEU cross section than the low $\boldsymbol{A}$, low-energy ion.

In the next section, we show that accurate SEE response predictions depend on a detailed description of the variability of radiation events (e.g., nuclear reactions), as opposed to the classical single-valued LET parameter, in order to explain the data in Fig. 1. MRED, which includes high fidelity physics models for all physical processes, is used for the cross section calculations.

C. Discussion and Hardness Assurance Issues

To model the ground test environment, MRED fully simulates each of the processes defined in Section II-A for an ensemble of unidirectionally incident primary particles, applies the appropriate interaction cross sections, and records the energy loss of the primary particle and all secondary particles within the sensitive volume (Fig. 3). The cross section for depositing a specific energy, $\boldsymbol{E}$, or greater is computed [2], [3]. These results are used to determine the SEU cross section by defining a critical charge (equivalently a critical energy) for upset. Conversely, if the measured SEU cross section is known, the critical energy (or critical charge) can be determined. In [3] we TCAD simulation to define ademonstrated the use of MRED to determine the contribution of various energy deposition processes to the SEU cross section.

The MRED simulation tool was used to simulate the twelve lowest energy ions listed in Table I. Current limitations within Geant4 (Geant4.8.1.p02) prevent the simulation of nuclear reactions for ions with a large atomic mass ($> \boldsymbol{Z} = 36$) [2]; therefore, the two ions used at NSCL were not simulated. Fig. 4 shows the measured SEU cross section (data from Fig. 1) for each ion (open circles). The measured data contain error bars

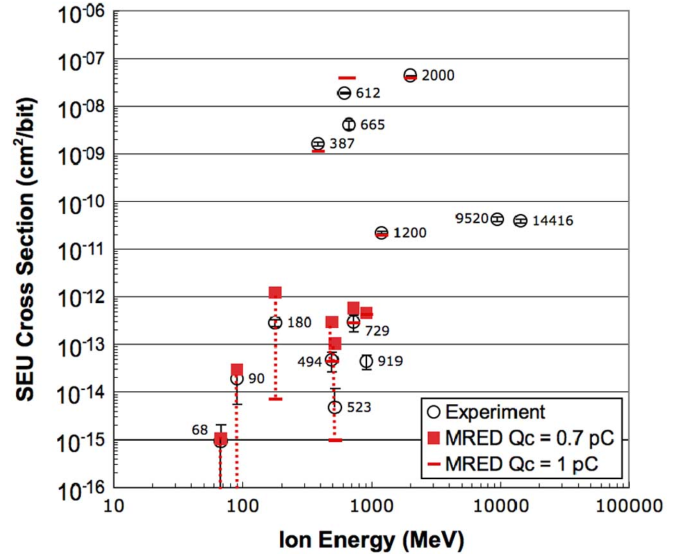

Fig. 4. Comparison of ground test results to MRED predictions for SRAM#1. These values for Q_c are used to predict the event rate presented in Fig. 1. Table I can be used to identify the ion species using the energy labels in this figure.

that represent a 95% confidence interval. The figure also shows the fit of MRED results to the measured SEU cross section data (fitting is described in the next few paragraphs). The abscissa is the total ion energy. Each data point is also labeled by the ion energy, which can be used to identify the ion species using Table I. MRED simulations are in good agreement with measured data.

Simulation results can be separated into two categories: SEUs induced by direct ionization and those induced by indirect ionization. The systematic errors described in the Appendix require that each category must be analyzed separately. Geant4 is much more accurate at predicting effects from direct ionization than those from indirect ionization. We determined that the simulation results are dominated by direct ionization effects for the Ar(387 MeV), Kr(665 MeV), Xe(612 MeV), Au(2 GeV), and Ag(1.2 GeV) ions. Indirect ionization effects dominate for all other ions.

The experimental data presented in Fig. 4 were used to determine the best value for critical charge. The value for the critical charge for direct ionization events was determined to be 1.02 pC (or 23 MeV), while for indirect ionization the fit to the data resulted in a range from 0.7 to 1.02 pC. This is not a surprising result given that a simple structure was assumed for the sensitive volume (Fig. 3) and that there are known systematic errors in Geant4 (see the Appendix).

We conclude that accurate SEE response predictions depend on a detailed description of the variability of radiation events (i.e., all applicable interaction physics must be used) to describe the data in Fig. 1 fully. We also conclude that tests over energy and species similar to that given in Table I, excluding the high-energy ions at NSLC, are sufficient to provide estimates for error rates. However, the testing at NSCL allowed us to conclude, with certainty, that LET is not the appropriate metric when studying single event upsets in these technologies. Further hardness assurance issues are discussed in [5].

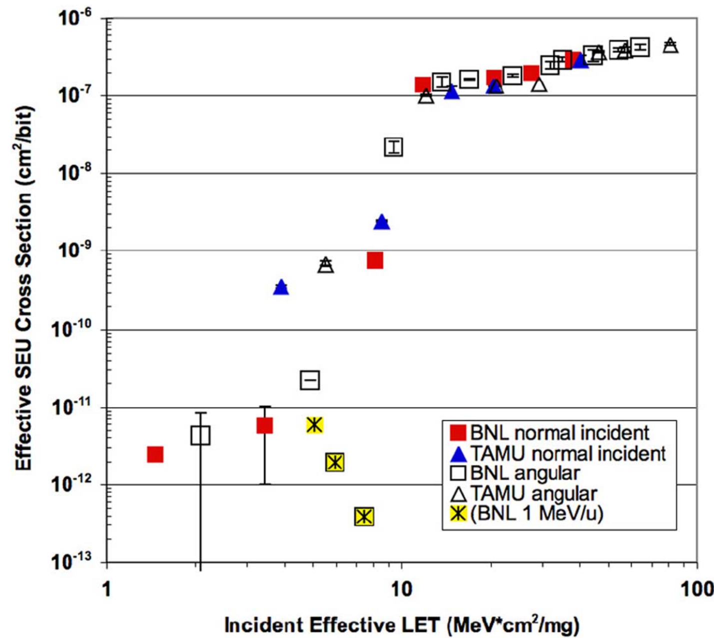

Fig. 5. Measured SEU cross section versus LET of normal and angularly incident ions on SRAM#3 (reproduced from [5]). At LETs less than 10 MeV-cm^2/mg, cross sections become very dependent on ion species and energy; note that at very low energy, cross section decreases with increasing angle.

TABLE II
IONS USED FOR TESTING SRAM#3 (FROM [5])

Test Facility	Species-Atomic Mass	Energy (MeV)	LET (MeV-cm^2/mg)	Angles Tested	Computation Method
BNL	C-12	12	1.464	0, 30, 45	Full
BNL	C-12	98.7	5.07	0, 45	Full
BNL	F-19	141	3.428	0, 45	Full
BNL	Si-28	185	8.126	0, 30	Full
BNL	Ti-48	193.8	11.81	0, 30	Full
BNL	Cl-35	210	20.54	0, 30, 45	Full
BNL	Ni-58	265	27.49	0, 30	Full
BNL	Br-81	279	38.24	0, 30, 45	Full
TAMU	Ar-40	509	8.55	0, 45	Full
TAMU	Ar-40	1560	3.9	0, 45	Full
TAMU	Kr-84	1879	20.4	0, 45	Full
TAMU	Kr-40	2981	14.7	0, 45	Full
TAMU	Xe-136	2835	40.2	0, 30, 45	No Nuclear Reactions

III. SEUs IN LOW CRITICAL CHARGE SRAMs

A. *Experimentally Measured Cross Section*

In SRAMs with low critical charge, we expect a reduced role of indirect ionization relative to direct ionization in causing single-event upsets [2], [3]. Examination of test data from [5] for a block of a 0.5-μm bulk 256-kbit SRAM without feedback resistors (hereafter referred to as SRAM#3) reveals that the measured SEU cross section for a fixed LET depends on ion energy and species, despite this block having a low critical charge for upset (Fig. 5). Details of the SRAM process and test methods are given in [26] and [5], respectively.

SEU tests on SRAM#3 were conducted at Brookhaven National Laboratory (BNL) and TAMU. Table II lists the ions used, their energies, and effective LETs. It is not the intent here to discuss these results in detail; this discussion can be found in [5]. The key point is that once again, there is no simple relationship between SEU cross section and ion LET.

B. *Simulation of the SRAM#3 Measured SEU Cross Section*

MRED was used to predict energy deposition distributions in a carefully selected sensitive volume for all ions listed in Table II. The method defined in [12] was used to develop the sensitive volume, which is to construct a concentric set of charge collection regions with different collection efficiencies by assuming a threshold LET of 7.5 MeV-cm^2/mg for upsets induced by direct ionization. The normally incident BNL data in Fig. 5 for this LET and higher were used to construct a set of ten weighted, concentrically nested sensitive regions; the aggregate of these regions defines the sensitive volume. Following the method detailed in [12], cross sections at each of ten logarithmically uniform points along the upset curve from 7.5 to 38 MeV-cm^2/mg were used to define the areas of the sensitive volumes. All of these regions have depths of 2 μm. Charge collection efficiencies were assigned per [12] such that all efficiencies summed to 100% in the center region where the ten volumes overlap. No assumptions were made as to the composition of the

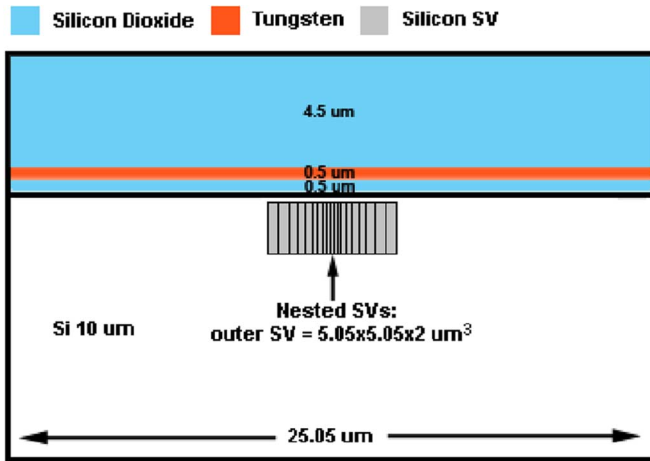

Fig. 6. Sensitive volumes and overlayers used for simulation of SRAM#3.

overlayers; the tungsten vias were modeled as a 0.5 μm layer placed 0.5 μm above the base of a 5.5 μm silicon-dioxide overlayer (Fig. 6). This simulation configuration was done without any process, circuit or device information.

Simulation results fitted to measured data are shown in Fig. 7 for incident ions normal to the die surface. Non-zero upset cross sections for C(98.7 MeV), F(141 MeV), and Ar(1560 MeV) are due to indirect ionization effects. MRED revealed that C(12 MeV), Si(185 MeV) and Ar(509 MeV) ions are in the threshold region [3] for causing upset due to direct ionization, with indirect ionization from Coulomb scattering potentially contributing to the cross section as well. Direct ionization effects dominate for all other ions. Using the fitting method described earlier, the critical charge for direct ionization events was determined to be 0.133 pC (or 3 MeV). As can be seen for the C(98.7 MeV) and F(141 MeV) ions, this critical charge fits these low-energy, nuclear-reaction-dominated simulations to the experimental data very well. Incorporation of a fitting range of 0.121 to 0.163 pC improved the fit, bringing the simulations into agreement with experiment for the C(12 MeV) and Ar(509 MeV) simulated ions. Note that the high energy Ar(1560 MeV) cross section remains fixed across this range of critical charge, and is due only to indirectly ionizing effects; the present limitations of Geant4 (see Appendix) prevent an accurate fit to the measured cross section for this high energy ion.

Using the upper and lower limits for critical charge, determined by fitting the normally incident-ion data, MRED simulations reproduce the angle dependence for the SEU response without any adjustable parameters. Simulation and experimental results for 30° (not shown) and 45° (Fig. 8) angles of incidence are in excellent agreement with measurement. Unlike in Fig. 5, measured data are shown without standard corrections to the fluence for off-normal angles imposed by the RPP method, i.e., the SEU cross sections are not effective cross sections. At both 30° and 45° angles, C(12 MeV) has a diminished measured cross section as compared with 90° incidence. MRED simulated this trend, predicting no upsets at off-normal angles of incidence for the above critical charges. This underprediction could be due to the very simplified geometry and the chosen sensitive volume depth.

We note that this analysis was done without detailed information about the circuit, device geometry and process. The quality and accuracy of these predictions are directly related to the details of device and circuit structure that are available. However, as the results reported here demonstrate, even relatively crude approximations are often sufficient to produce reasonably accurate simulations that describe responses to irradiation. By including detailed descriptions of all physical processes it has been possible to capture the complex cross section curve of Fig. 5, and to establish a self-consistent data set whose details are explicable in terms of the interaction mechanisms linking the incident ion and the target device.

IV. SEE Rate Prediction Methodology

In the previous sections we have shown that the variability of radiation events arising from the intrinsic randomness of the physical processes through which radiation interacts with matter now dominate single event effects in multiple technologies. In this section, we show how this variability may be quantified and used to predict the rate of single event effects in devices. The key strategy is Monte Carlo simulation to compute energy depositions in define sensitive volumes.

A Monte Carlo simulation program, such as MRED, may be viewed as a machine for determining a probability distribution by repetitive sampling. It is particularly useful when direct analytical computation of the distribution is difficult or impossible. For example, one might pose the question: "What is the probability density for an isotropic, mono-energetic flux of ions with atomic number $\boldsymbol{Z}$ and energy $\boldsymbol{E}_0$ to deposit energy $\boldsymbol{E}$ in a specific sensitive volume?" To answer this, MRED computes the energy deposited by a large number of ions with randomly chosen initial trajectories, produces a histogram of the resulting values, normalizes the histogram to unit area, and scales by the width of the histogram bins, to obtain a discrete approximation to a continuous probability density. Subsequently, we will represent this continuous probability density as $\mathrm{MRED}_z(E_0, E)$.

In order to understand the full Monte Carlo solution for an event rate in the space environment, one must first understand how the function $\mathrm{MRED}_z(E_0, E)$ would be used in an analytic computation to infer the event rate from a knowledge of the flux distribution of the various ions. Let $\Phi_z(E_0)$ be the flux of ions with atomic number $\boldsymbol{Z}$ and energy $\boldsymbol{E}_0$, in units, e.g., of particles/cm^2/second/ sterradian/MeV. For our computations, these values were obtained from CREME96 by appropriate scaling of the original distributions, which are normalized to energy per nucleon. In the simplest computation, one would integrate the product of $\boldsymbol{\Phi}$ and $\mathrm{MRED}_z(E_0, E)$ over all energies and scale appropriately by the sample area. However, this presents a challenge for a Monte Carlo computation, due to the very large dynamic range of the flux, $\boldsymbol{\Phi}$. To deal with this, it is useful to define a new integration variable $\boldsymbol{r}$ that may be thought of as a random number generated in the usual way in the interval [0], [1]. A function $E_0(r)$ is chosen that maps each $\boldsymbol{r}$ into an ion energy $\boldsymbol{E}_0$ in a way that distributes randomly selected energy values to give good sampling statistics in all regions of the flux distribution. In this way, very rare, high-energy ions are simulated as frequently as much more numerous low-energy ions. For this work we chose $E_0(r) = E_{\min}(E_{\max}/E_{\min})^r$, where $[E_{\min}, E_{\max}]$ is the range of CREME96 flux data used. The upper limiting ion energy was chosen to be 20 GeV/nucleon after tests demonstrated that energies above 20 GeV/nucleon did not contribute significantly to

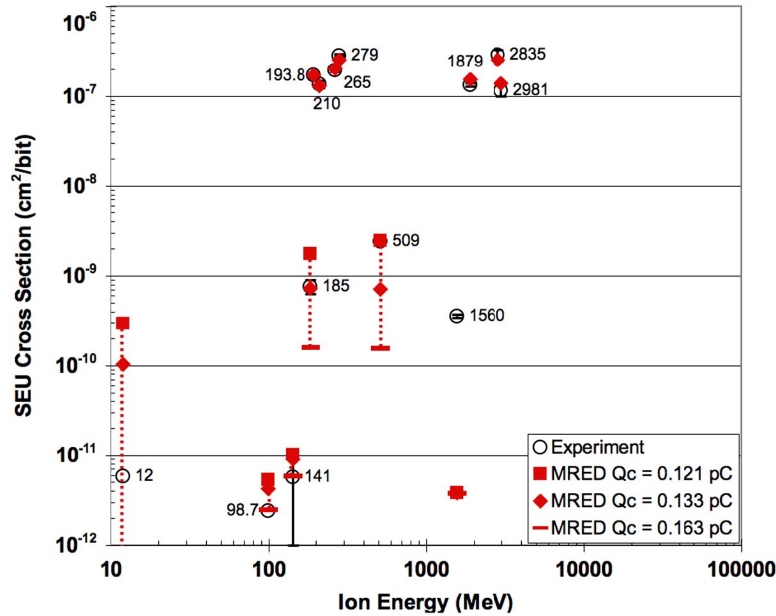

Fig. 7. Comparison of ground test results to MRED predictions for normally incident ions. These values for Q_c are used to predict the angle dependence in shown in Fig. 8. Table II can be used to identify the ion species using the energy labels in this figure.

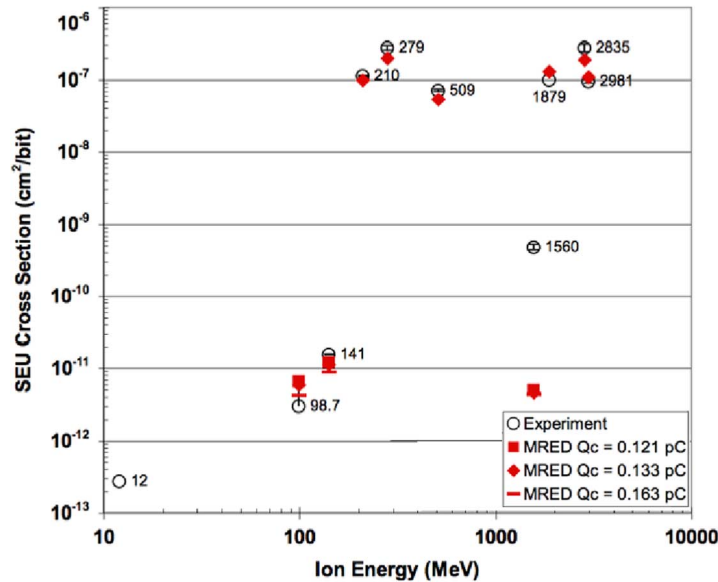

Fig. 8. Comparison show very good agreement between ground test results and MRED predictions for ions incident at tilt $= 45^\circ$. The angle of incident was the only simulation parameter that was changed.

final results. The inverse derivative $n(E_0) \equiv dr/dE_0$ may be thought of as the density of samples at energy E_0 and is uniform on a log scale between $E_{\min}$ and $E_{\max}$ for the particular $E_o(r)$ defined above. This results in a full equation for the differential event rate of

$$\frac{dR(E)}{dE} = \sum_{z=1}^{92} \left(4\pi^2\rho^2 \int_0^1 dr \left(\frac{\Phi_z(E_o(r))}{n(E_o(r))} \right) \cdot \mathrm{MRED}_z(E_o(r), E) \right). \quad (1)$$

Here $\pi\rho^2$ is the sample area and a factor of 4 π sterradians is included because $\mathbf{\Phi}$ is isotropic and normalized to solid angle. The sum is carried out over all species in the space environment for which CREME96 has data.

Examining (1) it is clear that the $\boldsymbol{r}$ integral can also be evaluated by other numerical techniques. As described above, the set of $\boldsymbol{r}$ values used to evaluate the integral consists of random points that are statistically uniform in the interval [0], [1]. Alternatively, these values may be deterministically uniform. If $\boldsymbol{r}$ values are chosen in this way, the difference is simply the dif-

ference in integrating by the trapezoid rule or by Monte Carlo integration, and (1) can be recast as follows:

$$\frac{dR(E)}{dE} = \sum_{z=1}^{92}\left(\frac{4\pi^2\rho^2}{N_z}\sum_{i=1}^{N_z}\left(\frac{\Phi_z(E_o(r_i))}{n(E_o(r_i))}\right)\cdot \mathrm{MRED}_z(E_o(r_i),E)\right) \quad (2)$$

where

$$r_i = \frac{2i+1}{2N_z} \approx \frac{i}{N_z}, i = 0,\ldots,N_z-1. \quad (3)$$

It is evident in (2) that the number of points chosen to evaluate the sum over $\boldsymbol{i}$ can be different for each ion species in the environment, where species is indexed by atomic number $\boldsymbol{Z}$. In order to maximize the efficiency of the numerical computation, it is desirable to select a smaller $\boldsymbol{N}_z$ when the species $\boldsymbol{Z}$ is a minor constituent of the space environment, or more precisely, is a smaller contributor to the effect being computed. In practice, this is done by establishing a heuristic selection probably $\boldsymbol{p}_z$ for each species in the environment. A simulation involving the tracking of $\boldsymbol{N}$ total incident ions is then conducted in this way

$$\frac{dR(E)}{dE} = \frac{4\pi^2\rho^2}{N}\sum_{z=1}^{92}\sum_{i=1}^{p_zN}\left(\frac{\Phi_z(E_o(r_i))}{p_z\cdot n(E_o(r_i))}\right)\cdot \mathrm{MRED}_z(E_o(r_i),E). \quad (4)$$

The selection of $\boldsymbol{r}_i$ may be deterministic according to (3) or a uniform random number in the interval [0], [1]. Since the quantity $N_z \approx p_zN$ is not guaranteed to be an integer, it must be rounded. This is done probabilistically so that it is possible to distribute the computation of (4) across a large number of independent processors.

The total rate of events that deposit energy greater than $\boldsymbol{E}_d$ is related to the differential rate by

$$R(E_d) = \int_{E_d}^{\infty} dE\frac{dR(E)}{dE}. \quad (5)$$

In practical calculations, between ten and 300 independent instances of (4) are computed in parallel, with each instance having an $\boldsymbol{N}$ value of order 10^7. Individual events are given initial weights of $\Phi_z(E_o(r_i))/(p_z\cdot n(E_o(r_i)))$. The heuristic selection probability $\boldsymbol{p}_z$ is often taken to be the fifth root of the relative total abundance of the ion $\boldsymbol{Z}$ in the space environment.

To further increase the quality of the data for nuclear reaction events, all nuclear reaction cross sections are artificially increased by a factor $\boldsymbol{\eta}$, which is typically chosen to be $\approx$200. If the primary ion in an event produces a nuclear reaction, the total weight of the event is reduced by a factor of $\boldsymbol{\eta}$ from its initial value given above. As long as the use of the $\boldsymbol{\eta}$ factor does not materially alter (by $< 5\%$ as our typical criteria) the number of events that *do not* experience nuclear reactions, the only effect on the final distribution is to reduce the variance in the region of rare, large-energy-deposition, nuclear-reaction events.

MRED typically uses the Geant4 binary intra-nuclear collision cascade to determine the final state for ion-ion nuclear reactions. Alternatively, the Bertini model may be, and is often, used for comparison purposes. The binary cascade code has been validated by the Geant4 collaboration for ions up to atomic number $\boldsymbol{Z} = 6$. Beyond this, its use is more speculative, although data have been presented by the code developers that suggest that it may be used with caution up to at least $\boldsymbol{Z} = 26$ (Fe) [27]. The magnitude of the effects we observe are dependent upon the details of this model, and will become less uncertain from systematic error as on-going efforts to improve the underlying physics are completed. However, the rates of nuclear reaction events depend on reaction cross sections, which are less uncertain than final state configurations. Therefore, while the quantitative results may improve with time, the qualitative conclusions are not likely to change. In any event, the mass, direction and energy of heavy nuclear reaction fragments are critical to single event computations and achieving statistical accuracy in predicting these quantities is critical for performing accurate rate calculations.

V. Conclusion

Primary ion LET is not sufficient to describe the observed trends in measured SEU cross section data for modern technologies. Experimental results on three SRAMs show multiple values for the SEU cross section when irradiated with particles that have the same LET but different mass and energy. MRED-based simulations provide insight by showing that one must include a detailed description of the variability of radiation events (e.g., nuclear reactions), as opposed to the classical single valued LET parameter, in order to develop a well-behaved description of the SEE response. This is true for most circuits; the contribution of reaction products to the event rate in the space radiation environment can dominate the response in certain cases or can be overwhelmed by the direct ionization contribution in others, depending on the sensitivity of the circuit to transient radiation events.

MRED-based predictions were shown to be in excellent agreement with the average observed SEU rate on NASA's MESSENGER mission to Mercury. A prediction from the traditional rate-prediction method (IRPP), which does not include the contribution from ion-ion reactions, underestimates the observed rate by two orders of magnitude. Ion-ion nuclear reactions have a significant impact on the observed event rate for circuits with high critical charge. This is most important for circuits that contain high-Z materials near sensitive structures. The quality and accuracy of predictions are directly related to the details of device and circuit structure that are available. However, as the results reported here demonstrate, even relatively crude approximations are often sufficient to produce reasonably accurate simulations that describe responses to irradiation.

In [2], we provided a recommendation on ion species and energy selection when large inconsistencies occurred in the measured cross section at a single LET value. The current work shows that tests over energy and species similar to that given in Table I, i.e., ion beams less than 40 MeV/u, are sufficient to provide estimates for error rates. However, the testing at the higher energies, e.g., 100 MeV/u, allowed us to conclude that indirect ionization contributes significantly to the error cross section.

Ion energy and species, as opposed to a single-value for the ion LET, is the key metric for assessing the SEU susceptibility

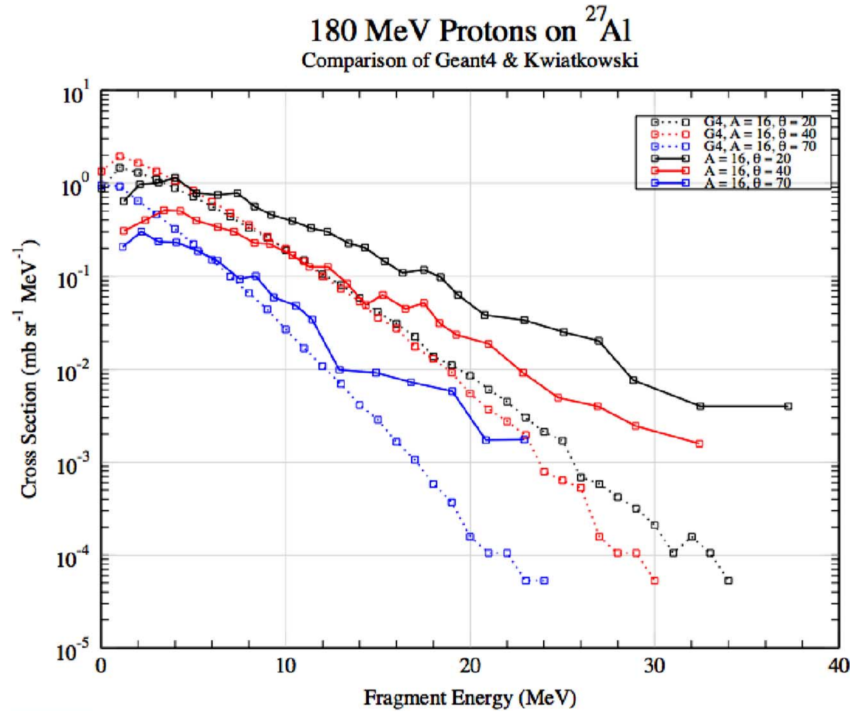

Fig. 9. Comparison of Geant4 and experimental results from [22] for 180 MeV protons on aluminum. Geant4 dramatically underestimates the fragment energy.

of certain modern technologies. Reaction products from ion-ion interactions are a key basic mechanism when studying SEUs. While the potential of these trends to increase SEU event rates is important, the implications are potentially catastrophic for hard failures like SEL or soft errors that have significant impact at the system level, e.g., single event functional interrupts.

Appendix
Systematic Uncertainty in Geant4 Nuclear Physics

One of the critical issues in understanding SEUs is the correct determination of the energy deposited by the fragmentation of heavy nuclei as a result of nuclear reactions. These reactions are particularly important in two regimes. The first regime is operation in a low LET light-ion background. Protons above 10 MeV have almost negligible direct energy deposition, but create many reactions. The other regime is heavy-ion reactions in which cosmic ray nuclei such as iron react with species in the target. These reactions can deposit many 10s of MeV in a small volume of an integrated circuit, resulting in upsets in even extremely hard circuits.

The underlying physics in each of these regimes is quite different, and not very well characterized in either case. However, some data are available for the fragmentation of nuclei by protons. Although nuclear physics in the relevant energy range for protons (10 MeV and higher) has been extensively studied, very few experiments have been carried out that contain the detailed information needed to understand energy deposition in semiconductors. Most nuclear physics experiments have looked at total reaction cross sections, and simple few-nucleon reactions. However, the light fragments of a nuclear reaction have very low LET. The protons, deuterons, and alpha particles emitted deposit energy very diffusely, and so spread a small amount of energy over many semiconductor devices, resulting in a low probability of an upset. One the other hand, when a nucleus breaks up leaving high-energy heavy fragments, these can deposit all their energy in a small volume, upsetting a circuit.

Triply differential cross sections, measured by fragment energy, fragment mass, and fragment angle, are the minimal requirement to understand how these reactions deposit energy in semiconductors. An experiment [28] using 173 MeV protons on an aluminum target produced data of the quality needed for use in simulations. The experimental results for oxygen residual nuclei are compared to nuclear fragmentation models currently available through Geant4 in Fig. 9; Geant4 results are plotted using open symbols connected by dashed lines and the experimental data are open symbols connect by solid lines. Similar results were obtained for other residual nuclei.

The results of this comparison are disappointing. Current breakup models predict heavy fragment production with significantly lower energy than was observed in this experiment. The distribution of the energies of fragments is roughly exponential with energy, so a small error in the scale energy can result in a spectacular underproduction of the highest energy fragments. Comparison to data in [28] shows that, for protons on aluminum, the scale energy is 30%–40% too low. This results in an under-production of more than an order of magnitude of the most energetic fragments, which results in under-prediction of the energy deposited.

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A Generalized SiGe HBT Single-Event Effects Model for On-Orbit Event Rate Calculations

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***Abstract*—This work draws on experimental and simulation results to derive a generalized SEU response model for bulk SiGe HBTs. The model was validated using published heavy ion and new proton data gathered from high-speed HBT digital logic integrated circuits fabricated in the IBM 5AM SiGe BiCMOS process. Calibrating to heavy ion data was sufficient to reproduce the proton data without further adjustment. The validated model is used to calculate upset event rates for low-earth and geosynchronous orbits under typical conditions.**

***Index Terms*—Deep trench isolation, Geant4, geosynchronous orbit, low-earth orbit, rate prediction, silicon-germanium HBT, single-event upset.**

I. Introduction

A. Overview

SILICON-GERMANIUM heterojunction bipolar transistor (SiGe HBT) technology, due to its inherent total ionizing dose (TID) tolerance [1]–[3], high-speed capability [4]–[8], superior low-temperature performance [6], [10], and seamless integration with deep sub-micrometer CMOS makes it a suitable candidate for space-based applications.

However, despite these appealing characteristics, heavy ion tests on GHz-speed current mode logic (CML) master–slave D flip-flop (DFF) shift registers, fabricated in several generations of SiGe HBTs, showed single-event upset (SEU) thresholds below linear energy transfers (LET) of 2 MeV $\cdot$ cm^2/mg and saturated cross sections above 200 μm^2 for single shift register stages [4]–[9]. Significant SEU susceptibility has always been an issue when considering SiGe HBT or SiGe BiCMOS applications, but the issue can be managed if the likely SEU event rates for planned mission environments are known. This work describes the development of a generalized energy deposition SEU response model for SiGe HBTs that can be used to calculate event rates for various well-defined environments. The response model was designed for use with our simulation framework [10]–[14], which includes the Monte Carlo radiative energy deposition (MRED) tool [10]–[12], [15], [16].

The generalized model developed in this work was applied to two different DFF shift register designs fabricated in the IBM 5AM SiGe BiCMOS (IBM 5AM) process: a baseline design and a radiation hardened by design (RHBD) variant. This process is characterized by a 0.5 μm drawn emitter width, a unity-gain cutoff frequency of 50 GHz, and a BV_{CB0} of 3.3 V [1], [17].

Of the two IBM 5AM designs considered here, one was a baseline, nominal switching current, DFF shift register design [7] and the other employed a RHBD dual-interleaving technique that included duplicated pass and storage cells, which effectively decoupled the differential inputs and outputs in the storage cell [7], [18]. This input/output decoupling increased the critical charge (Q_{crit}) of this design. For the sake of simplicity, these designs are referred to as "baseline design" and "RHBD design" throughout. Both shift register designs are 127-bits long and were fabricated solely out of IBM 5AM SiGe HBTs; no complementary metal–oxide–semiconductor (CMOS) transistors were used.

B. Context and Motivation

It is important to understand the basic physical structure of a typical bulk SiGe HBT since the single-event response is driven mostly by structural processing geometry [19]. A technology computer-aided design (TCAD) cross section of the IBM 5AM process is shown in Fig. 1. Three features dominate single-event charge collection: the deep trench isolation (DTI), the lightly doped substrate, and the large area of the reverse-biased subcollector junction that is a minimum of approximately 10 μm^2.

Microbeam data sets [19]–[25] of several different bulk SiGe HBT process generations have shown that individual devices exhibit significant charge collection from lateral distances on the order of 10 μm and significant vertical collection to depths of approximately 15 μm under the active region of the device.

Manuscript received July 20, 2007; revised September 13, 2007 and October 4, 2007. This work was supported in part by the NASA Electronic Parts and Packaging Program and the Defense Threat Reduction Agency Radiation Hardened Microelectronics Program under IACRO #07-4201i to NASA, as well as the Georgia Electronic Design Center at the Georgia Institute of Technology.

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Digital Object Identifier 10.1109/TNS.2007.909987

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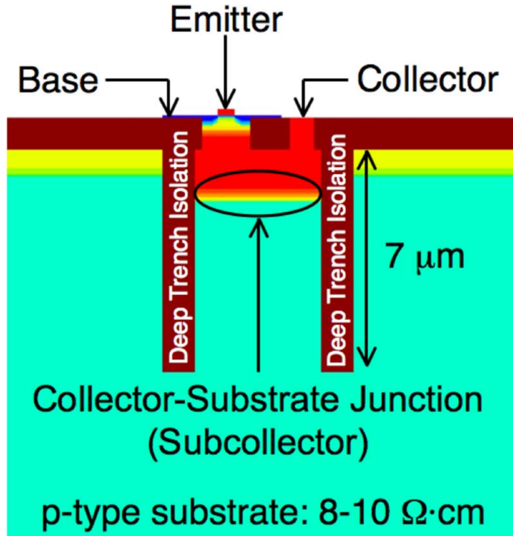


Fig. 1. TCAD cross section of the IBM 5AM SiGe HBT. Single-event charge collection is driven by the lightly doped substrate that allows for long minority carrier lifetimes and the large area of the subcollector junction. For a minimum-sized device, this junction is has an area of approximately 10 μm^2.

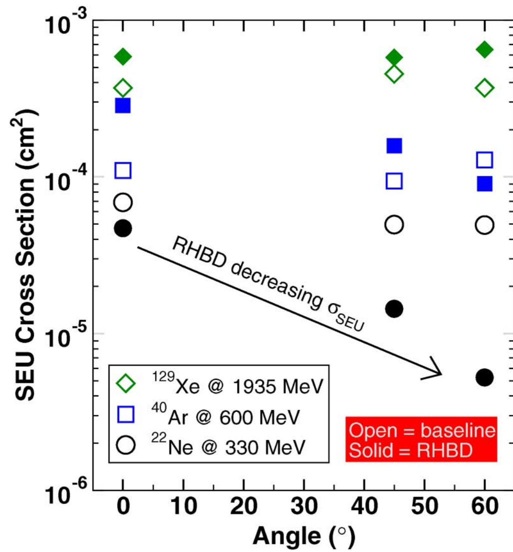


Fig. 2. Broadbeam heavy ion data for the baseline and RHBD 127-stage shift register designs after [7]. The important feature is the cross section decrease with increasing angle for the RHBD device with a higher critical charge. This roll-off behavior violates RPP model assumptions, so all RPP cosine corrections have been removed. The data are plotted with respect to angle and the cross section was scaled by $\cos(\theta)$ to remove the effective fluence correction.

These lateral and vertical charge collection distances are governed by the lightly doped substrate and the 3–5 V dropped across the subcollector space charge region (SCR). While the microbeam data sets provide unique insight into charge collection mechanisms [5], [20]–[23], [25], it is difficult to obtain reliable angular microbeam data sets, so broadbeam experiments must be used. A limited amount of small-angle microbeam data was presented in [19].

The primary broadbeam heavy ion data set [7] upon which this work is based is shown in Fig. 2. It is obvious that with the low LET neon ion the cross section of the RHDB design does not increase with increasing angle, but instead *decreases* with *increasing* angle—i.e., decreasing cross section with increasing effective LET. This behavior violates the assumptions of the original rectangular parallelepiped (RPP) model, which generally assumes increasing cross sections with increasing effective LET [26]–[28]. This lack of agreement between the RPP model and data was discussed in detail in [19]. Since these data are not described adequately by the default RPP model, they have been re-plotted with the RPP cosine corrections removed. The data are plotted as a function of angle instead of effective LET and the cross section was scaled by $\cos(\theta)$ to remove the effective fluence correction. All subsequent data sets will be plotted in this manner to avoid confusion. For the sake of reference, the normally-incident LETs for the ions in Fig. 2 are $^{22}\text{Ne} = 2.8\ \text{MeV}\cdot\text{cm}^2/\text{mg}$, $^{40}\text{Ar} = 8.3\ \text{MeV}\cdot\text{cm}^2/\text{mg}$, and $^{129}\text{Xe} = 53\ \text{MeV}\cdot\text{cm}^2/\text{mg}$.

While the microbeam data provide adequate information to develop an energy deposition response model for normally-incident particles, most of the particles in an isotropic environment, like geosynchronous orbit, are incident at large angles. The solid angle of a cone, shown below in (1)

$$\Omega = 2\pi\left[1 - \cos\left(\frac{a}{2}\right)\right] \tag{1}$$

can be used to approximate a plane of sensitive volumes. When the apex, a, is equal to 120°, $\Omega = \pi$, which is half the solid angle subtended by the surface of a hemisphere. This means that half of the particles in an isotropic environment will be incident at angles below 60° and the other half at angles above 60°. Since a large number of particles are incident at oblique angles, understanding the angular response of bulk SiGe HBTs is critical to developing a representative rate prediction model.

It is interesting to note that some of the atypical angular response observed in Fig. 2 for the RHBD design can be accounted for by using RPP model geometry corrections proposed by Sexton [29] and Petersen [27]. The trigonometric cross section scaling factors work well for the decrease in the argon cross section, but do not account for the approximate 10× decrease in the neon cross section. However, though these model extensions help to explain some of the data, they only apply to a single ion in a limited case. The model sought here must be able to handle any angle of incidence by any ion in the galactic and low-earth spectrums The model must be unified in a way that has not been attempted before in the context of SiGe BiCMOS technologies. To understand why the traditional RPP model extensions fail to account for effects observed in these SiGe HBT data, device-level modeling is required.

II. Device Modeling

A. Ion-Device Interactions

The two types of ion-device interactions considered are normally-incident and large-angle heavy ion strikes with stopping powers of 0.028 pC/μm, which is consistent with the 330 MeV ^{22}Ne used in [7], where the large cross section deviations occurred. The large angle strike is at 60° relative to the surface normal of the device in order to maintain consistency with the broadbeam data set shown in Fig. 2.

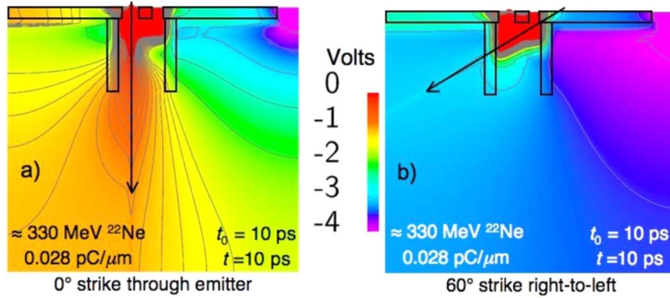


Fig. 3. These slices from 3-D TCAD simulations show the electrostatic equipotential contour lines at the peak of the temporal-Gaussian ion strike, $t = 10$ ps, which is centered at $t_0 = 10$ ps and has a width of 2 ps. In both images, (a) and (b), the substrate p-tap is located on the right side of the figure, where the potential is pinned at -4 V. The normally incident strike through the emitter produces potential warping, or push-out, into the substrate, down to a depth of approximately 18 μm in (a). In contrast, the 60° strike shown in (b) exhibits none of the potential warping seen in (a). The ion-DTI interaction essentially cuts off any subcollector junction response that could affect the electrostatic potential in the substrate.

Position-dependent, normally-incident heavy ion data for the IBM 5AM process are available through the microbeam data sets in Fig. 7 in [21], Fig. 2(c) in [20], and Fig. 3(a) in [19]. These data show that 36 MeV ^{16}O strikes within the region bounded by the DTI result in a charge collection efficiency of approximately 80%, assuming that about 1 pC of charge is liberated during the stopping range of the oxygen ion, which is approximately 25 μm in pure silicon.

Normally-incident 36 MeV ^{16}O strikes outside the DTI have a maximum charge collection efficiency of approximately 20%. That efficiency falls off to a few percent at ≥ 8 μm outside the DTI. Though the IBM 5AM microbeam data sets referenced in the previous paragraph only report a measurable charge collection signal up to 8 μm outside the DTI, other microbeam data sets with the same substrate resistivity and DTI geometry in [20], most notably the bulk SiGe HBTs in Fig. 2(a) and 2(b) therein, show measurable charge collection in excess of 15 μm outside the DTI.

Reliable position-dependent charge collection data gathered at a specific angle, even small angles less than 20°, are difficult to obtain with the microbeam due to spatial and mounting constraints within the beamline vacuum chamber. Therefore, angular effects need to be inferred from broadbeam data and confirmed with 3-D TCAD simulations.

The two heavy ion broadbeam conditions of interest were simulated in the IBM 5AM TCAD model described in [19]–[21] using a particle track with $dQ/dx = 0.028$ pC$/\mu$m. The device was biased in the CML off-state: $V_{\rm E,B,C} = 0$ V and $V_{\rm Sx} = -4$ V. The substrate voltage was taken from the test conditions for the DFF shift registers in [7]. The off-state was previously determined to be the most sensitive operating condition [9], [18], [22]. The simulations were carried out using the Synopsys TCAD tool suite and version X-2005.10 of Sentarus Device. The results of the simulations are shown in Fig. 3(a) and (b).

Comparing Fig. 3(a) and (b) is a straightforward, visual explanation of the cross section roll-off observed in the heavy ion broadbeam data plotted in Fig. 2. For normally-incident strikes, the potential dropped across the subcollector SCR will often push-out into the substrate resulting in a large amount of collected charge. This push-out is very similar to the mechanism described by Hsieh [30]–[32] and Hu [33], published in the context of alpha particles. This topic, in the context of SiGe HBTs, has been discussed [19], [20]. At large angles though, the potential push-out into the substrate is mitigated by the ion passing through the DTI. In this case, since a large portion of the charge liberated by the ion appears outside of the DTI and far away from the SCR of the subcollector junction, a sufficiently large potential-compensating charge density cannot be maintained in the SCR, resulting in no potential push-out.

This same mechanism occurs in both the baseline and RHBD IBM 5AM designs; however, the difference in $Q_{\rm crit}$ between each design, $Q_{\rm crit}(\rm baseline) < Q_{\rm crit}(\rm RHBD)$, means that each will have a different response. At normal incidence, each design behaves in the conventional manner—larger amounts of charge liberated in the substrate result in higher cross sections. However, at oblique angles, though approximately the same amount of charge is liberated, the charge collection efficiency of that charge is much lower since the device response is different, and much less dramatic.

At low dQ/dx, as in the case of 330 MeV ^{22}Ne, which is close to the design SEU threshold, the angular response of the RHBD design makes a large difference in the cross section trend since the amount of charge collected drops with increasing angle, approaching the value of $Q_{\rm crit}$. The baseline design, though it experiences the same angular response as the RHBD design, still collects enough charge to sufficiently exceed $Q_{\rm crit}$, which maintains the normal-incidence cross section.

B. Energy Deposition Response Model

This work relied on the energy transport and calorimetry capabilities of the MRED tool set, which are described in [10]–[16]. Using this tool, it is possible to compute the energy deposited in one or more sensitive (fiducial) volumes due to impinging ions. Furthermore, these fiducial volumes can have weights. The volumes and their weights function in an ensemble to form a linear combination that approximates the total collected charge. This idea was first reported in [13], and subsequently in [14]. The approach is described by (2). The total collected charge is the sum over all fiducial volumes of the product of the weight and total charge liberated.

$$Q_{\rm coll} = \sum_i \alpha_i Q_{L_i}. \tag{2}$$

The total charge liberated (Q) is related to the total energy deposited (ED) through the relationship $Q = (1\ {\rm pC}/22.5\ {\rm MeV}) \times ED$. This linear combination of weighted fiducial volumes is the construct that will be used to model the energy deposition response of the SiGe HBTs considered in this work. Once calibrated to data, usually heavy ion broadbeam cross section data, this modeling method provides an accurate, high-speed approximation to the initial conditions and ensuing temporal evolution of charge transport and collection.

A 2-D projection of the basic energy deposition response model is shown in Fig. 4. The fiducial volumes have been overlaid on the TCAD cross section from Fig. 1. The top-down area

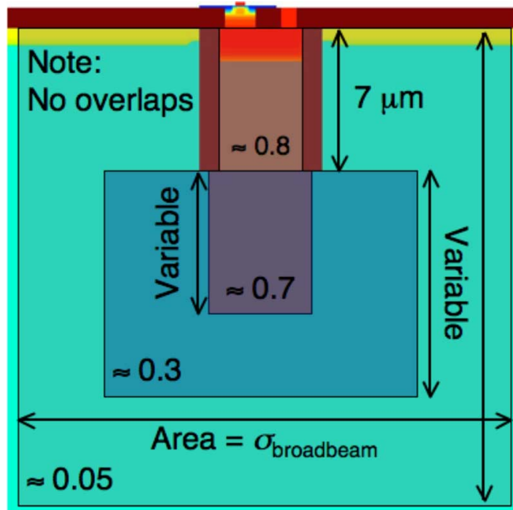


Fig. 4. This is the basic weighted fiducial volume ensemble used to model the radiation response of the IBM 5AM SiGe HBT process considered in this work. The top-down area is estimated from the normal-incidence cross section of each ion in the broadbeam heavy ion data set—three estimations in this case. The weights (efficiencies) of each of the volumes were derived from microbeam data and previous TCAD simulations [19], [20].

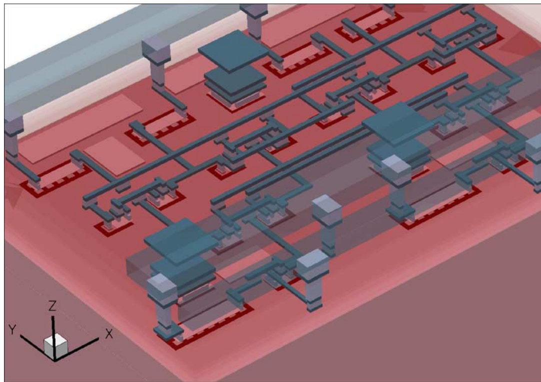


Fig. 5. Full 3-D solid geometry model of the baseline shift register design. The interlevel dielectric and metal have been made transparent. This model, and the one for the RHBD design, were used for the radiation transport simulations. The models themselves are quite large—$110\ \mu\text{m} \times 85\ \mu\text{m} \times 75\ \mu\text{m}$ in the case of the baseline design and $217\ \mu\text{m} \times 85\ \mu\text{m} \times 75\ \mu\text{m}$ for the RHBD design.

of each volume is determined by the normal-incident cross section of the broadbeam heavy ion data, which includes ^{22}Ne, ^{40}Ar, and ^{129}Xe. The weights and depths of each of the volumes are calculated by correlating microbeam data to TCAD simulations, both of which have been discussed previously [19]–[21]. This model was used in a fully reconstructed 3-D model of a shift register stage for all subsequent simulations, including the calibration steps described in Section III-A and the event rate calculations in Section IV. An image of this 3-D model is shown in Fig. 5. The response model shown in Fig. 4 is sufficient to model one stage of the shift register chain in [7]. More volume sets can be used for further variance reduction if necessary.

An important feature of the model shown in Fig. 4 is that it is scalable within the limits evaluated here. The transistors in the baseline and RHBD designs are different sizes. The RHBD transistors are $0.5 \times 2.5\ \mu\text{m}^2$, whereas the baseline transistors are $0.5 \times 1.0\ \mu\text{m}^2$. The difference in transistor size accounts for some of the cross section difference between the baseline and RHBD designs for the argon and xenon data. The model dimensions can be adjusted within reason to account for the size difference without making drastic geometrical or phenomenological changes. The top-down areal cross section is dictated by the data and does not require modification.

The volume depth and weight need to be modified for different transistor sizes because the geometry of the subcollector junction changes with the emitter length. A larger junction presents a larger solid angle to mobile minority carriers in the substrate, which results in higher collection efficiency. A larger junction also results in deeper potential push-out, though this only occurs to a point, plateauing around 18–20 μm below the base-collector junction, which is located at the surface of the shallow trench isolation.

C. *Response Model Implications*

Recalling the ion strikes highlighted in Fig. 3, the linear combination of fiducial volumes shown in Fig. 4 approximates both ion strike conditions. It is clear that the most collected charge will result from normally incident strikes within the region bounded by the DTI. Since the broadbeam data in Fig. 2 show nearly constant cross sections over angle, with the exception of the RHBD data for neon and argon, the larger fiducial volumes have an aspect ratio close to unity.

It is important to note that using a model of weighted fiducial volumes in a linear combination, as is done here, is not a single-point solution. The combination of the fiducial volumes does not have to be linear; it can be non-linear continuous like a polynomial or even discontinuous if logic tests are added in order to add more advanced correlation. The model employed here is part of a much more generalized class of approximations that can be applied to many different situations See the models in [13] and [14] where a linear combination of fiducial volumes is used to model heavy ion, proton, and neutron data in a 0.25 μm CMOS SRAM.

III. Model Calibration

A. *Heavy Ion Response*

Before computing on-orbit event rates, the model was verified against data sets that covered enough of the possible response-parameter space to ensure predictable behavior in a more diverse environment such as geosynchronous or low-earth orbit. The model described in Section II-B was calibrated to the heavy ion datasets for the baseline and RHBD designs shown in Fig. 2.

In each of the two cases, the calibration scheme is the same and follows this general procedure.

1) Size top-down area of all three fiducial volumes corresponding to their counterpart heavy ion cross section at normal incidence—neon, argon, and xenon in this case.
   a) This step excludes the volume contained entirely within the DTI, labeled with a weight of 0.8 in Fig. 4. The normally incident neon cross section is slightly larger than the in-trench silicon area in both the baseline and RHBD design data.

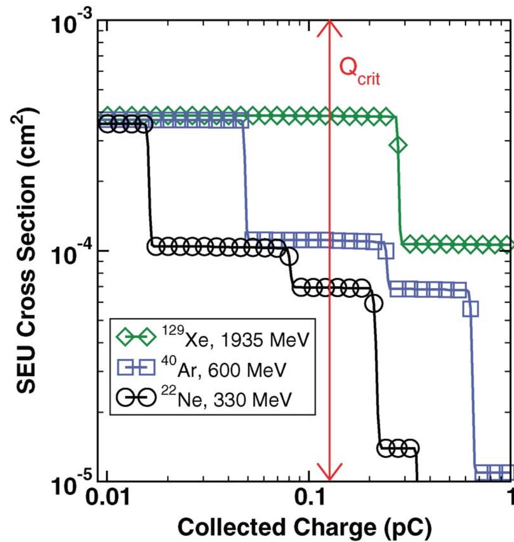


Fig. 6. This figure shows simulated charge collection cross sections at normal-incidence for the baseline shift register design. The Q_{crit} is chosen so that the extracted cross section most closely matches the dataset in question. Data markers are sparse to aid viewing.

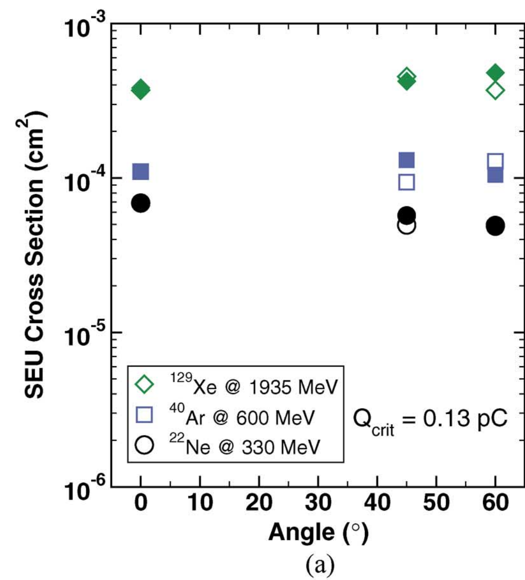
2) Infer the thickness and weight of each volume from microbeam or laser test data and TCAD simulations. The numbers listed in Fig. 4 are appropriate starting values.
3) Simulate all ions in the dataset at normal incidence to check that this simplest case returns the correct result.
   a) At this point, a critical charge must be determined so that the cross section can be evaluated with consistency for all ion species and angles. An example cross section collected charge curve is shown in Fig. 6.
4) Simulate each set of ion angles individually and make minor adjustments to the thickness and weight of the appropriate fiducial volumes.
5) Finally, in order to gain a self-consistent solution, all data points must be simulated, the results evaluated using the same critical charge value, and an accurate match to all data achieved.

At this point, it is important to mention a feature of the simulation results displayed in Fig. 6: the device sensitivity is dominated by direct ionization from the primary incident particle. This fact could also be derived from the low SEU threshold in combination with the knowledge of large charge collection volumes. Regardless of this fact, all simulations were carried out with complete physics lists, including the Geant4 binary intra-nuclear collision cascade [34] to determine the final state for ion-ion nuclear reactions.

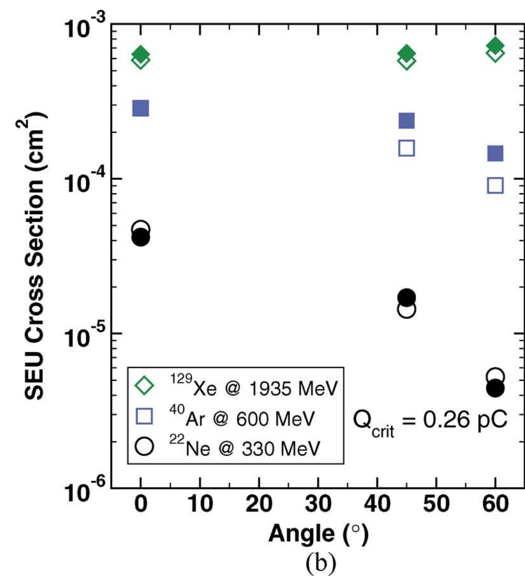
The calibrated heavy ion results for both the baseline and RHBD circuit designs are shown in Fig. 7(a) and (b). The Q_{crit} for each of the calibrations is displayed on the individual figures.

B. Proton Calibration Results

The experimental data shown in Fig. 2 were gathered and published in 2005 [7] and only included heavy ion cross sections. Proton data were collected during recent experiments on the CREST chip [7] at the Crocker Nuclear Laboratory (CNL) at the University of California at Davis using 63 MeV protons.



(a)



(b)

Fig. 7. Plots (a) and (b) show the calibrated results of the computer simulations for the entire 127-stage shift register from [7]. In each case the open symbols are the data from Fig. 2 and the closed symbols are the derived simulation results from output similar to that shown in Fig. 6. (a) Baseline design heavy ion calibration; (b) RHBD heavy ion calibration.

As with other high-speed bit error rate tests, all the cross sections reported refer to the event cross section and not the error (number of upset bits in an event) cross section. This also applies to the heavy ion data already presented.

These data were taken on the baseline and RHBD designs at several different data rates at normal incidence and a grazing angle. The full data set is plotted in Fig. 8(a). For reference, the baseline design is the nominal switching architecture from [7] and the RHBD design is the dual-interleaved architecture from [7]. The test was conducted using the CREST on-board data and clock generation, but the events were recorded using an external Anritsu MP1764C error detector, which is part of a bit error rate test (BERT) system. This data set is consistent with other SiGe HBT high-speed proton tests [5], [9]. The cross section is approximately constant across different data rates.

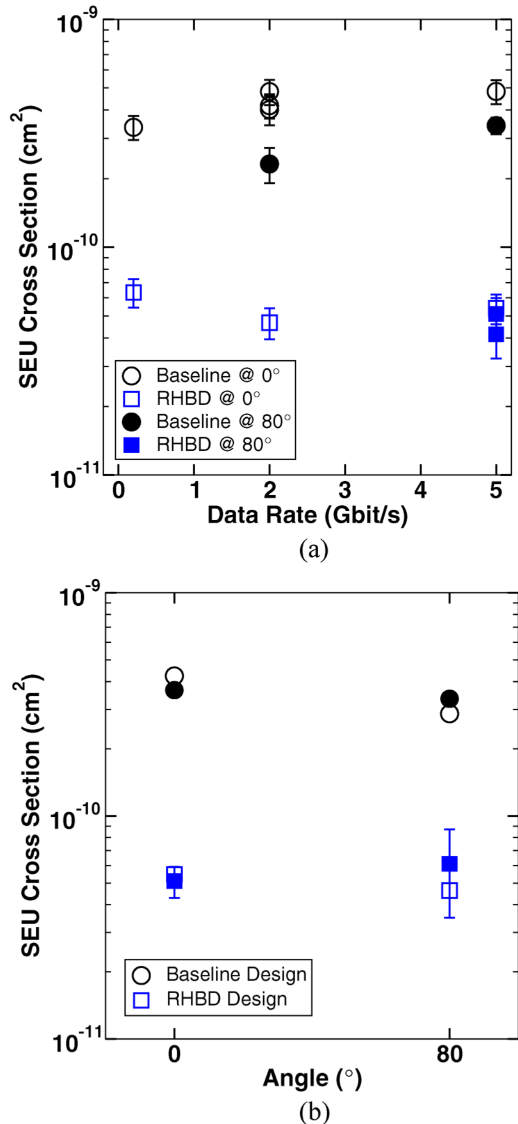


Fig. 8. (a) 63 MeV proton data from CNL taken on the baseline and RHBD CREST chip designs. In [7] these were referred to as the nominal switching current (baseline) and dual-interleaved (RHBD) architectures. The error bars are 1σ and represent the propagation of a 10% fluence error and a 1σ statistical error on the number of events recorded. (b) A comparison between the proton data from (a) and simulation results based on the model described in Section II-B, which was calibrated to heavy ion data. The strong agreement shown above was obtained by simply changing the particle and energy in the simulation; no further adjustments were made. The open symbols are data based on the average across data rate from (a) and the solid symbols are simulation results using the response model. Error bars, shown if they are bigger than the data marker, are 1σ statistical errors.

This data set can now be used to check the proton response of the model developed in the previous section. These modeling results are shown in Fig. 8(b). The data shown in Fig. 8(b) are the average cross section across data rate since the simulation model cannot take data rate into account, something that is the subject of current investigations.

As in previous modeling scenarios [14], the heavy ion model was validated against proton data by only a change of particle and energy in the simulation environment. The strong match between simulation and data validates a larger portion of the model's acceptable parameter space, making it usable for environments with large proton fluxes. These simulation results were obtained from the model calibrated with heavy ion data only; no further adjustment was required.

IV. Event Rate Calculations

A. Geosynchronous and Low-Earth Orbit Event Rates

MRED, used for the modeling throughout this work, has the ability to import and sample across pre-defined particle flux spectra [11], [12]. CREME96 [35] was used to generate the particle flux spectra for the geosynchronous (GEO) and low-earth orbit (LEO) environments, but CREME96 was not used to perform the rate calculations. Both of the environments were solar minimum/quiet conditions, included available ion species from $1 \leq Z \leq 92$, and assumed 100 mil of aluminum shielding. The LEO spectra were for the space station orbit, which, according to CREME96, is at an inclination of 51.6° and an orbital radius of 500 km. The rate prediction methodology used to carry out the computations is described in [11] and [12].

The environment computations for the baseline and RHBD designs used the simulated energy deposition from approximately 5×10^8 individual events with a hadronic cross section bias factor of 75. The bias factor serves to reduce the variance for very rare events by increasing their occurrence in a statistically well-defined manner. In previous cases [11], the bias factor was set to 200. However, if the bias factor is set too high, too many primary particles are consumed in nuclear reactions, artificially depleting the transmitted flux on the backside of the target, which is non-physical. The target, shown in Fig. 5, is large and quite thick, about 110 μm $\times$ 85 μm $\times$ 75 μm, so backside flux depletion is an issue. All ions simulated were incident on the target uniformly over 4π steradians for both GEO and LEO environments.

The event rates for both GEO and LEO environments are plotted in Fig. 9(a) and (b). The rates shown for each ion in the environmental spectrum have been reverse integrated, from right-to-left, so that the total event rate for each design, at a particular critical charge, is that rate or less.

There is a 1.6$\times$ to 6.2$\times$ difference between the total rate for the baseline and RHBD designs due to the higher critical charge of the RHBD design. The dominant contribution to each of the four rate curves shown comes from $25 \leq Z \leq 30$, which are the elements manganese, iron, cobalt, copper, and zinc. This large contribution is due to the fact that many of these impinging ions have high stopping powers in conjunction with significant flux. The contributions of these five ions approach the contributions from the other 81 ions that were simulated; this is true for both GCR and LEO event rates. However, in LEO orbits, the flux of these key ions is much lower due to natural magnetic shielding, leading to the lower event rate.

The baseline and RHBD curves shown in Fig. 9(a) and (b) appear in a counterintuitive way since the rate curve for the RHBD device is above the baseline device. However, the RHBD device has a larger subcollector junction area by a factor of approximately 1.6 since it is a bigger device relative to the baseline design. The rate curve of the RHBD design is higher since the area of the subcollector junction plays a significant role in the device's response to charge liberated from ionizing radiation.

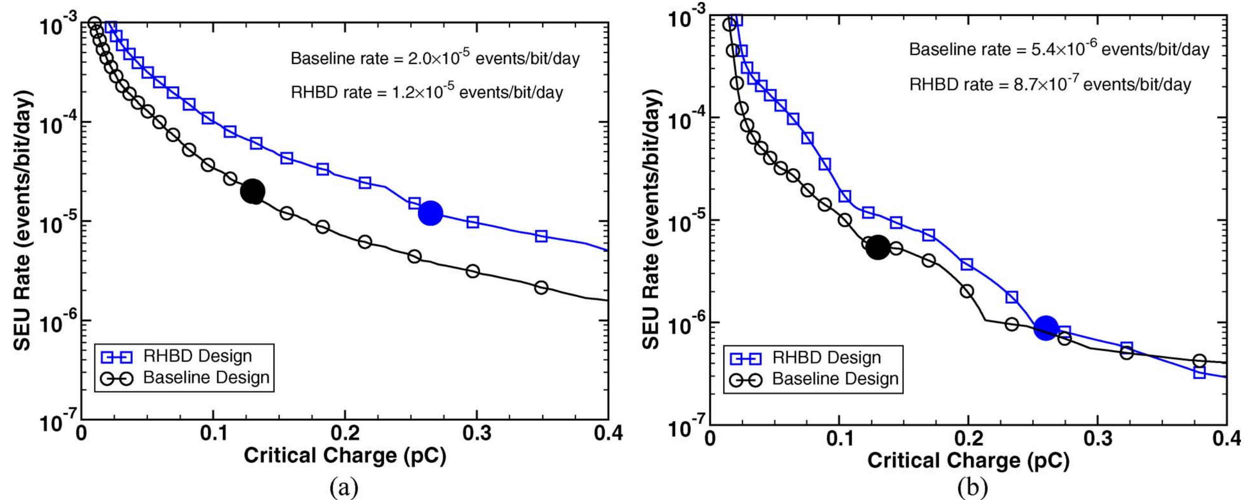


Fig. 9. These figures show the simulated event rates for the two shift register designs. The LEO event rate is approximately one order of magnitude below the GCR event rate due to sensitivity dominated by direct ionization and the reduced flux of many significant contributors. There is a 1.6× to 6.2× difference between the event rates for the baseline and RHBD designs. The data markers have been thinned to aid viewing. The large markers show where the rate was evaluated based on the critical charge derived from the fit shown in Fig. 7(a) and (b)—0.13 pC and 0.26 pC. (a) Geosynchronous orbit event rate; (b) low-earth orbit event rate.

The environment-based SEU rates presented are to be interpreted as event rates, not error rates. The energy deposition response model developed in Section II-B makes no attempt to derive temporal or event-composition information—i.e., zero-to-one, one-to-zero, flatten-to-one, flatten-to-zero, mangle, etc. [36]. The model neither calculates the number of upset bits in the event nor yields any information regarding preferences for burst error modes. However, the model makes the most accurate representation to date by providing an energy deposition response behavior consistent with device geometry and the charge collection mechanisms present in this type of process technology.

The present modeling approach is the first and necessary step towards solving the more intricate, time-dependent problem, which requires the energy deposition model to adapt its properties and volume-to-volume logic dynamically. Such a model would also have to be tied to a circuit-level simulator with compact models in order to produce burst error information reliably. In addition to those non-trivial steps, there is a great need for experimentally measured radiation-induced current transients in SiGe HBT BiCMOS process technology. Current commercial TCAD simulators have been successful at modeling the total collected charge from radiation events [19]–[21], [24], [37], but there are no experimental data with which to compare the induced current transients. It is believed that the present TCAD radiation-induced transients are inaccurate in some regimes. Experiments and simulations are currently underway to make these types of high-bandwidth transient measurements and continue advancing the state-of-the-art in energy deposition response modeling.

V. Conclusion

The shape and relationship between the fiducial volumes represents a critical aspect of this study. The fiducial volumes explain in a quantitative and qualitative way the once-anomalous angular response of the technology, the low SEU threshold, and the large saturated cross section observed for the most highly ionizing particles. Putting this model together unifies many years of experimental and theoretical work and provides intuition to designers considering SiGe HBT projects. It also opens the door for more complex types of modeling that will begin to look at time-domain effects and other aspects of extreme, high-speed digital technologies like this.

Acknowledgment

The authors would like to thank K. LaBel, L. Cohn, the Special Purposes Processor Group at the Mayo Foundation, and D. M. Fleetwood. Thanks are also due to AJ KleinOsowski, G. D. Carpenter, and IBM Research for supporting the author during manuscript preparation and the Nuclear and Space Radiation Effects Conference. This work was conducted in part using the resources of the Advanced Computing Center for Research and Education (ACCRE) at Vanderbilt University, Nashville, TN.

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Impact of Heavy Ion Energy and Nuclear Interactions on Single-Event Upset and Latchup in Integrated Circuits

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***Abstract*—The effects of heavy ion energy and nuclear interactions on the single-event upset (SEU) and single-event latchup (SEL) response of commercial and radiation-hardened CMOS ICs are explored. Above the threshold LET for direct ionization-induced upsets, little difference is observed in single-event upset and latchup cross sections measured using low versus high energy heavy ions. However, significant differences between low- and high-energy heavy ion test results are observed below the threshold LET for single-node direct ionization-induced upsets. The data suggest that secondary particles produced by nuclear interactions play a role in determining the SEU and SEL hardness of integrated circuits, especially at low LET. The role of nuclear interactions and implications for radiation hardness assurance and rate prediction are discussed.**

***Index Terms*—Indirect ionization, integrated circuit reliability, nuclear reactions, radiation effects, radiation hardness assurance, single-event effects, single-event latchup, single-event upset, soft errors.**

I. Introduction

GROUND-BASED heavy ion testing for single-event effects (SEE) is often used to study the physical mechanisms contributing to SEE, estimate on-orbit error rates, and qualify parts for use in space-based systems. In the past, typical accelerator facilities used for SEE testing have provided particles whose energy is on the order of a few (1–10) MeV per nucleon (MeV/u, or equivalently, MeV/amu). With the advent of multi-micron thick device overlayers and flip-chip packaging, the usage of facilities in the 10–100 MeV/u range has increased dramatically. However, heavy ion energies in the natural space environment reach into hundreds of GeV/u, with a peak flux at a few hundred MeV/u [1]. With few exceptions, such ion energies are not available in ground-based test facilities, and concerns about the fidelity of accelerator tests for simulating the response of integrated circuits (ICs) in the real space radiation environment have resulted [2]. Previous studies in the literature have sometimes shown differences in single-event upset (SEU) response with ion energy [3]–[5], and in other cases have not [6]–[8].

Recently, the role of nuclear interactions between high-energy particles and the materials in integrated circuits has received growing attention [7]–[13]. Typically, heavy-ion-induced SEU results from direct ionization caused by the release of electron-hole pairs along the path of an energetic charged particle incident on an integrated circuit. Although in some cases upsets due to proton direct ionization have been observed [14], proton and neutron-induced SEUs are generally attributed to ionization by reaction products (e.g., spallation reaction products or Si recoils from Coulomb scattering) produced indirectly by nuclear interactions between an incident energetic particle and the materials in an IC. In 1998, Koga suggested that ions with very low LET (<1 MeV-cm^2/mg) might cause SEUs due to nuclear interactions that would be observable if the threshold LET for direct ionization-induced upsets was high (for example, as would be the case for SEU-hardened ICs) [7]. More recently, Warren, *et al.*'s experiments [9] on hardened 4-Mbit SRAMs have corroborated this mechanism, with high-energy heavy ion SEU observed for LETs less than 2 MeV-cm^2/mg in an SRAM that appears to have a direct ionization upset threshold LET of greater than 20 MeV-cm^2/mg. Unfortunately, no equivalent low-energy data was presented to more conclusively prove that high-energy nuclear interactions were the mechanism for the observed results. Upsets in SEU-hardened SRAMs have also been attributed to secondary particles traversing multiple sensitive volumes and causing upsets at lower LETs than are possible from single-node strikes [13]. In [12], we showed data taken at high- and low-energy heavy ion accelerators indicating that in some cases significant differences exist between SEU cross sections as a function of ion energy. While it was conjectured that these differences were due to the effects of nuclear interactions as described in [9], [11], the limited data that were available did not overwhelmingly support this hypothesis. In addition, it was shown

Manuscript received July 19, 2007; revised September 9, 2007. This work was supported in part by the Defense Threat Reduction Agency under DTRA IACRO # 07-4196, in part by the U. S. Department of Energy, and in part by the NASA Electronic Parts and Packaging Program. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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Digital Object Identifier 10.1109/TNS.2007.909844

0018-9499/$25.00 © 2007 IEEE

TABLE I
HEAVY ION BEAMS USED IN THIS WORK

Facility	Ion	LET (MeV-cm^2/mg)	Energy (MeV/u)
BNL	360 MeV Au	82.7	1.8
	320 MeV I	59.7	2.5
	290 MeV Br	37.1	3.7
	265 MeV Ni	26.6	4.6
	190 MeV Ti	19.8	4.0
	190 MeV Ca	16.3	4.8
	210 MeV Cl	11.4	6.0
	185 MeV Si	7.9	6.6
	12 MeV C	4.5	1.0
	140 MeV F	3.4	7.4
	99 MeV C	1.4	8.3
TAMU	2.9 GeV Xe	40.6	25
	262 MeV Kr	40.0	3.1
	961 MeV Kr	28.7	15
	1.9 GeV Kr	20.6	25
	785 MeV Cu	19.6	15
	3.0 GeV Kr	14.7	40
	509 MeV Ar	8.6	15
	944 MeV Ar	5.6	25
	1.6 GeV Ar	3.9	40
	531 MeV Ne	1.8	25
	788 MeV Ne	1.2	40

that it is critical to perform SEE measurements below the direct ionization threshold at sufficiently high ion fluence to ensure that any differences due to ion energy effects can be resolved.

In this summary, we describe new high and low-energy measurements of SEE in a variety of ICs from multiple manufacturers. ICs tested include commercial and radiation-hardened devices fabricated in bulk silicon and silicon-on-insulator (SOI) technologies. The ICs studied here are primarily CMOS SRAMs, but also include an analog-to-digital converter (ADC). While previous studies have focused almost exclusively on the impact of ion energy and the role of nuclear interactions on SEU response, in this paper we also explore the importance of ion energy on single-event latchup (SEL) response. Finally, implications for hardness assurance and SEE rate prediction are discussed.

II. EXPERIMENTAL DETAILS

Low-energy heavy ion irradiations were performed using the tandem Van de Graaff at Brookhaven National Laboratory (BNL), while high-energy heavy ion irradiations were performed at the Texas A&M University (TAMU) heavy ion cyclotron. Beams at BNL ranged in energy from 1–8 MeV/u, while the ion beams at TAMU ranged from 3–40 MeV/u. A complete listing of the heavy ion beams used is shown in Table I. Static SEU cross sections in SRAMs were measured using either a Hewlett Packard HP82000 digital ASIC tester, a CertiMAX Model 105 portable digital ASIC tester, or a TEMIC dedicated portable memory tester. A checkerboard pattern was loaded into the memory, the SRAM was exposed to heavy ions, and following the irradiation the memory was read and the number of errors was counted. In almost all cases, the same test setup was used to test the same parts for both low- and high-energy ions to minimize any variation in cross section due to test setup. Single-event latchup cross sections were measured using a computer-controlled power supply. The IC was allowed to power up into its preferred state (i.e., no specific pattern was written), the IC was exposed to heavy ions, and during the irradiation the power supply current was monitored. If the current exceeded a predetermined threshold (set slightly above the static current), a latchup was counted and the IC power supply was cycled. Experiments were performed using ions at both normal and angled incidence; data from angled irradiations are plotted using effective LET as defined by the standard inverse cosine law. The implications of this are discussed below. Error bars on plots indicate either the standard deviation in cross section between parts (when multiple parts were tested) or the 95% confidence interval for errors given by Poisson statistics [15]. Throughout this paper, the term "low-energy" will be used to refer to BNL ions with energy less than 10 MeV/u, while TAMU ions with energy greater than 10 MeV/u will be referred to as "high-energy".

TABLE II
DEVICES STUDIED IN THIS WORK

Study	Vendor	Part No.	Size (bits)	Bias Voltage (V)
SEU	MHI	N/A	256K	1.8
	Sandia	EC256K	256K	4.5
	Sandia	EC1024K	1M	3.0
SEL	ST Microelectronics	M68AW511	4M	3.6
	Samsung	K6X4008C1F	4M	5.5
	Vendor A	N/A	1M	1.6
	Analog Devices	AD7827BR	N/A	5.5

Seven different device types were studied in this work, three for SEU and four for SEL. For SEU, 256-Kbit fully depleted 0.2-μm SOI SRAMs from Mitsubishi Heavy Industries (MHI) with body ties were tested [16], as well as 256-Kbit 0.5-μm bulk SRAMs and 1-Mbit 0.35-μm SOI SRAMs fabricated at Sandia National Laboratories [17]. For SEL, three commercial SRAMs and a commercial ADC were tested. Table II lists more detailed information on the device types and bias conditions used. For SEU, all tests were performed at room temperature and the minimum rated bias voltage, while SEL tests were performed at the maximum rated bias voltage and a temperature of either 75°C or 85°C. All parts were delidded for experiments at both heavy ion test facilities.

III. SINGLE-EVENT UPSET EXPERIMENTAL RESULTS

A. *Sandia 256-Kbit Bulk SRAM*

The 256-Kbit radiation-hardened bulk silicon Sandia SRAM was designed as a special test IC to have regions of differing SEU sensitivity. The SRAM is split into 16 blocks (16 Kbits each) with different-sized feedback resistors used for SEU hardening. Blocks 8–15 of the SRAM comprise 128 Kbits of the SRAM and have the nominal (largest) size feedback resistors used in the technology, while the other eight 16-Kbit blocks have resistors ranging down to no feedback resistance in Block 0. Fig. 1 shows the measured low-energy (BNL) upset cross section curves for the 256-Kbit Sandia SRAM, indicating that the SEU threshold LET varies between the blocks from less than 10 to about 30 MeV-cm^2/mg (the nominal design target). This range of direct ionization threshold LET allows us to examine the effects of ion energy on SRAM blocks that have differing upset thresholds (i.e., different critical charges) but that are otherwise identical.

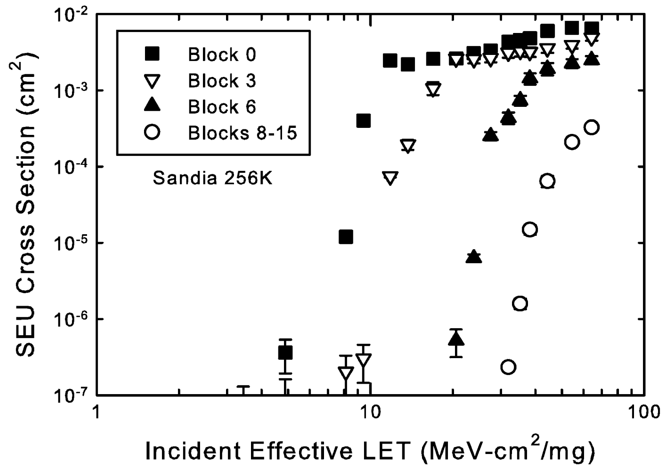

Fig. 1. Measured SEU cross section for Sandia 256-Kbit SRAMs taken with low-energy (BNL) heavy ions. Different blocks of the SRAM have different feedback resistors for SEU hardening. Data for blocks 8–15 have been normalized to a single 16-Kbit block size. Error bars indicate 95% confidence interval for Poisson statistical error.

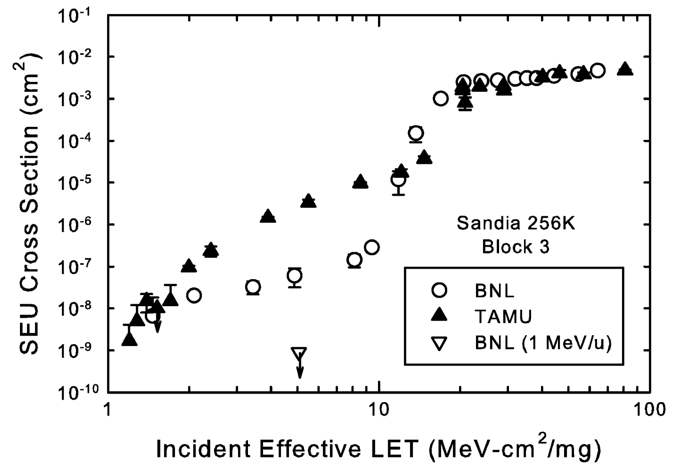

Fig. 3. Measured SEU cross section for Block 3 of the Sandia 256-Kbit SRAM taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars represent standard deviation in cross section between parts tested.

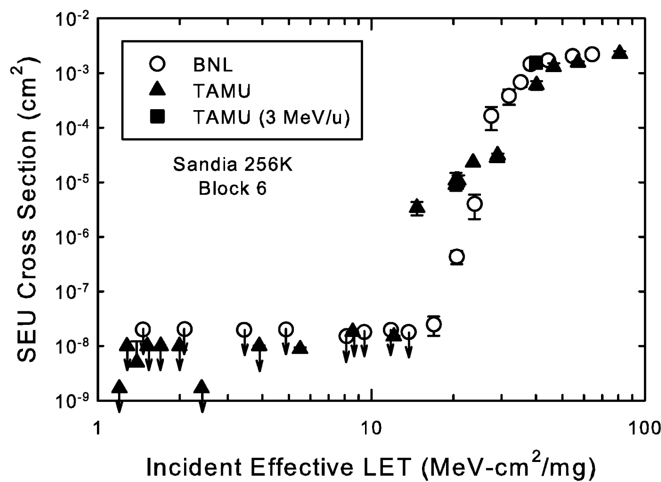

Fig. 2. Measured SEU cross section for Block 6 of the Sandia 256-Kbit SRAM taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars represent standard deviation in cross section between parts tested.

Fig. 2 shows the high and low-energy SEU cross sections for Block 6 of the Sandia 256-Kbit SRAM. Note that throughout this paper, cross section data will be plotted using a logarithmic scale on both axes to accentuate any differences between low- and high-energy data. Plotting the data in this manner also shows more clearly when (or if) saturation in the cross section has been reached and facilitates interpretation of the data [18]. Downward pointing arrows indicate that the data point is an upper bound and that no upsets (or latchups in the case of SEL data) occurred at this point. Data for Blocks 8–15 were previously analyzed and included in [12], and the characteristics of Block 6 are similar. First, note that the high and low-energy data converge at high LET. In this region, direct ionization dominates and the upset cross section is expected to be energy independent [8]. Note also that a low-energy (3 MeV/u, LET ~40 MeV-cm^2/mg) data point taken at TAMU by degrading the high-energy beam (yellow square) lies exactly on the BNL data (which in this region were taken at an energy of ~3.7 MeV/u). However, between incident effective LET's of 12 to 20 MeV-cm^2/mg, the high-energy TAMU data lie significantly above the BNL data. At an LET of 15 MeV-cm^2/mg, the TAMU SEU cross section is nearly 3 orders of magnitude greater than the SEU cross section measured at BNL.

At BNL, no incident particle with LET less than 16 MeV-cm^2/mg ever causes an upset, even after multiple irradiations to a cumulative fluence in excess of 10^8 ions/cm^2. At TAMU, numerous high-fluence irradiations with LET less than 10 MeV-cm^2/mg produced only 2 upsets (one at 1.4 and one at 5.5 MeV-cm^2/mg) after a total delivered fluence for all parts and all ions of nearly 3×10^9 ions/cm^2. If we assume that the BNL data give a true indication that the threshold LET for single-node direct ionization-induced SEU in this block of the SRAM is ~20 MeV-cm^2/mg, these data suggest that incident particles with LET below 16 MeV-cm^2/mg at BNL energies are unable to produce secondary particles (via nuclear interactions) with LET greater than 20 MeV-cm^2/mg. While such interaction products apparently can occasionally be produced at TAMU for incident effective LETs less than 10 MeV-cm^2/mg, they are rare events indeed.

The high and low-energy SEU cross sections for Block 3 of the Sandia 256-Kbit SRAM are shown in Fig. 3. This block of the SRAM has a threshold LET for direct ionization-induced SEU of only about 10 MeV-cm^2/mg. Once again, at high LET all of the cross section data converge to a single curve. However, at lower incident effective LETs (<10 MeV-cm^2/mg) something interesting happens. Even at BNL, there is an extended "tail" in the cross section curve, with upsets occurring down to incident LETs of 1.5 MeV-cm^2/mg (albeit with very low cross section). At TAMU, this tail in the cross section curve is more than an order of magnitude higher than at BNL between incident effective LETs of 3–10 MeV-cm^2/mg, but converges to the low energy data for LET <2 MeV-cm^2/mg. If we again assume that the "main" part of the BNL curve indicates a true threshold LET for single-node direct ionization-induced upsets of ~10 MeV-cm^2/mg, these data suggest that both high and

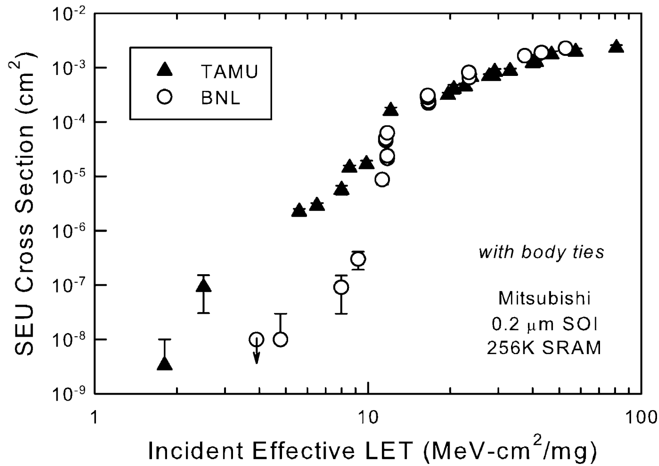

Fig. 4. Measured SEU cross section for Mitsubishi 256-Kbit fully-depleted SOI SRAM taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars indicate 95% confidence interval for Poisson statistical error.

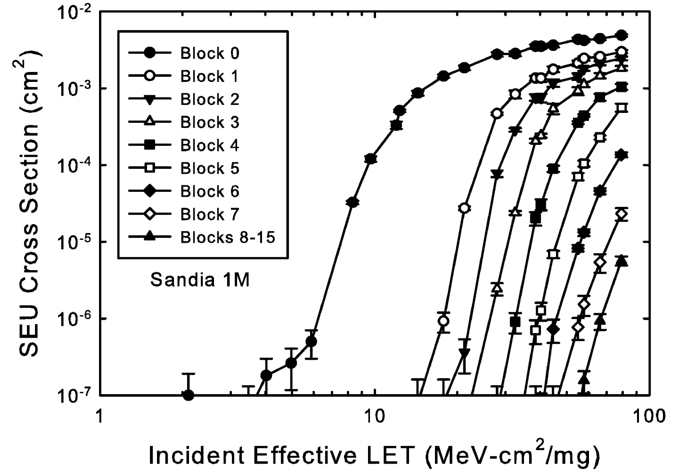

Fig. 5. Measured SEU cross section for Sandia 1-Mbit SOI SRAMs taken with low-energy (BNL) heavy ions. Different blocks of the SRAM have different feedback resistors for SEU hardening. Data for blocks 8–15 have been normalized to a single 64-Kbit block size. Error bars indicate 95% confidence interval for Poisson statistical error.

low-energy ions are capable of producing secondary particles above this threshold. For example, silicon recoil atoms have a maximum LET of about 14 MeV-cm^2/mg and would be able to cause upsets in this block of the SRAM. At both BNL and TAMU, beams with incident LET below 10 MeV-cm^2/mg have sufficient energy to exceed the Coulomb barrier for silicon interactions [11], and such events are likely a key contributor to the low-LET tails at both facilities. Also shown in Fig. 3 is a data point taken with a very low energy (1 MeV/u) carbon beam at BNL. At this energy, even though the heavy ions are able to penetrate several microns deep into the active silicon, no upsets are observed. This is consistent with computations in [11] that suggest that 1-MeV/u carbon ions are below the threshold energy (i.e., the Coulomb barrier) required to produce the interactions responsible for the upsets that are observed with higher energy ions.

Data for Block 0 (no feedback resistors) are similar to Block 3, with the exception that the tails in the cross section curve for both BNL and TAMU are nearly an order of magnitude higher in cross section, suggesting that even more secondary particles produced by nuclear interactions are able to exceed the direct ionization threshold LET ($\sim$7.5 MeV-cm^2/mg) for this block. These data are discussed in detail and analyzed using MRED nuclear interaction calculations in [19].

B. Mitsubishi 256-Kbit SOI SRAM

The measured SEU cross section as a function of heavy ion incident effective LET for the Mitsubishi fully depleted 256-Kbit SOI SRAM with body ties is shown in Fig. 4. Note that high- and low-energy data on this SRAM were presented in [12], and no significant differences were observed. However, as pointed out in that paper, the measured data covered only three orders of magnitude in SEU cross section and no high-fluence data at low LET had been taken to ensure that a a low-LET “tail” in the upset cross section was not present. Fig. 4 clearly shows the importance of taking high-fluence data at LETs below the threshold for upsets due to direct ionization, as will be discussed in more detail below. As can be seen in this figure, there is indeed a significant tail in the cross section curve for LETs less than 10 MeV-cm^2/mg. Similar to the results for the Sandia 256-Kbit SRAM, the high-energy cross section is considerably higher than the low-energy cross section in this region, with about a factor of 100 difference at an LET of $\sim$5 MeV-cm^2/mg.

C. Sandia 1-Mbit SOI SRAM

The Sandia 1-Mbit radiation-hardened SOI SRAM test IC is similar to the Sandia 256-Kbit bulk SRAM. Like the 256-Kbit bulk SRAM, the SOI SRAM is split into 16 blocks (this time 64 Kbits each) with different-sized feedback resistors. The upper 512 Kbits of the SRAM (blocks 8–15) have the nominal (maximum) size feedback resistors used in the technology, while the other eight 64-Kbit blocks have resistors ranging down to no feedback resistance in Block 0. Fig. 5 shows the measured low-energy (BNL) upset cross section curves for all blocks of the 1-Mbit SOI SRAM. For this SRAM, the direct ionization SEU threshold LET varies from less than 10 MeV-cm^2/mg for no feedback resistors to about 60 MeV-cm^2/mg for nominal feedback resistors. Note that even though these low-energy curves were taken with many different ions at many different angles of incidence, the curves are very well-behaved, with no outlying points or large discontinuities in the data as the ion or angle is changed.

The data change dramatically at high energies, as shown in Fig. 6 for Block 1 of the 1-Mbit SOI SRAM. At high LET, the data again appear to be converging to a single curve, although the BNL cross section is still slightly larger than at TAMU. Below the threshold LET for single-node direct ionization-induced upsets (a bit less than 20 MeV-cm^2/mg), the high-energy data show an abrupt discontinuity as the beam is switched from 40-MeV/u Ar at a high angle of incidence (53°) to a lower-energy 15-MeV/u Ar beam at normal incidence. Similar discontinuities were observed in the other blocks of the SRAM at different LET/energy/ion combinations. In each case, irradiation with the higher-energy, higher-angle ion resulted in a much larger SEU cross section than the lower-energy,

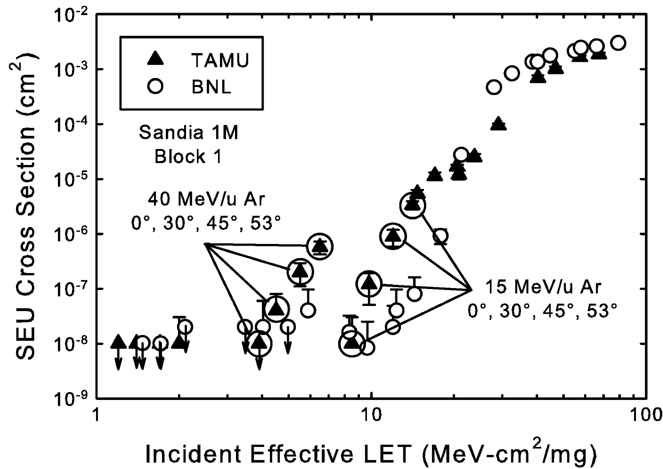

Fig. 6. Measured SEU cross section for Block 1 of the Sandia 1-Mbit SOI SRAM taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars indicate 95% confidence interval for Poisson statistical error.

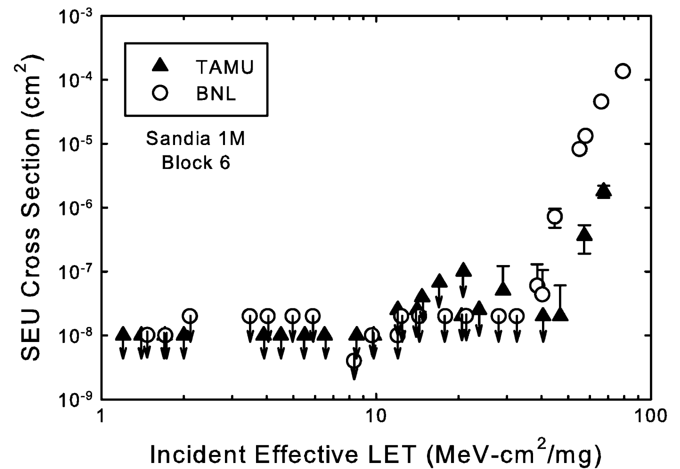

Fig. 7. Measured SEU cross section for Block 6 of the Sandia 1-Mbit SOI SRAM taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars indicate 95% confidence interval for Poisson statistical error.

normally-incident ion with similar effective LET. Obviously, curves such as Fig. 6 are a clear indication of the breakdown of the effective LET concept for high-energy ions that produce upsets by mechanisms other than direct ionization within a single sensitive volume.

It is interesting to contrast the results shown in Fig. 6 for the Sandia SOI SRAM with those in Fig. 2 for the Sandia bulk silicon SRAM. At BNL, both SRAMs (Block 6 for the bulk SRAM and Block 1 for the SOI SRAM) have a very similar direct ionization SEU threshold LET of about 20 MeV-cm^2/mg. Coincidentally, both SRAMs even have similar SEU cross section near saturation. However, the bulk SRAM shows no unusual angular behavior similar to the SOI SRAM, *even though the same 40-MeV/u and 15-MeV/u Ar beams were used to characterize both devices*. Both devices are fabricated in the same facility using almost entirely the same materials and similar processes. It seems likely that this difference in behavior is due to the very different sensitive volume in the SOI SRAM (very thin and truncated by the buried oxide) compared to the bulk silicon device.

Turning to one of the blocks with larger feedback resistors, Fig. 7 shows the high- and low-energy SEU cross section curves for Block 6 of the 1-Mbit SOI SRAM. For this block, the direct ionization SEU threshold LET as measured at BNL is about 40 MeV-cm^2/mg. Below this LET, no upsets are ever observed at BNL even after an accumulated fluence of 10^9 ions/cm^2. Similarly, no upsets are observed at TAMU below 40 MeV-cm^2/mg after a similar accumulated fluence, with the exception of 2 upsets observed at an LET of 29 MeV-cm^2/mg using 25-MeV/u Kr ions at an angle of incidence of 45°. Once again, if the direct ionization SEU threshold LET is large enough, it appears that it becomes impossible (or at least, extremely unlikely) for nuclear interactions to generate particles capable of inducing upsets. This strongly suggests that for devices with such high direct ionization SEU thresholds, only very rare interactions between high-energy ions and high-Z materials such as W are capable of producing reaction products with large enough LET to cause upsets. In Fig. 7, for the first time we see a significant difference between the low and high-energy results at high LET, with the BNL cross section larger than at TAMU by almost 2 orders of magnitude at an LET of 70 MeV-cm^2/mg. Data for the other blocks having large resistors is similar, with the difference in high-LET cross sections becoming less as the resistor size is decreased. Although we have no definitive mechanism for this effect, we believe it may be due to differences in the heavy ion track structure. As noted previously, the more spread out track of high-energy heavy ions may lead to reduced charge collection in the sensitive volume, making low-energy testing conservative with respect to high-energy facilities [8]. We also suspect that given high enough test LET, the two curves might well converge to the same saturation cross section.

IV. Single-Event Latchup Experimental Results

As shown previously, it is difficult to observe nuclear interaction-induced upsets in many commercial devices because their threshold for direct ionization-induced upsets is so low that relatively rare nuclear interactions are dominated by direct ionization events [12]. However, several commercial ICs have been shown to be sensitive to latchup and to have heavy ion SEL threshold LETs between 10–20 MeV-cm^2/mg [10]. If heavy ions can cause nuclear reaction-induced SEU, it is reasonable to expect that the same mechanism could lead to SEL, especially in high-energy heavy ion environments. Therefore, it seems likely that heavy ion nuclear interaction-induced latchup could be observed in commercial ICs. Indeed, recent research has suggested that high-energy proton-induced latchup in commercial ICs can result from interactions between protons and high-Z materials used in semiconductor manufacturing [10]. Accordingly, we selected several commercial ICs that had been previously shown to be sensitive to SEL and studied their response as a function of ion energy.

A. ST Microelectronics 4-Mbit SRAM

High and low-energy SEL cross sections for an ST Microelectronics 4-Mbit SRAM (M68AW511) are shown in Fig. 8. The SEL cross section was measured at a temperature of 85° C. The characteristics are remarkably similar to the SEU cross sections discussed up to this point. The direct ionization threshold LET for latchup as measured at BNL is ~16 MeV-cm^2/mg. However, the high-energy SEL cross section curve shows latchup

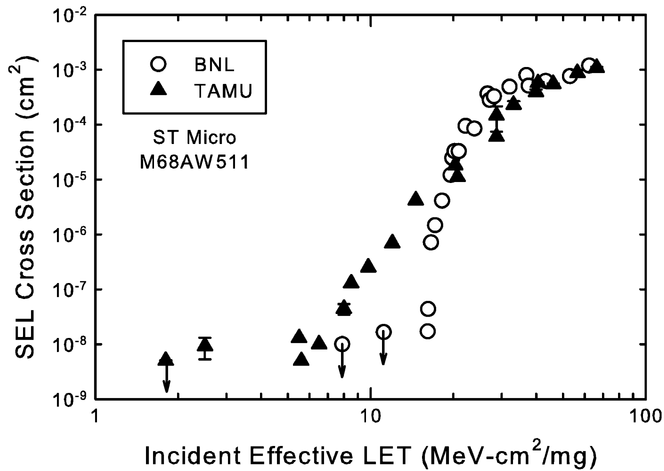

Fig. 8. Measured SEL cross section for 4-Mbit ST Microelectronics SRAMs taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars represent standard deviation in cross section between parts tested.

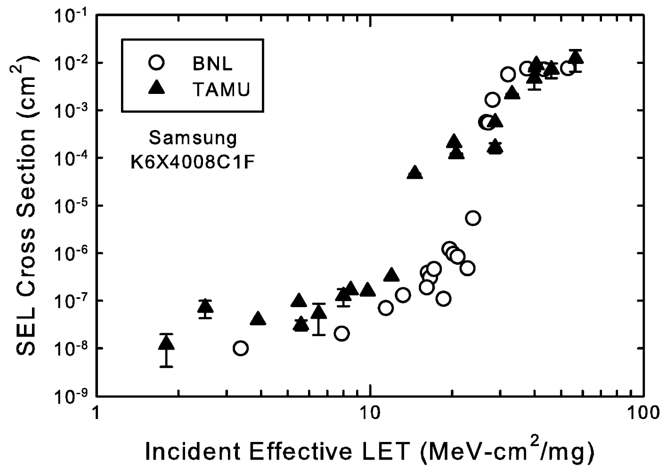

Fig. 9. Measured SEL cross section for 4-Mbit Samsung SRAMs taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars represent standard deviation in cross section between parts tested.

occurring at much lower incident effective LET values than this. For example, the only LET at which latchup did not occur at TAMU was 1.8 MeV-cm^2/mg, while at BNL the same part was latchup-free at an LET of 11 MeV-cm^2/mg. At an LET of 15 MeV-cm^2/mg, the high-energy SEL cross section is nearly 3 orders of magnitude higher than at low energy. At high LET, the high-energy SEL curve falls somewhat below the low-energy curve; the reason for this discrepancy is currently unknown, however, it is consistent with much of the SRAM SEU data.

B. Samsung 4-Mbit SRAM

Fig. 9 shows high and low-energy SEL cross sections for a Samsung K6X4008C1F 4-Mbit SRAM. The SEL cross section was measured at a temperature of 85° C. Similar to the soft blocks of the Sandia 256-Kbit SRAM (e.g., Fig. 3), there is a substantial tail in the SEL cross section data at both low and high energy. In fact, no ion/energy combination at which any test was performed at either facility ever produced zero latchups. In the low-LET tail region, the high-energy data exhibit a higher SEL cross section than the low-energy data, but the difference is considerably smaller than observed in Fig. 3 for SEU in the Sandia

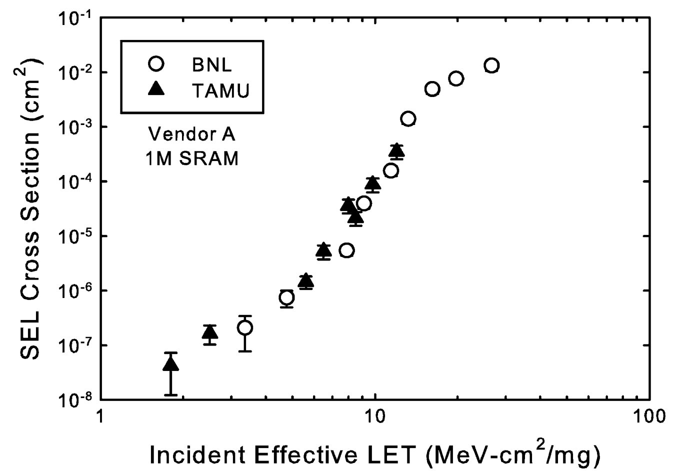

Fig. 10. Measured SEL cross section for 1-Mbit Vendor A SRAMs taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars indicate 95% confidence interval for Poisson statistical error.

SRAM. In addition, the cross section in this region is about 100 times lower than in the Sandia SRAM. At intermediate LETs near 15 MeV-cm^2/mg, the largest difference (about 2 orders of magnitude) in SEL cross section is observed, similar to the ST Microelectronics SRAM. Finally, it appears that at the highest LETs, the high- and low-energy curves converge.

C. Vendor A 1-Mbit SRAM

The SEL cross section for Vendor A 1-Mbit SRAM test ICs is shown in Fig. 10. The SEL cross section was measured at a temperature of 75°C. This SRAM, fabricated in a 0.14-μm CMOS technology, is the most SEL-sensitive part that was studied. Like the Samsung 4-Mbit SRAM, there was no ion/energy at which the Vendor A SRAM was tested that did not induce latchup. Previous testing has shown this technology to be sensitive to both proton and neutron-induced latchup [20], [21]. Note that at an incident effective LET of 10 MeV-cm^2/mg, the SEL cross section for this part is about 3 orders of magnitude higher than in the Samsung 4-Mbit SRAM. Previous analysis has shown that the Samsung K6X4008C1F uses a 4-transistor NMOS cell design, while the Vendor A SRAM uses a 6-transistor CMOS memory cell. SEL in the Samsung SRAM is therefore likely limited to peripheral circuitry, while a previous study of the Vendor A SRAMs suggested that latchup occurs within both the peripheral circuitry and the memory array itself [21]. No significant difference between the low-energy and high-energy data is observed in Fig. 10. This may be because, just like with ICs that are highly sensitive to SEU, it is difficult to observe rare indirect ionization events that might be energy dependent compared to numerous direct ionization events.

D. Analog Devices Analog-to-Digital Converter

Although there is no reason to believe that the effects observed in this work are specific to SRAMs, an Analog Devices AD7827 8-bit analog-to-digital converter (ADC) was also characterized for latchup in low- and high-energy heavy ion environments. Previous testing had shown this IC to be sensitive to heavy-ion induced latchup at BNL. The SEL cross section was measured at a temperature of 85° C. Fig. 11 shows the

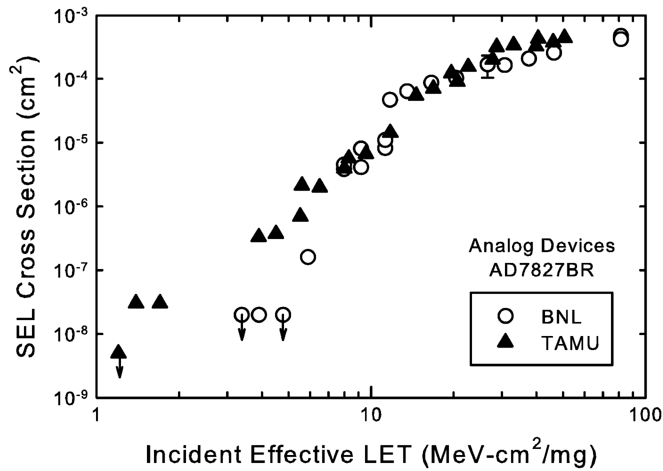

Fig. 11. Measured SEL cross section for an Analog Devices AD7827 ADC taken with low-energy (BNL) and high-energy (TAMU) heavy ions. Error bars represent standard deviation in cross section between parts tested.

SEL cross section curves for the AD7827 taken at BNL and TAMU. At BNL, the SEL threshold LET was found to be about 4 MeV-cm^2/mg, while latchup at TAMU was observed down to an LET of 1.4 MeV-cm^2/mg. Similar to most of the other ICs, the difference in measured cross section was greatest at intermediate LETs near the direct ionization threshold. For the AD7827, the high-energy SEL cross section was $\sim$10 times higher in this region than the cross section measured with low-energy heavy ions. At higher LETs, the low- and high-energy cross section curves are not significantly different.

V. Discussion

A. Physical Mechanisms

The data of Figs. 2–4 and 6–11 clearly show that significant differences can exist between SEU and SEL cross sections measured using low and high-energy heavy ions. These differences are greatest near or below what appears to be the direct ionization threshold for upsets or latchup. At LETs beyond the direct ionization threshold LET, high and low-energy SEE data appear to be in better agreement, with the low-energy data being in some cases conservative, as previously observed [8]. Of course, for cases where low-energy ions have insufficient range to reach the entire sensitive volume(s), high-energy ions will show different results throughout the LET range.

Our results here for low-LET upset and latchup are consistent with the mechanism of SEU or SEL caused by secondary particles that result from nuclear interactions within the IC [9], [11], [13][19]. The fact that blocks of the Sandia bulk and SOI SRAMs with large resistors exhibit a sharp cutoff to upsets below an incident effective LET of $\sim$15 MeV-cm^2/mg, while blocks with smaller resistors exhibit continued upsets below an incident LET of 2 MeV-cm^2/mg is very suggestive of a nuclear interaction mechanism. For devices where the direct ionization SEE threshold LET is less than about 15 MeV-cm^2/mg, reactions between incident heavy ions and silicon are sufficient to generate secondary particles capable of inducing SEE by indirect ionization, and these reactions are reasonably common for low-LET beams at both BNL and TAMU. Therefore, we observe low-LET tails in SEE cross section curves at both facilities. For devices with direct ionization SEE threshold LETs greater than about 15 MeV-cm^2/mg, interactions with high-Z materials within the IC may be required to produce particles capable of depositing enough charge to cause SEE [9], [10]. These reactions are much less common and lead to lower SEE cross sections. For low-energy heavy ions, the incident particle energy is generally not high enough to exceed the Coulomb barrier for interactions with high-Z materials such as W, and therefore no low-LET SEE may be observed at low-energy facilities for devices with high direct ionization threshold LET. At higher-energy facilities such events are still rare, but they do occur. A detailed analysis of the various interaction mechanisms at play for a given ion species and energy requires detailed nuclear interaction modeling, and is the subject of [19].

An alternative mechanism for the observed energy dependence that cannot be ruled out here is that of secondary particles generated by nuclear interactions that subsequently affect multiple sensitive nodes [13]. While this mechanism does not materially alter most of the discussion up to this point, it does offer an alternative mechanism for producing low-LET upsets in SEU-hardened SRAMs that have a high threshold LET for single-node direct ionization-induced SEU. In this mechanism, a heavy ion nuclear interaction produces one or more secondary particles that result in simultaneous charge collection at two sensitive nodes (for example the off n- and p-channel transistors in a CMOS SRAM). This charge collection reduces the effectiveness of delay-element SEU-hardening, since the ion-induced voltage transients can simultaneously propagate through both paths of the cross-coupled inverter pair. Such dual-node strikes, while rare, may result in a dramatically reduced SEU threshold LET and hence offer an alternative to high-Z interactions necessary to upset SRAMs with a high single-node SEU threshold LET.

B. Impact of Nuclear Interactions

SEUs due to nuclear interactions have been shown to increase the error rate observed in SEU-hardened 4-Mbit SRAMs operating in space by almost 3 orders of magnitude compared to the predicted rate based on ground measurements [19]. Clearly, then, nuclear interactions can play a very significant role in the on-orbit failure rates of SEU-hardened ICs. For very SEU-soft devices it has been shown that even if such effects exist, they will be difficult to detect because the direct ionization threshold LET is so low [12]. For such devices, nuclear interactions are not expected to play a significant role and mission error rates will be dominated by direct ionization events. It might be argued that nuclear interactions are important only for SEU-hardened ICs that have a relatively high direct ionization threshold LET. However, as shown in this work, it is not uncommon for commercial ICs that are SEU-sensitive to have relatively high latchup threshold LETs (on the order of 15–20 MeV-cm^2/mg). For such ICs, nuclear interactions may be important for SEL even if direct ionization dominates their SEU response. We also note that other single-event effects such as certain single-event functional interrupt (SEFI) modes or long-duration analog single-event transients (ASETs) may have higher direct ionization threshold LETs. These failure modes

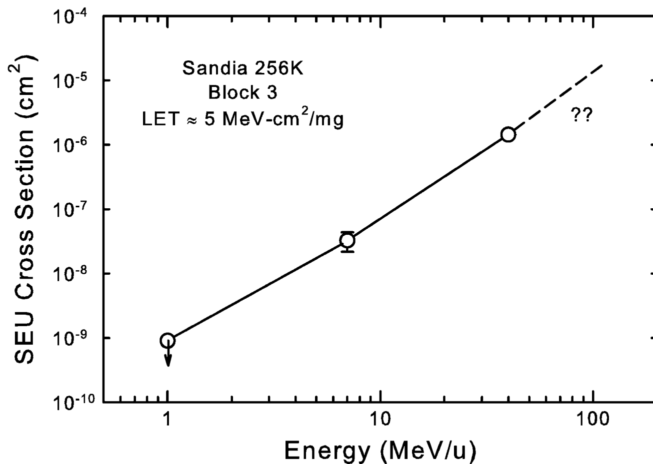

Fig. 12. Measured SEU cross section as a function of energy for Block 3 of the Sandia 256K SRAM at an incident effective LET of ~5 MeV-cm^2/mg. Error bars represent standard deviation in cross section between parts tested.

might be triggered due to nuclear interactions at lower incident LET than expected based on low-energy ground level tests.

For failure modes with high criticality, even small SEE cross sections may present an unacceptable mission risk. For example, we have conducted SEE testing of a hardened-by-design point-of-load power controller ASIC using high- and low-energy ions at TAMU and BNL. At both facilities, single-event transients in an internal voltage monitor circuit led to the triggering of the ASIC's overvoltage protection circuitry and a subsequent shutdown of the ASIC. At BNL, the threshold LET for this failure mode was ~26 MeV-cm^2/mg, while at TAMU the threshold LET was only ~15 MeV-cm^2/mg. Because of its criticality to the power system of the application, this SET sensitivity would probably have led to a redesign based on the results from either facility, but the low threshold LET at TAMU was clearly unacceptable based on system requirements. In addition, for systems utilizing a very large number of an IC (for example, memory ICs in a solid-state data recorder), it should be remembered that even a small SEE cross section can have important system ramifications [22]. We also note that in the actual space environment, particle energies significantly exceed those used in this study. As illustrated in Fig. 12, our results do not show a saturation in the increase of cross section with energy for the energy range studied here. In this figure, we plot the SEU cross section for Block 3 of the Sandia 256K SRAM as a function of energy at an incident effective LET of ~5 MeV-cm^2/mg. As suggested by this figure, it is possible that higher energy particles will result in even larger SEU cross sections for a given incident effective LET.

Assuming that the observed differences in high and low-energy heavy ion SEE response are due to nuclear interactions, our existing framework for understanding, analyzing, and predicting SEE phenomena must be significantly altered. Because upsets may be caused by secondary particles with higher LET than the primary incident heavy ion, standard techniques for plotting event cross sections against the incident ion LET must be revisited. This is clearly illustrated by Fig. 6, where plotting data without regard to different incident ion energies can lead to large discontinuities in the cross section curve. In addition, the concept of effective LET breaks down, since secondary particles don't necessarily follow an inverse cosine law based on the angle of incidence of the primary particle. This will require new methods of analyzing and plotting heavy ion data, for example as a function of energy, incident angle, and normally-incident LET rather than lumping all of these into a single parameter of effective LET. Finally, standard heavy ion error rate prediction tools currently depend on the validity of the effective LET concept and LET distribution functions based on direct ionization within a single sensitive volume. Accurate error rate predictions for ICs with significant heavy ion nuclear interaction effects will require extensive experimental characterization at multiple energies, as well as detailed nuclear physics calculations to determine secondary particle distributions [9], [11], [19]. Such calculations will also be needed to extrapolate results to the actual space environment, where particle energies can reach hundreds of GeV/u (far above the "high-energy" range studied here). These calculations will require accurate descriptions of the materials present in ICs and their locations relative to SEU-sensitive volumes. These themes are explored further in [19]. Upsets due to multiple-node charge collection mechanisms also present challenges to the concept of effective LET and standard error rate prediction tools. Methods to account for multiple sensitive volumes have been developed and will be key to accurate rate prediction when multiple-node charge collection plays a role [23]–[25].

C. Hardness Assurance Implications

In light of the significant differences in SEE response observed here as a function of heavy ion energy, any heavy ion test campaign must be conducted with a view toward evaluating whether nuclear interactions will play a significant role in the reliability of the test devices in their intended application. As a first recommendation, if a high-energy heavy ion facility is available and affordable, it should be given first consideration. At any facility, devices should be thoroughly tested at low LET using large heavy ion fluences (we suggest a minimum of 5×10^7 ions/cm^2) to determine the threshold (if there is one) at which effects are no longer observed. Note that this may require multiple devices to prevent total dose degradation of the test devices. If possible, devices should be characterized at multiple energies to explore their sensitivity to indirect ionization events.

There may be cases where scheduling pressures and economic or programmatic reasons make usage of a lower energy facility the only viable option. In such a case, the experimenter must proceed carefully. If the results at the low-energy facility show that a part is very sensitive to direct ionization effects (e.g., has a direct ionization SEE threshold LET less than 2 MeV-cm^2/mg), low-energy test data are probably sufficient because direct ionization events will dominate the SEE rate. If the low-energy test data show a direct ionization SEE threshold LET greater than about 40 MeV-cm^2/mg, low-energy data may again be adequate because even heavy ions with energies from 10–50 MeV/u are unlikely to produce secondary particles with sufficient charge deposition to cause SEE. However, it is important to remember that the actual space environment contains heavy ions with energies far in excess of 50 MeV/u, and it

is possible that nuclear interactions not present in high-energy ground-level facilities will cause failures in space. These very high energy heavy ions may also be able to cause SEU in hardened SRAMs at lower LET than expected via direct ionization into multiple sensitive volumes within a memory cell. Finally, it should be remembered that many new materials are being incorporated into advanced technologies, and these materials may lead to new sensitivities and higher nuclear reaction cross sections for events that produce high-LET secondary particles.

For devices with intermediate direct ionization SEE threshold LET (between 2 and 40 MeV-cm^2/mg), there is a high probability of energy dependence of the SEE response. These parts will require testing at a high-energy facility to establish the role of nuclear interactions in their SEE response. Devices with a direct ionization SEE threshold LET less than 15 MeV-cm^2 will likely show indirect ionization-induced effects even at low-energy facilities, but these effects will be even more pronounced at high-energy facilities. Devices with threshold LET between 15 and 40 MeV-cm^2/mg may not show any nuclear interaction-induced effects at low-energy facilities but will likely show small but non-zero SEE cross sections at high-energy facilities due to nuclear interactions. Whether these small cross sections lead to unacceptable failure rates will depend on system requirements and the criticality of the part.

VI. Summary

We have studied the impact of heavy ion energy and the role of nuclear interactions on SEU and SEL in CMOS ICs. Above the threshold LET for direct ionization-induced SEE, little difference is usually observed in single-event upset and latchup cross sections measured using low *versus* high energy heavy ions. However, below the threshold LET for direct ionization-induced upsets, we find significant differences between low- and high-energy heavy ion test results. The data suggest that secondary particles produced by nuclear interactions play a role in determining the SEU and SEL hardness of integrated circuits, especially at low LET. Although the cross sections for nuclear reaction-induced SEE from heavy ions are small, in such cases high-energy heavy ion testing may be required, depending on the overall error rate requirements of a given system. The presence of significant heavy ion nuclear interaction effects will challenge current methods for analyzing and predicting SEE phenomena.

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Physical mechanisms of single-event effects in advanced microelectronics

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Available online 12 April 2007

Abstract

The single-event error rate in advanced semiconductor technologies can be estimated more accurately than conventional methods by using simulation based on accurate descriptions of a large number of individual particle interactions. The results can be used to select the ion types and energies for accelerator testing and to identify situations in which nuclear reactions will contribute to the error rate.
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PACS: 85.30.De; 85.30.Tv; 85.40.−e

Keywords: Single-event effects; Soft errors; GEANT4; Radiation effects

1. Introduction

The passage of a single energetic particle through an integrated circuit may result in loss of data, propagation of an erroneous signal, or physical damage. The resulting single-event effects (SEEs) are caused by the portion of the incident particle's energy that is converted to charge through ionization. The charge deposited by a single ionizing particle can produce a wide range of effects, including single-event upset, single-event transients, single-event functional interrupt, single-event latchup, single-event burnout, single-event dielectric rupture and others. In general, the sensitivity of a technology to SEE increases as device dimensions decrease and as circuit speed increases [1]. These effects can be produced by direct ionization or by ionization caused by secondary particles resulting from nuclear reactions or elastic collisions. Single-event effects are of particular concern for electronics in space systems, but ground-level electronics also may be vulnerable.

As microelectronic technologies become smaller, faster and denser, it becomes important to understand the detailed mechanisms responsible for single-event effects. The circuit response depends on the amount of charge collected by sensitive nodes and the rate at which the charge is collected. The presence of high-Z metallization layers, like tungsten or copper, or materials with very large neutron cross sections, like Boron-10, may strongly impact the single-event error rate. Also, circuits designed to be immune to charge collection at a single circuit node may still be vulnerable to upset caused by charge collection at multiple nodes [2].

Particle accelerator-based SEE testing is used for qualifying parts that will be deployed in space systems and predicting error rates. However, accelerators cannot provide the full range of particles and energies that are encountered in space. In addition, the time and cost required to test over a realistic space environment would be prohibitive, even if this type of comprehensive testing were available. Hence, accelerator tests are supplemented with modeling and simulation to identify vulnerabilities and predict error rates.

Single-event effects analysis and simulation are typically based on average particle strikes, described by the stopping power, or linear energy transfer (LET), of the incident particle. However, the amount of energy deposited in the

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doi:10.1016/j.nimb.2007.04.050

sensitive device volume due to a particular event, as well as the spatial and temporal distribution of the deposited energy, may vary significantly even when considering a group of particles having the same mass and incident energy. Thus, the response of the circuit to an average event does not always produce an accurate picture of how a circuit will respond in a real radiation environment. In particular, the results will be very misleading when a significant portion of the SEEs are initiated by nuclear reactions.

In this paper,we describe a method for simulating large numbers of realistic single events using custom software tools based on the Geant4 Monte Carlo model library to describe the energy-deposition processes and technology computer aided design (TCAD) tools for device and circuit simulations. The results of these simulations show that event-to-event variation may have a significant impact when predicting the single-event error rate in advanced spacecraft electronics.

1.1. Simulating single-event effects

A comprehensive approach to simulating single-event effects requires tools that describe physical processes at the following levels:

- a quantitative description of the relevant radiation environment (particle flux, energy, etc.),
- energy deposition in the electronic materials resulting from interaction with the impinging radiation,
- conversion of energy into charge,
- charge transport and recombination in the semiconductor,
- device simulations, including the effects of charge deposited by the incident radiation, and
- circuit simulations, including radiation-induced transients.

The approach for simulating single-event effects described here is based on detailed descriptions of large numbers of individual particle interactions [3]. Spatially and temporally realistic representations of the charge deposited by individual energetic particles are used as input for device simulations [4], which in turn are used to determine the circuit-level response. By describing radiation environments using a large number of events initiated by individual primary radiation quanta and studying device response to these individual events, this approach allows us to obtain both average device response and statistical variability. Unlike the radiation-effects simulation methods commonly used, mechanisms that depend on the microstructure of radiation interactions with highly scaled and emerging devices, such as multiple bit upsets, secondary radiation from materials near active devices [5,6], microdose effects [7] and highly localized displacement damage, can be analyzed quantitatively. An overview of this approach is illustrated in Fig. 1.

In this implementation, the virtual irradiator uses Monte Carlo radiative energy deposition (MRED), a custom application based on Geant4 [8]. The virtual irradiator requires descriptions of the radiation environment, as well as the geometry and composition of the device to be analyzed. MRED is used to generate very large numbers of individual event descriptions. These events are intrinsically three-dimensional and the resulting particles may include electrons, protons, neutrons, other subatomic particles, larger atomic fragments and photons. MRED provides the amount of energy for each particle as a function of space and time, along with the fraction of the energy that results in ionization. Custom tools are used to process this information and convert it to a 3-D charge distribution that is automatically meshed for use in a device simulation tool; an example is shown Fig. 2, which was generated by simulating 1 GeV/nucleon ^{12}C ions incident on a 5-μm Si cube.

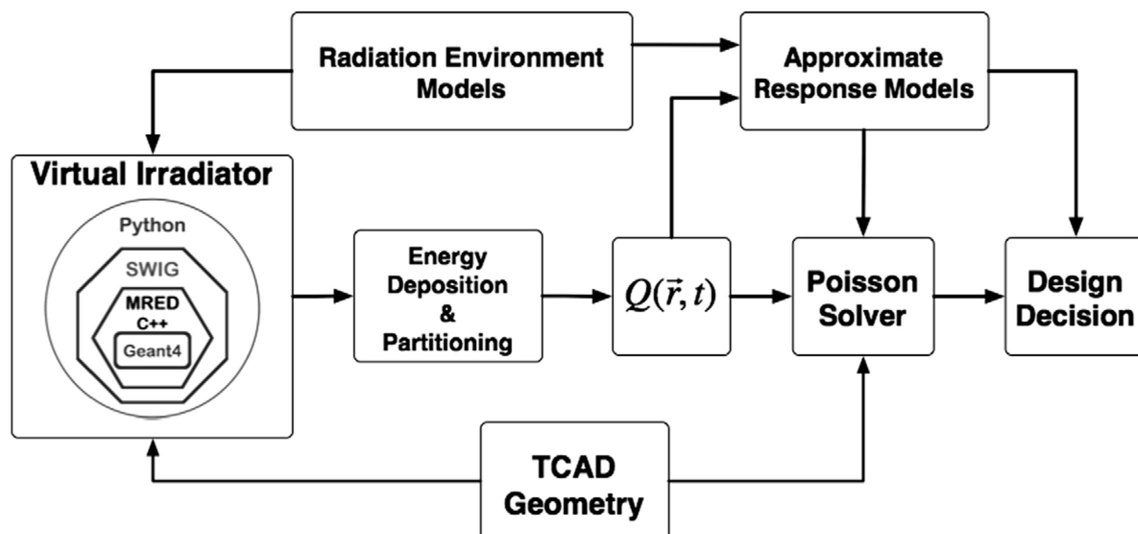

Fig. 1. Block diagram of the RADSAFE simulation environment. The MRED module within the virtual irradiator is used to generate detailed event descriptions.

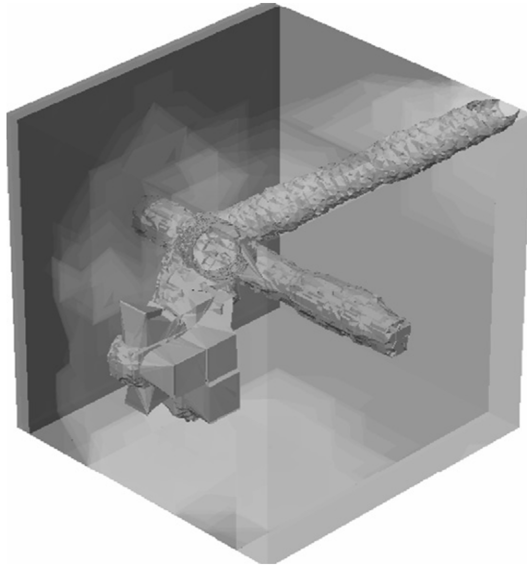

Fig. 2. Charge deposited in a Si cube by an ion-induced nuclear reaction. The iso-charge surfaces within the cube correspond to an electron density of 10^{14} cm^{-3}.

The device-simulation tool accepts the radiation-generated charge as input and provides terminal currents versus time, and if the device is embedded in a circuit, the occurrence of an upset can be determined. Analysis of a large number of these events allows determination of higher-level representations of circuit response, such as upset cross-section versus incident particle characteristics.

1.1.1. Error-rate calculations

Fig. 3 presents an example of how MRED can be used to estimate the error rate of a circuit if the critical charge required to produce an upset is known [9]. The sample used for this calculation is a silicon cube that is 30 μm on a side, with a sensitive volume consisting of a 1 μm^3 cube, centered 10.5 μm below the top surface. There is a 0.5 μm layer of tungsten just above the sensitive volume, representing the presence of a via above the sensitive portion of the circuit. The data points represent the computed cross section, $\sigma_{ED}(E)$, for depositing an energy E or greater in the sensitive volume for ions normally incident on the top surface of the sample. Results are included for 5 MeV/u Ne ions and 5, 40 and 143 MeV/u Ar ions. Each ion has an LET between 1.5 and 13.7 MeV cm^2/mg. The SEE cross section, σ_{SEE}, can be determined from $\sigma_{ED}(E)$ by evaluating it at the critical charge required to produce an upset, Q_{crit}, where the critical energy is related to the critical charge by $E_{crit} = Q_{crit} \times 22.5$ MeV/pC.

$$\sigma_{SEE} = \sigma_{ED}(E_{crit}). \tag{1}$$

The abrupt decrease in each cross-section curve below 5 MeV corresponds to the transition from energy deposition by direct ionization to that by indirect ionization. Events above the knee are due to indirect ionization. These results show that the measured σ_{SEE} of a circuit that has a high critical charge would depend strongly on the ion energy. For example, a circuit with a critical charge for SEU of 0.5 pC would exhibit a significant number of upsets if exposed to 40 MeV/u argon ions. However, no SEUs will occur if the circuit is exposed to 5 MeV/u argon ions, even though the 5 MeV/u ions have a greater LET than the 40 MeV ions (14 versus 3.8 MeV cm^2/mg). By irradiating devices with ions at several different energies (selected based on the results of the simulations), an experimenter can use accelerator testing to identify if nuclear reactions will contribute to the measured SEE cross section.

1.2. Multiple-bit upsets

The simulation approach described here also can be used to determine the number of events that deposit at least a specified amount of energy in more than one sensitive volume [10]. This is important for determining the number of multiple-bit upsets that occur in a memory or for determining the upset vulnerability of a cell that is immune to charge deposition at a single node, but can be upset by

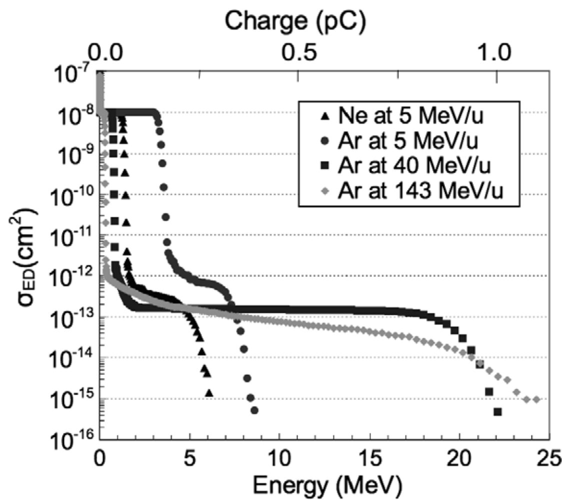

Fig. 3. Energy-deposition cross section versus energy for Ne and Ar ions incident on a block of Si containing a 1 μm^3 sensitive volume [9].

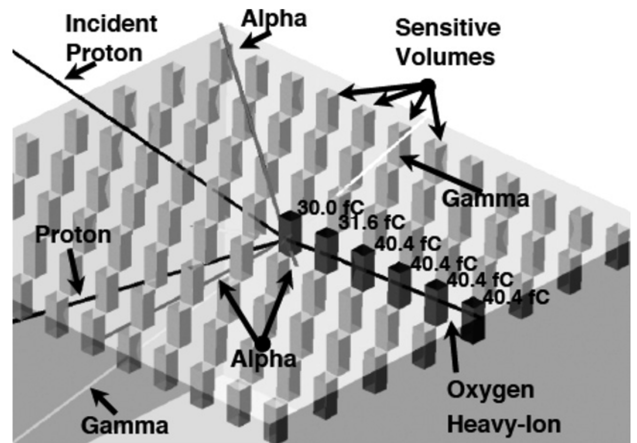

Fig. 4. Energy deposition in a 130-nm CsMOS memory due to a proton-induced nuclear reaction [10]. The oxygen ion produced by the reaction upsets six bits.

simultaneous charge deposition at two or more nodes [2]. Fig. 4 is an example of a multiple-bit upset in a 130-nm CMOS memory produced by a 63-MeV proton that causes a nuclear reaction. Each shaded box represents the sensitive volume of one memory cell. In this particular case, the incident proton enters at a grazing angle and reacts with the silicon to cause a nuclear event. Among the reaction products is a 14-MeV oxygen ion that traverses six, darker shaded, sensitive volumes. The amount of charge deposited in each sensitive volume is indicated in the figure. For typical values of critical charge, all six of the cells traversed by the oxygen ion will be upset.

1.3. Conclusions

For older technologies (minimum feature sizes $\geqslant$ 0.5 μm), it was usually sufficient to predict SEE rates through a combination of accelerator testing based on the LET of the particles and simulations that use a track structure corresponding to an average event. However, this approach may yield inaccurate results in more advanced technologies, particularly those in which particle-track sizes are comparable to transistor and cell dimensions or those with abnormal charge-collection mechanisms. More accurate SEE rates, as well as better insight, can be obtained by simulation of a large number of physically realistic events. The insight provided by the simulations can be used to guide accelerator testing and identify situations in which nuclear reactions are likely to play a significant role.

Acknowledgements

This work was supported in part by the NASA Electronic Parts and Packaging Program and DTRA. The authors gratefully acknowledge the contributions of Ken LaBel and Lew Cohn to this work.

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Implications of Nuclear Reactions for Single Event Effects Test Methods and Analysis

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***Abstract*—Simulation results for the full galactic cosmic ray environment demonstrate that current accelerator-based test methods using linear energy transfer as the engineering metric to characterize single event effects are not sufficient to capture the nuclear reaction portion of the response. Nuclear reactions contribute significantly to on-orbit single-event rates as compared to those from direct ionization induced by the primary ions. Based on these results, the applicability of current single-event test methods to predicting on-orbit event rates is examined and improved procedures are identified. For devices with critical charge values that are in the range where nuclear reactions may play a role in determining the event rate, ground-based tests should include irradiation with several types of ions of different energies to identify the contribution of these reactions to the measured SEE cross section.**

***Index Terms*—Nuclear reactions, single event effect rate, single event effects.**

I. Introduction

FOR more than two decades, Linear Energy Transfer (LET) has been used extensively as the engineering metric to assess "heavy ion" Single Event Effects (SEEs) in microelectronics. Also, the "effective" LET concept, which results from changing ion path-length through thin volumes over angle, has been so widely used that most technical papers in the field drop the word "effective" when labeling figures and discussing results. While we recognize the long history of successful engineering practice using these two metrics, recent advances in microelectronic technology require a careful evaluation of the applicability of LET to solve current engineering problems. Specifically, there is an immediate need to evaluate the use of LET rigorously in situations where nuclear reactions contribute significantly to the event rate [1]–[3].

In this paper we investigate the role of nuclear reactions when performing "heavy ion" SEE ground testing and on-orbit event-rate predictions. The computed probability for energy deposition by various ions in small volumes representative of SEE sensitive regions in modern microelectronics are compared. These calculations show that the typical test method of measuring the SEE cross section over LET is not sufficient to characterize the circuit response when nuclear reactions are a contributing factor. Additionally, we present a new Monte Carlo method to predict event rates for space radiation environments. This method is used to demonstrate the importance of including nuclear reactions in these types of calculations. Finally, we describe ground test methods to determine the contribution of nuclear reactions to a specific single event effect.

The simulation tool used for this investigation is MRED (Monte Carlo Radiative Energy Deposition, developed by researchers at Vanderbilt University). MRED is based on Geant4 [4], which comprises reliable and well-calibrated computational physics models for the transport of radiation through matter. Geant4 is a library of $c++$ routines assembled by an international collaboration for describing radiation interaction with matter. MRED includes a model for screened Coulomb scattering of ions [5], tetrahedral geometric objects [6], a cross section biasing and track weighting technique for variance reduction, and a number of additional features relevant to semiconductor device applications. The Geant4 libraries frequently contain alternative models for the same physical processes, which may differ in levels of detail and accuracy. Generally, MRED is structured so that all physics relevant for radiation effects applications are available and selectable at run time.

II. Energy Deposition Probability

To investigate the impact of nuclear reactions on the applicability of LET, we performed a series of MRED calculations to obtain estimates of the probability of depositing energy near SEE-sensitive regions for different ion species, all having the same LET. The observed relative probability of inducing a single-event effect depends strongly on the ion species and energy.

Fig. 1 presents a series of MRED calculations of the integrated probability for depositing a specific amount of energy or greater via ionization in a 10 μm $\times$ 10 μm $\times$ 1 μm embedded silicon volume for several ions all having an incident LET of 3 MeV-cm^2/mg. (See Fig. 2 the dark gray strip indicates the location of the embedded layer and is defined as the sensitive volume.) The ions selected are 35 MeV carbon $(Z = 6)$, 65 MeV nitrogen $(Z = 7)$, 105 MeV oxygen $(Z = 8)$, 8 GeV iron $(Z = 26)$, and 70 GeV zirconium $(Z = 40)$. Note that all of these ions exist in the space environment at various relative abundances. In the simulations, these ions were unidirectional and incident on the top of the 100 μm^2 layer. Going from top to bottom the ions encounter layers having a thickness of 10 μm,

Manuscript received July 14, 2006; revised October 4, 2006. This work was supported in part by the NASA Electronic Parts and Packaging Program, and the Defense Threat Reduction Agency Radiation Hardened Microelectronics Program under IACRO06-4012I to NASA.

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Digital Object Identifier 10.1109/TNS.2006.885950

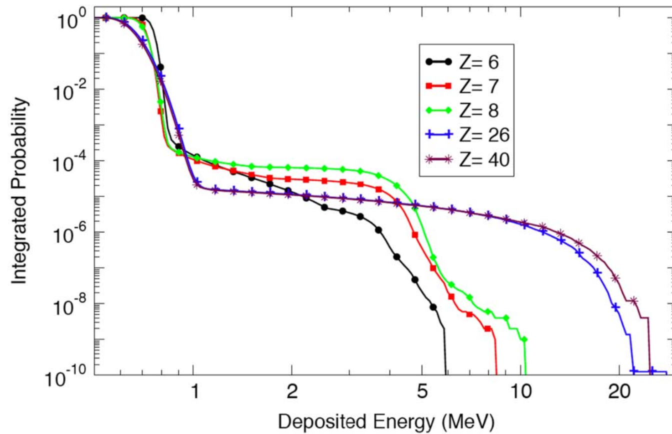

Fig. 1. Integrated probability for depositing a specific energy or greater in a 10 μm × 10 μm × 1 μm silicon sensitive volume for various incident ions. These results demonstrate the dramatic impact that nuclear reactions would have on measured SEE cross-section.

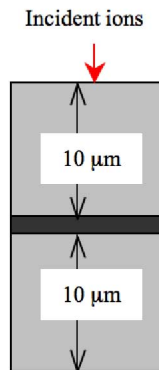

Fig. 2. Cartoon of geometry used in MRED to compute the data in Fig. 1.

1 μm, then 10 μm. The energy deposited in the sensitive volume by each incident particle was tracked and used to generate the data in Fig. 1.

Events that deposit less than 1 MeV in the sensitive volume are dominated by direct ionization from the primary ion. An ion incident normal to one face of the volume with a fixed LET of 3 MeV-cm^2/mg will deposit approximately 0.7 MeV in a 1 μm sensitive volume. Indirect ionization processes dominate for events that deposit energy larger than 1 MeV. For reference, energy deposition of 1 MeV corresponds approximately to 45 fC of liberated charge, assuming the well-known 3.6 eV/e-h pair relationship.

The integrated probability for depositing more energy than that occurring due to direct ionization alone depends strongly on the incident ion species. For example, comparing the data at 2 MeV of deposited energy, it is shown that the probability varies by more than an order of magnitude for the different particle types, even though all of them have the same LET.

The implications are dramatic for SEE testing and on-orbit rate prediction, with the relative importance depending strongly on the critical charge of the device under test. The integrated probability is directly related to the measured SEE cross section and the energy deposited is, in turn, directly related to critical charge for SEE. For example, if a circuit is susceptible to a Single Event Upset (SEU) due to direct ionization by particles with LET less than 3 MeV-cm^2/mg (energy deposition in the sensitive volume less than 1 MeV), then the SEU cross-section is independent of incident ion species. Naturally it follows that the classical analysis approach is a valid method of analyzing data for this case. However, if the circuit is not sensitive to events that deposit 1 MeV or less, but is sensitive to events that deposit greater than 2 MeV, then the SEU cross-section depends strongly (over an order of magnitude in some cases) on ion species. Note that this species dependence grows dramatically (several orders of magnitude) for events that deposit large amounts of energy within the sensitive volume.

We also note that the device geometry has a significant effect on the relationship between integrated probability and ion species, the details depend on the materials near the sensitive volume and the sensitive volume size. In particular, the proximity of metals such as tungsten or copper can have a significant effect on the energy deposited in the sensitive volume [2].

III. Importance of Direct and Indirect Ionization Processes

Particle radiation interacts with matter through two fundamental processes, electromagnetism and the strong nuclear force. LET is usually defined as the mean energy lost by an ion per unit path length in collisions with electrons of the material and is a good quantity to characterize the energy available to produce free charge. A similar quantity is adequate, with some limitations, to characterize energy lost to nuclei [7].

LET is inappropriate to describe nuclear reactions, because the underlying probability distribution is very broad, and not well described by a single mean value. Indeed, the projectile usually ceases to exist as a result of the event. For nuclear reactions the final states—the energy, direction and mass of reaction fragments, particularly heavy fragments—are critical for SEE. This is because the heaviest fragments are often very highly ionizing, both in an absolute sense, and relative to the primary ion.

Ionization and eventual thermalization of electron-hole pairs are responsible for SEEs in integrated circuits. The ionization can result either from the direct interaction of incident particles with the integrated circuit (called direct or primary ionization) or from ionization induced by scattered particles or reaction products (called indirect ionization).

The Coulomb barrier is an important metric to establish the potential for nuclear reactions between the penetrating ion and the nuclei of the atoms in a device. Equation (1), well known from nuclear physics as the energy required to bring two nuclei into contact in a head-on collision, gives the value of the Coulomb barrier as a function of the incident ion's atomic number and atomic mass, $(\mathrm{Z_1, A_1})$, and the $(\mathrm{Z_2, A_2})$ of the target nucleus

$$1.03\left(\frac{1+A_1}{A_2}\right)\left(\frac{Z_1Z_2}{A_1^{1/3}+A_1^{1/3}}\right)\mathrm{MeV}. \qquad (1)$$

The last section of this paper discusses the implications of the Coulomb barrier for ground-based testing; the current section uses the Coulomb barrier as a metric to investigate the likelihood that the space radiation environment can cause nuclear

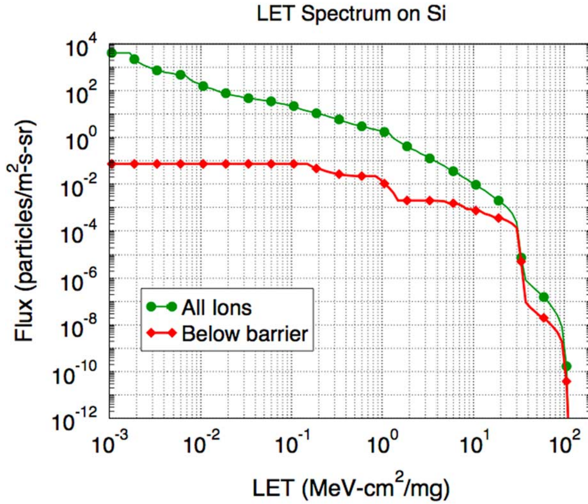

Fig. 3. Integrated space ion flux versus LET. These data show that a significant fraction of the space environment contains heavy ions that can induce nuclear reactions.

reactions. Fig. 3 shows a plot of the reverse-integrated flux of ions during solar minimum that have a specific LET or higher. Two cases are shown: 1) for all ions and 2) for all ions that have energies below the Coulomb barrier. CREME96 [8] was used to predict the detailed environment, i.e., ion flux versus energy. We developed a simple routine to parse the environment based on the Coulomb barrier between the ion and silicon.

Clearly there are a significant number of ions in the space environment that can induce nuclear reactions that lead to indirect ionization. One now asks: "Is the number sufficient to contribute to the observed on-orbit event rate as compared to the contribution to the rate other processes (e.g., direct ionization induced by the primary ions or Coulombic scattering of target nuclei)?" If so, the next question would be: "What are the appropriate ground-based test methods to identify when nuclear reactions contribute significantly to the measured SEE cross section?" The next sections will address these questions.

IV. Impact of Nuclear Reactions on SEE On-Orbit Rate Predictions

A. Previous Work

MRED fully simulates each of the processes defined above for an ensemble of incident primary particles, applies the appropriate interaction cross-sections, and records the energy loss of the primary particle and all secondary particles within a defined box. MRED has complex schemes for determining energy deposition in various volumes [9], [10]; a simple single sensitive volume is used in this paper.

MRED simulations in [11] show that the classical SEU rate prediction techniques and existing ground test methods fail to provide conservative estimates of on-orbit performance for certain device structures that include tungsten (or other high Z materials). In that work, the space environment was approximated by oxygen and helium incident ions. As a result, [10] did not demonstrate that the technique used could reproduce the expected event rates due to direct ionization, the method used on the CREME96 website. In the present calculations, we use all ions in the space environment, in their correct proportions, as determined by CREME96. The results support the conclusion from [11].

The remainder of this section describes the methodology use to predict energy deposition event rates and discusses how these predictions can be used to assess the impact of nuclear reactions on the SEE rate.

B. Rate Prediction Methodology

A Monte Carlo simulation program, such as MRED, may be viewed as a machine for determining a probability distribution by repetitive sampling. It is particularly useful when direct analytical computation of the distribution is difficult or impossible. For example, one might pose the question: "What is the probability density for an isotropic, monoenergetic flux of ions with atomic number Z and energy E_0 to deposit energy E in a specific sensitive volume?" To answer this, MRED computes the energy deposited by a large number of ions with randomly chosen initial trajectories, produces a histogram of the resulting values, normalizes the histogram to unit area, and scales by the width of the histogram bins, to obtain a discrete approximation to a continuous probability density. Subsequently, we will represent this continuous probability density as $\mathrm{MRED}_z(E_0, E)$.

In order to understand the full Monte Carlo solution for an event rate in the space environment, one must first understand how the function $\mathrm{MRED}_z(E_0, E)$ would be used in an analytic computation to infer the event rate from a knowledge of the flux distribution of the various ions. Let $\Phi_z(E_0)$ be the flux of ions with atomic number Z and energy E_0, in units, e.g., of particles/cm^2/second/sterradian/MeV. For our computations, these values were obtained from CREME96 by appropriate scaling of the original distributions, which are normalized to energy per nucleon. In the simplest computation, one would integrate the product of Φ and MRED over all energies and scale appropriately by the sample area. However, this presents a challenge for a Monte Carlo computation, due to the very large dynamic range of the flux, Φ. To deal with this, it is useful to define a new integration variable r that may be thought of as a random number generated in the usual way in the interval [0,1). A function $E_0(r)$ is chosen that maps each r into an ion energy E_0 in a way that distributes randomly selected energy values to give good sampling statistics in all regions of the flux distribution. In this way, very rare, high-energy ions are simulated as frequently as much more numerous low-energy ions. For this work we chose $E_0(r) = E_{\min}(E_{\max}/E_{\min})^r$, where $[E_{\min}, E_{\max}]$ is the range of CREME96 flux data used. The upper limiting ion energy was chosen to be 20 GeV/nucleon after tests demonstrated that energies from 10 GeV/nucleon to 20 GeV/nucleon did not contribute significantly to final results. The inverse derivative $n(E_0) \equiv dr/dE_0$ may be thought of as the density of samples at energy E_0 and is uniform on a log scale between $E_{\min}$ and $E_{\max}$ for the particular $E_o(r)$ defined above. This results in a full equation for the differential event rate of:

$$\frac{dR(E)}{dE} = \sum_{z=1}^{92} (4\pi^2\rho^2 \int_0^1 dr \left(\frac{\Phi_z(E_0(r))}{n(E_0(r))}\right) \cdot \mathrm{MRED}_z(E_0(r), E)). \quad (2)$$

Here, $\pi\rho^2$ is the sample area and a factor of 4π sterradians is included because Φ is isotropic and normalized to solid angle. The sum is carried out over all species in the space environment for which CREME96 has data. The total rate of events that deposit energy greater than E_d is related to the differential rate by:

$$R(E_d) = \int_{E_d}^{\infty} dE \frac{dR(E)}{dE}. \quad (3)$$

Each summand of (2) is computed by one or more (usually between 10 and 100) Monte Carlo processes using events whose initial weights are given by the parenthetical term $\Phi_z(E_0(r))/n(E_0(r))$, where $E_0(r)$ is an incident ion energy determined from a uniform random number in [0, 1) by the above equation. Typically a total of $\approx 10^{10}$ individual events are computed to obtain the curves presented in this paper.

To further increase the quality of the data for nuclear reaction events, all nuclear reaction cross sections are artificially increased by a factor η, which is typically chosen to be $\approx$ 200. If the primary ion in an event produces a nuclear reaction, the total weight of the event is reduced by a factor of η from its initial value given above. As long as the use of the η factor does not materially alter (by $<5\%$ xas our typical criteria) the number of events that *do not* experience nuclear reactions, the only effect on the final distribution is to reduce the variance in the region of rare, large-energy-deposition, nuclear-reaction events.

MRED is a Geant4 application, which for this work used the Geant4 binary intra-nuclear collision cascade to determine the final state for ion-ion nuclear reactions. This code has been validated by the Geant4 collaboration for ions up to atomic number $Z = 6$. Beyond this, its use is more speculative, although data have been presented that suggest that it may be used with caution up to at least $Z = 26$(Fe) [12]. The magnitude of the effects shown in this paper are dependent upon the details of this model, and will become less uncertain from systematic error as on-going efforts to improve the underlying physics are completed. However, the rates of nuclear reaction events depend on reaction cross sections, which are less uncertain than final state configurations. Therefore, while the quantitative results may improve with time, the qualitative conclusions are not likely to change. In any event, the mass, direction and energy of heavy nuclear reaction fragments are critical to single event computations and achieving statistical accuracy in predicting these quantities should be a high priority in any future research to improve the underlying nuclear physics models.

C. Impact of Nuclear Reactions on SEE Event Rate

The environment was obtained from the CREME96 website using a solar minimum geosynchronous orbit with 100 mils of Al shielding. Fig. 4 shows the integrated event rate for depositing a specific energy or greater in two MRED structures and a similar rate calculated using the CREME96 website.

The first structure (labeled *Si only* : MRED) is a silicon cube that is 50 μm on a side with a 1 μm^3 silicon cube sensitive volume (Fig. 5) that is centered on one face and 10 μm below that face (into the larger volume). The other structure (*Si with W layer* : MRED) is identical to the first, but the 0.5 μm layer of silicon just above the sensitive volume is replaced with tung-

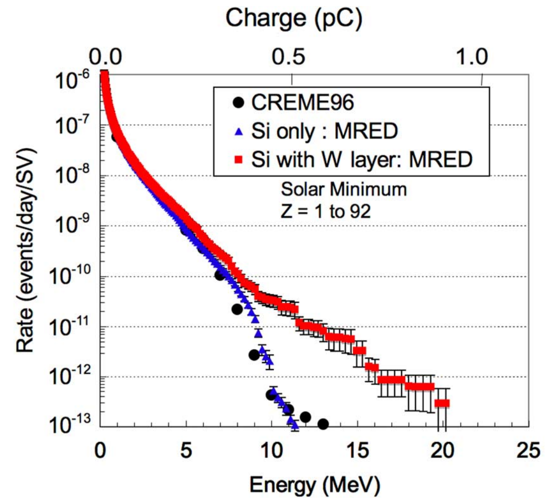

Fig. 4. Energy deposition event rate predictions for pure silicon sensitive volume using MRED (triangles) and CREME96 (circles). The squares are the event rates when a thin tungsten layer is place near the sensitive volume. MRED and CREME96 predict similar trends for energy depositions less than 11 MeV. Adding tungsten layer to this geometry shows that the nuclear reaction contribution to the event rate must be considered for circuits with threshold LETs larger than approximately19 MeV-cm^2/mg.

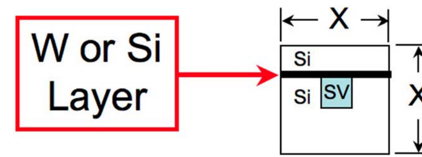

Fig. 5. Cartoon of geometry used to in MRED to compute the data in Fig. 4, 6, and 7.

sten. (Note the size of the silicon cube was made large enough so that any reaction occurring outside this volume would not result in an energy deposition within the sensitive volume.) The "critical charge" method was used to define the "cross-section parameters" for the CREME96 calculations; inputs included the solar-minimum space environment for ions between $Z = 1$ to 92, 100 mils of Al shielding, and a sensitive volume identical to that used in MRED, i.e., a 1 μm^3 cube. Also, the energy deposited was computed from the input value for the critical charge by multiplying by 22.5 MeV/pC.

There are two key results shown in Fig. 4. The first is reasonable agreement between the *Si only MRED* simulations (triangles) and the CREME96 results (circles) for energy deposition less than 11 MeV. Since the validity of CREME96 in this situation is well established, these results confirm the accuracy of the methodology used to compute the event rates using MRED.

The second key result is the significant increase in the number of events that deposit greater than about 8 MeV when the tungsten layer is added. This increase is more than two orders of magnitude for events that deposit greater than 10 MeV. We note that an ion would need an LET between 19 and 35 MeV-cm^2/mg to deposit 8 MeV in the 1 μm^3 volume, depending on its path-length though the volume. The implication is that the single-event rates of circuits with high-Z materials near these 1 μm^3 sensitive volumes and threshold LETs greater than $\sim$19 MeV-cm^2/mg will depend strongly on nuclear reactions initiated by spaceborne ions. In general, the increase in the

rate for these types of circuits will depend on the details of the geometry and the charge transport and collection mechanisms, but will be significant as compared with the direct ionization-induced rates.

V. Implication of Nuclear Reactions and the LET Engineering Metric

A. Relationship to Proton-Induced SEEs

Most researchers recognize that ion energy is the appropriate engineering metric for studying proton-induced SEEs. Proton LET alone is insufficient to cause single event effects in many technologies. Nuclear reactions, on the other hand, which deposit significantly more localized energy on the scale of microelectronic devices, can and do produce single-event effects. This is also true when direct ionization from a heavier (higher Z) ion is not adequate to induce SEEs. Indirect ionization from ion-ion reactions can result in large amounts of localized energy deposited near SEE sensitive structures.

In the next few subsections we present a case study that shows the energy deposition characteristics for various ions and energies incident on a large silicon cube with an embedded single sensitive volume (see Fig. 5). The cube was 30 μm on a side. The sensitive volume was a 1 μm^3 silicon cube, centered at 10.5 μm below the top surface. There is a 0.5 μm layer of tungsten just above the sensitive volume. The ions were randomized normally over the 900 μm^2 plane that is closest to the sensitive volume.

This study highlights some of the issues that should be considered when investigating ion-ion reaction effects. The ions used in this study are consistent with those available at existing ground-based SEE test facilities. The selection of the sensitive volume is somewhat arbitrary, but is typical of modern sensitive volume geometries.

Many device, circuit, and radiation-transport issues add complexity to the energy deposition, charge generation, and charge collection processes. These range from parasitic circuit effects, such as charge sharing among multiple nodes [13], to radiation transport concerns, such as single reaction products crossing multiple sensitive regions within a circuit [14]. These issues make the generalization of the ion-selection problem difficult. This simple single-volume example is used to provide guidance on ion and energy selection when investigating the contribution of nuclear reactions to measured SEE cross sections.

B. Computing Ground-Based SEE Cross Section

From the cumulative event rate given in (2) above, the cross section for upsets requiring a specific deposited energy $E, \sigma_{\mathrm{ED}}(E)$, follows by simply scaling by the total integrated flux. An analogous differential cross section to deposit a specific amount of energy, $d\sigma_{\mathrm{ED}} dE$, can similarly be obtained by scaling (1) by the total flux. Both cross sections are clearly sums of component cross sections for each element. These cross sections are for the omnidirectional space radiation environment.

SEE ground testing to measure the cross section is typically performed with a single ion that is monoenergetic and unidirectional ion beams. The number of upsets is determined by exposing the circuit to a specific fluence.

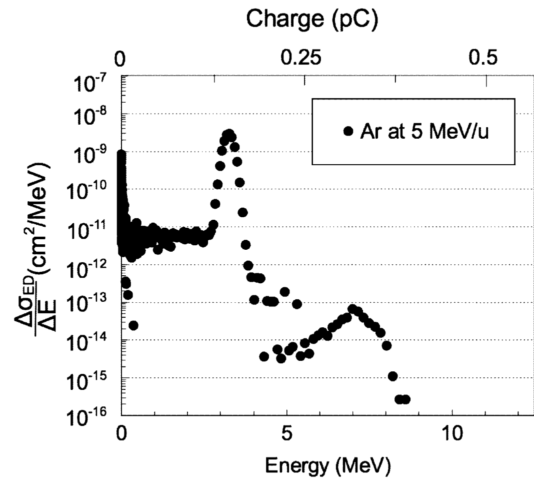

Fig. 6. Differential cross section for depositing a specific energy in a 1 μm^3 sensitive volume. The peak near 3 MeV is due to the direct ionization of the primary ion. The events to the left of this peak are due to indirect ionization events, e.g., nuclear inelastic reactions.

Equations (2) and (3) can easily be modified to account for this ground-test scenario by replacing the flux, Φ, with the fluence (the time integral of the flux), defining MRED_z to be a single direction, and eliminating the summation over various ions. $R(E)$ is replaced by $N(E)$, the number of events, and $dR(E)/dE$ is replaced by the differential number of events, $dN(E)/dE$. (Said another way, integrating $dR(E)/dE$ and $R(E)$ over time produces the differential, $dN(E)/dE$, and total number, $N(E)$, of events, respectively). The unidirectional cross section, $\sigma_{\mathrm{ED}}(E)$, and differential cross section, $d\sigma_{\mathrm{ED}}/dE$, can be determined by scaling the new $N(E)$ and $dN(E)/dE$ by the fluence. References [2], [10] provide additional details on using MRED outputs for the study of SEE effects.

Fig. 6 shows a differential energy deposition spectrum (d σ_{ED}/dE) for Ar (5 MeV/u) ions incident on the silicon cube defined above. The incident LET is 13.7 MeV-cm^2/mg and the fluence is 9.72×10^{12} ions/cm^2. The energy deposited (lower abscissa) is related to charge generated (upper abscissa) by 3.6 eV/e-h pair. The peak at 3 MeV is due to direct ionization occurring in the 1 μm^3 cube sensitive volume. Events that deposit more energy than those contained in this peak are due to indirect ionization events.

The filled circles in Fig. 7 represent the computed cross section, $\sigma_{\mathrm{ED}}(E)$, for depositing an energy E or greater in the sensitive volume for the 5 MeV/u Ar ion exposure defined above. (The next section provides more details on Fig. 7). The SEE cross section, σ_{SEE}, can be determined from $\sigma_{\mathrm{ED}}(E)$ by evaluating it at the critical charge, Q_{crit}, where $E_{\mathrm{crit}} = Q_{\mathrm{crit}} \times 22.5$ MeV/pC

$$\sigma_{\mathrm{SEE}} = \sigma_{\mathrm{ED}}(E_{\mathrm{crit}}). \tag{4}$$

C. SEE Cross Section Dependence on Ion Energy

Experiments performed using ions that have sufficient energy to overcome the Coulomb barrier between the ion and the target

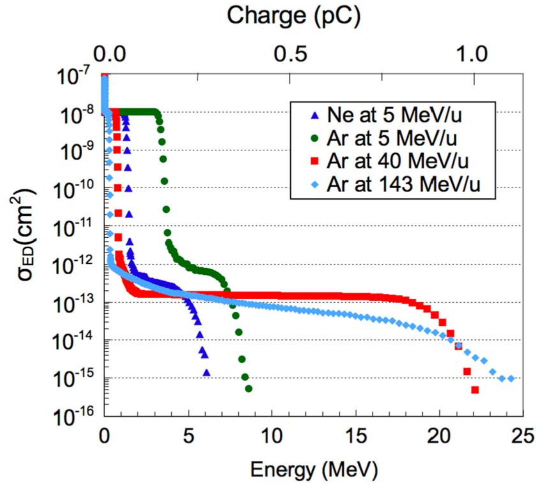

Fig. 7. Cross section for depositing a specific energy or greater in a 1 μm^3 sensitive volume. Each ion has an LET between 1.5 and 13.7 MeV-cm^2/mg. Experimental characterization the response of a circuit over ion species and energy will identify if nuclear reactions contribute to SEE cross section.

TABLE I
ION SPECIES TYPICALLY AVAILABLE AT SEE TEST FACILITIES

Ion	Energy (MeV/u)	LET (MeV-cm^2/mg)	Range (μm)
Ar-36	143	1.5	8500
Ar-40	40	3.8	1100
Ar-40	5	14	54
Ne-20	5	5.4	61

nuclei will include a nuclear reaction contribution to the measured SEE cross section. The cross section will also include a contribution from other processes like direct ionization induced by the primary ions and ionization from Coulombic scattering of target ions. The relative contribution depends on the number of sensitive volumes, cell critical charge, amount and location of high-Z materials, and the ion fluence used in the testing [2]. Next we compute a series of cross sections, $\sigma_{\rm ED}(E)$, for various ions and energies to demonstrate the ion energy dependence of the SEE cross section.

Fig. 7 plots $\sigma_{\rm ED}(E)$ for the ions listed in Table I These ion and energy combinations are typically available at SEE test facilities. Each simulation was performed with ions normally and randomly incident on the top surface of the silicon cube defined above. The equivalent fluence was between 9.7×10^{12} and 1.1×10^{13} p/cm^2. This fluence is consistent with that typically used to characterize a high-bit-count logic circuit. For example, if a simulation were required to reproduce an exposure of 1×10^7 p/cm^2 on a 1 MB memory device, then the simulation on a single sensitive volume would require approximately 1×10^{13}p/cm^2. (See [2] for a detailed discussion).

The decrease in each $\sigma_{\rm ED}(E)$ curve from 1×10^{-8} cm^2 to near $1{\times}10^{-13}$ cm^2 provides a delineation between energy deposition by direct ionization and that caused by indirect ionization. Events above the knee are due to indirect ionization events [2].

Comparison of the energy dependence of $\sigma_{\rm ED}(E)$ for the argon ions in Fig. 7 shows that experimental evaluation of a circuit that has a high critical charge would show a dramatic

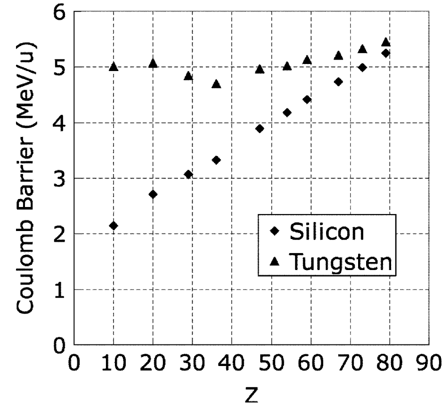

Fig. 8. Coulomb barrier computed from (1) scaled for A.

ion energy dependence of the measured $\sigma_{\rm SEE}$. For example, assuming that a 4 MB memory has a critical charge for SEU of 0.5 pC and is exposed to 1×10^8 p/cm^2 40 MeV/u argon ions, the simulation predicts that there will be nearly 40 SEUs. In contrast, the same experiment with a 5 MeV/u argon ion will result in no SEUs. Note that the ion with the lower LET results in upsets, while that with the higher LET does not.

Comparing the 5 MeV/u Ne and Ar simulation results to those for Ar at 40 or 143 MeV/u shows that the lower energy ions result in lower maximum energy depositions. The experimenter can use this fact to uncover the nuclear reaction contribution to the measured SEE cross section.

Another useful metric is the Coulomb barrier for nuclear reaction. Fig. 8 shows a plot of the Coulomb barrier (MeV/u), computed from (1) and scaled by A, between typical ions available at SEE test facilities and two different incident targets: silicon and tungsten. These data can be used to guide test energy and ion selection. Ideally, the experimenter would test using a series of ions that fall well above and well below these energies. If the circuit if the circuit upset cross section falls to nearly zero then the experimenter can assume that there is a significant nuclear reactions component to the SEU cross section for that ion species. If the SEU cross section does not decrease dramatically then direct ionization processes and/or Coulombic scattering of the target nuclei dominates mechanism for upset. One warning is that testing at energies below 3 MeV/u is often not practical because of the limited penetration depth of these ions; this is especially true for the heavier ions.

VI. CONCLUSION

A new method of estimating on-orbit event rates is presented that includes the nuclear reaction contribution. Using this method, we show that the nuclear reaction contribution to the event rate for modern circuits, particularly those containing high-Z materials with a moderate critical charge, is significant as compared with the contribution from direct ionization induced by the primary ions. The detailed response to nuclear reactions will depend on the charge collection volume structure and charge collection efficiency of that volume.

Simulation results show that current accelerator-based test methods that use linear energy transfer exclusively as the engineering metric to characterize single event effects are not suf-

ficiently general to capture the nuclear reaction portion of the response. Ground-based test methods should include a sequence of exposures that identify the contribution of nuclear reactions to the measured SEE cross section.

ACKNOWLEDGMENT

The authors would like to thank K. LaBel, J. Adams, L. Cohn, B. Sierawski, and J. Pellish for technical discussion and support during this work. The authors would also like to thank B. Borsody for editing this paper. The computational portion of this work was performed with the resources of Vanderbilt University's Advanced Computing Center for Research and Education (ACCRE).

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Simulating Nuclear Events in a TCAD Model of a High-Density SEU Hardened SRAM Technology

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***Abstract*—The interaction between a heavy ion and the overlayer materials in an integrated circuit may result in a nuclear reaction. This reaction leads to a charge generation profile that is substantially altered from the profile generated during a direct ionization event. In this work, nuclear reactions are integrated into the modeling of the SEU response of an SRAM cell using GEANT4-based simulations. The simulated transient response is compared to the response obtained using a typical heavy ion model that includes only direct ionization.**

***Index Terms*—Heavy, ion, Monte Carlo, nuclear event, SRAM, TCAD.**

I. INTRODUCTION

HEAVY ion interactions with semiconductor materials induce transient responses at the device, circuit and system levels. One area of interest are nuclear reaction products and the charge generation profiles which may be quite different from the charge generation profiles of a direct ionization event. In this paper we demonstrate a new technique, using fully-integrated and detailed physics simulation tools, to estimate the response of a CMOS SRAM cell to a nuclear reaction event that occurs in one of the metallization layers over the active part of the cell.

As an energetic heavy ion interacts with materials, there is a small probability for the ion to react with a nucleus, resulting in the generation of reaction products capable of charge-generation events that are much larger than that generated by the primary particle. Recent work has shown that reactions in the metallization and dielectric layers above the active circuitry can have a significant impact on the error rate, even for processes with just a few micrometers of material over the active region [1], [2]. The probability of a nuclear event occurring is significantly increased if the primary ion passes through high-Z materials, such as a tungsten plug—a common structure used to connect different levels of metal in a multi-layer interconnect system [2].

In this work, a complete SRAM cell, including overlayers (metal and interlevel dielectrics), was modeled using the Synopsys TCAD tool suite and combined with Monte Carlo Radiative Energy Deposition (MRED), a Monte Carlo based simulator, in order to produce realistic nuclear events. These events were used as input into TCAD electrical simulations to determine the device and circuit response to the event and then compared to a standard heavy ion model based upon direct ionization. Charge generation due to the nuclear event greatly exceeds the charge generation expected based on the LET of the primary ion and the circuit response is consequently much more significant.

Manuscript received September 16, 2005. This work was supported by the Defense Threat Reduction Agency.

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Color versions of Figs. 1, 3, and 5 are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2006.880933

II. EXPERIMENTS

The technology under study is a commercially available, radiation-hardened 4 Mbit SRAM, each cell consisting of 10 transistors, with a supply voltage of 3.3 V. This is a dual well process and the minimum drawn gate length is 0.4 μm. There are three layers of metal available in the process, which is very significant to this study due to the interaction of the materials with incoming ions. The schematic and layout are shown in Fig. 1. NMOS transistors M4 and M9 and PMOS transistors M0 and M8 are hardening devices. M5 and M10 are pull down devices with M2 and M7 functioning as pull up devices. Further detail can be found in [1].

Heavy ion test data were taken at the Texas A&M cyclotron facility with the species ranging from 523 MeV Ne with an LET of 1.79 MeV-cm^2/mg to 2000 MeV Au with an LET of 87.1 MeV-cm^2/mg. These data were taken at static operating conditions with a normally incident beam and are shown in Fig. 2. There are two regions of interest in the data: a high probability-of-upset, high LET region, and a low probability-of-upset, low LET region. The data do not show a clearly defined threshold with decreasing LET, but rather a gradual decrease in cross section as the LET decreases.

McMorrow *et al.* [3], [4] discussed a two-photon absorption technique that allows one to identify regions in a circuit that may be sensitive to single event upset. This method was applied to this SRAM circuit and a single region was identified as responsible for the upsets that occur near the upset threshold [3], [4]. The sensitive area is shown in Fig. 1 and was the focus of the simulations that are discussed below.

III. DIRECT IONIZATION SIMULATIONS

A three-dimensional (3-D) TCAD structure representative of the memory cell was created for simulation in a mixed-mode environment. The models were implemented in the ISE TCAD tool suite (now part of Synopsys), using DEVISE to describe the devices and DESSIS (a multidimensional device and circuit simulator) to simulate the electrical characteristics as well as the device response to single event strikes.

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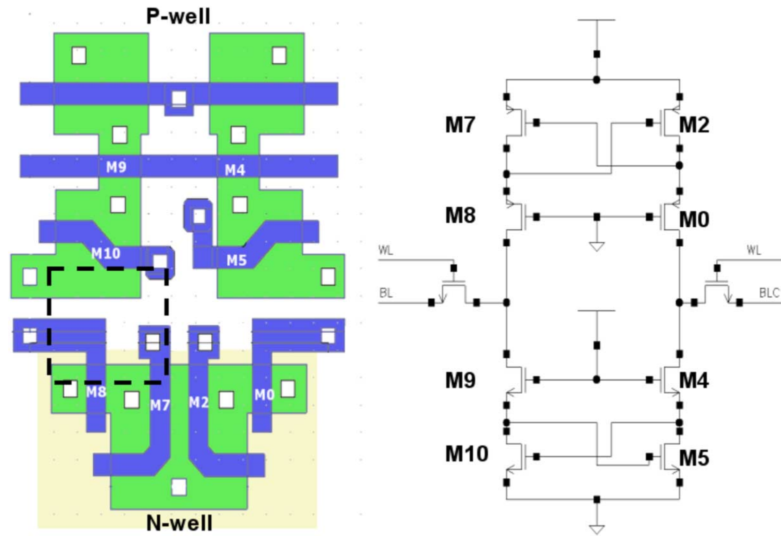

Fig. 1. Layout and schematic of the 10-T SRAM cell. The "sensitive region" shown in the layout was identified using twophoton backside irradiation and is approximately 4 μm^2.

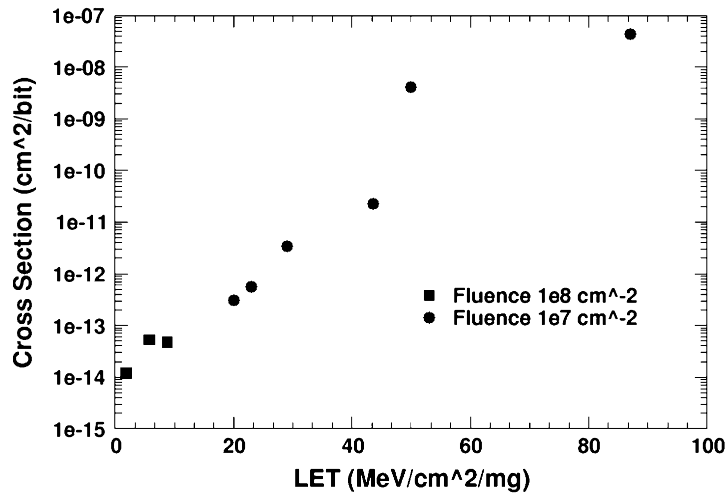

Fig. 2. SEU cross section curve for 4 Mbit memory. "Diamonds" represent a fluence 1×10^8 cm^{-2}, "circles" a fluence of 1×107 cm^{-2}. Data were taken at Texas A&M.

In Fig. 3, the 3-D model that was used in simulating the SRAM is shown. For the device simulations, the silicon substrate, gate oxides and polysilicon gates are present. The model includes all four PMOS transistors and the two pull-down NMOS transistors. The device was biased into an appropriate bias condition, with one side logic-high (the left side) and one side logic-low (the right side). Effectively, the drain of transistor M8 is the high-side bit line, and the drain of transistor M0 is the low-side bit line. The remaining circuit elements in the SRAM were modeled using SPICE BSIM3V3 models.

The simulator has two independent methods of depositing charge within the TCAD structure. The first method is a built-in function that generates a specified amount of charge per unit path length (pC/μm), over a specified distance. This method includes only charge generated by direct ionization. The second method was developed at Vanderbilt to allow for the generation of multiple charge tracks defined by complex events produced by MRED. The simulations described in this section are based on a simple uniform-LET model of the ion strike; more physical simulations using MRED are described in the next section.

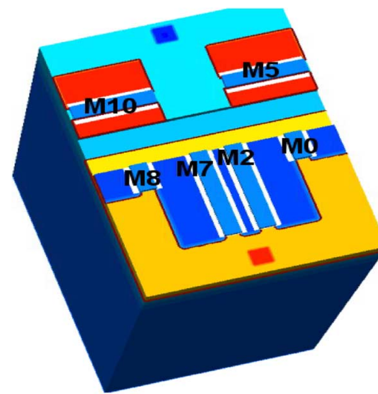

Fig. 3. Three-dimensional TCAD structure mimicking the layout of the 10-T SRAM. It includes the 4 PMOS transistors and the two pull-down NMOS transistors.

The TCAD SRAM was subjected to normally incident heavy ion particles through simulations, ranging in both energy and location over the surface of the device. The sensitive region

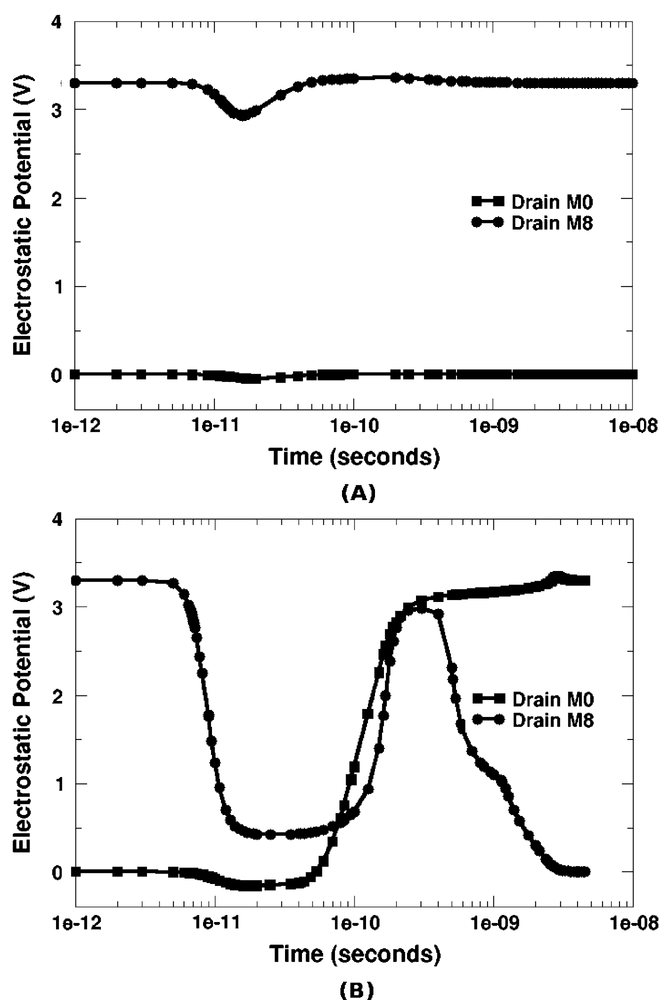

Fig. 4. Shown is the output voltage swing of the bit lines in the 10-T SRAM cell. A standard TCAD heavy ion with $\mathrm{LET} = 1.79$ MeV-cm^2/mg causes very slight voltage perturbation in (A). In (B), a $\mathrm{LET} = 50$ MeV-cm^2/mg causes severe disruption of the voltages and results in the cell upsetting.

identified in the two-photon irradiation (effectively the area contained by transistors M7, M8 and M10 — shown in Fig. 1) was verified by studying the response of the SRAM as a function of heavy-ion hit location. Simulated upsets were first observed at an LET of 50 MeV-cm^2/mg, but only for hit locations inside the sensitive region, which corresponded to the sensitive region identified in two-photon irradiation. However, the data presented in Fig. 2 show that the SRAM is sensitive to ions with an LET of less than 50 MeV-cm^2/mg. No low-LET upsets occurred for the direct-ionization, uniform-LET events.

In Fig. 4(A) and (B), the results of a heavy ion track with a uniform LET located in the middle of the sensitive region of the SRAM can be seen for LET's of both 1.79 and 50 MeV-cm^2/mg. Shown are the high (drain of M8) and low (drain of M0) side bit lines. The lower LET particle perturbs the high side bit line by less than 0.4 V, and the low side perturbation is even less. In Fig. 4(B), sufficient charge is deposited into the sensitive region by the high LET particle to force the SRAM to flip states. While these results verify that the SRAM can be caused to flip by a reasonably high LET particle, the low LET upset mechanism is not observed.

Sensitive volume depth was estimated in a series of simulations by varying the heavy ion track length from 1.0 μm to 3.0μm and monitoring the total collected charge at the drain node. The charge collection depth was observed to be roughly equal to the epitaxial thickness of 2 μm. Assuming an average upset threshold LET of 50 MeV-cm^2/mg (as derived from TCAD simulation), the critical charge for upset (Q_{crit}) was calculated as 1.13 pC. This simulated threshold LET corresponds approximately to the LET at which there is a large increase in upset cross-section in the experimental data. These results show that considering only direct ionization does not describe all of the upset mechanisms that may occur in this memory cell We address this in the next section by extending TCAD simulations to include detailed descriptions of events resulting from nuclear reactions.

IV. Indirect Ionization Results

The existence of low-LET upsets was hypothesized to arise from secondary particles of high stopping power, which occur following nuclear reactions between the primary ion and the irradiated material. In order to study these types of events, we use MRED. It is a Geant4 [5] application program that includes additional physics processes, developed at Vanderbilt University to model screened Coulomb collisions [6]. The structure of MRED is such that all of the electromagnetic and hadronic physics in Geant4 that are relevant to microelectronic applications can be selected at run time. This includes four different electromagnetic interaction models, four ion-ion collision hadronic models, four models for nucleons, and basic interactions of elementary particles. MRED can alternatively parse and process complex device structures defined by TCAD geometry tools (the Synopsys suite of tools). Several output formats are available, all of which are structured as Mathematica objects for higher level processing. Version 7.0 of Geant4 was used to build the version of MRED used in this study.

Using vendor-supplied layout files, a simulation structure was built that included the active portion of the memory cell (shown in Fig. 3), plus all overlayer materials. This structure was built using the Synopsys tools, however, the format is able to be input directly into MRED, ensuring the seamless flow of information from the TCAD tools to MRED and back to the TCAD tools that is needed in order to preserve the geometry of the SRAM and the location of the sensitive region. In Fig. 5, the polysilicon gates, tungsten plugs and three layers of aluminum metallization residing above the silicon are shown. Note that the insulating and passivating layers are present in the structure used for MRED simulations, but are not shown in the illustration for clarity. It should also be noted that this structure is used for MRED simulations, however the presence of the overlayers is not required for the TCAD device simulations.

Charge deposition simulations were performed in MRED with the complete structure as the target. A mono-energetic beam of 523 MeV^{20}Neon ions was randomized over the structure at normal incidence. This particular ion was chosen as the test case because it represented the lowest LET (1.79 MeV-cm^2/mg) that caused upset in the SRAM. The results of 1×10^8 simulation events are shown in Fig. 6 and are represented by a differential charge spectrum. The total energy

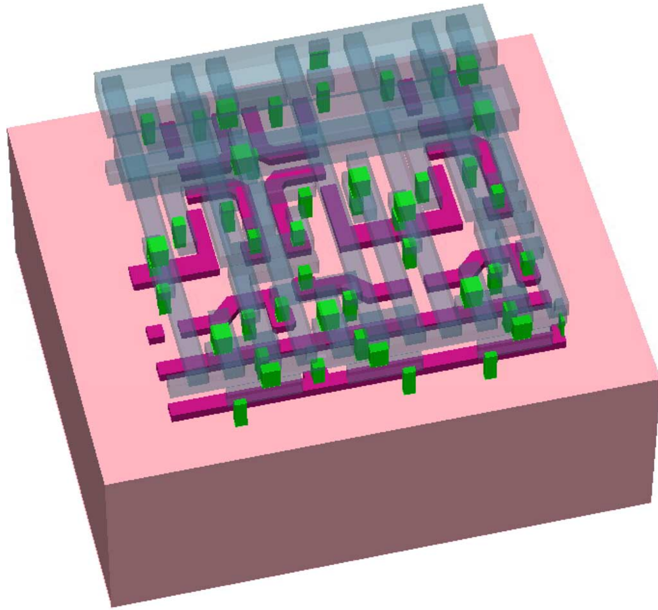

Fig. 5. Complete model of a fully detailed structure entailing the silicon and all overlayer materials. Shown are aluminum metallization, tungsten plugs, polysilicon gates, and the silicon.

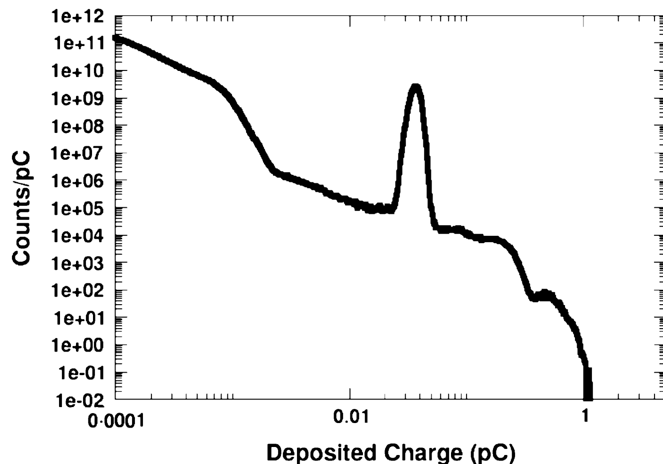

Fig. 6. Histogram of number of particles/pC versus deposited charge shows an average $\mathrm{LET} = 1.79$ MeV-cm^2/mg while also showing a peak deposited charge at about 1.1 pC, or comparable to the amount of charge deposited by a primary ion with $\mathrm{LET} = 50$ MeV-cm^2/mg.

deposited in the sensitive volume for each of the particles was binned and used to generate the charge deposition spectrum.

MRED computes the energy deposited in the volume and the deposited charge is calculated by dividing this by 22.5 MeV/pC. The data in Fig. 6 yield an average LET of 1.79 MeV-cm^2/mg. However, the data also show that there are some events that deposit more than 1 pC of charge. In [1], Warren showed several similar figures, with varying overlayer materials that resulted in significantly different amounts of deposited charge. The stacks with metallization showed a deposited charge of slightly over 1 pC, while the stacks without metallization showed maximum deposited charge that is about half as much. The high-Z overlayers both increase the probability of nuclear reactions occurring, while also increasing the amount of possible charge that can be generated.

The important physical processes for charge generation are: ionization by the primary ion, nuclear elastic and inelastic reactions between the primary ion and target element, and screened Coulombic scattering. The events occurring in the peak around 35 fC are due to direct ionization by the primary ion; the high-energy deposition events are due to a combination of direct ionization and indirect ionization events. Indirect ionization is defined as any event that produces ionization within a volume by means other than direct ionization induced by the primary ion. For example, the primary ion interacts with a silicon atom and produces several reaction products. Each reaction product can deposit energy, or charge, within the volume. The charge deposited by the primary ion is direct ionization, while that deposited by the reaction products is indirect ionization. Events other than direct ionization also contribute to the charge deposition spectrum shown in Fig. 6 and the events depositing the most charge are equivalent to a primary ion with an LET of approximately 50 MeV-cm^2/mg (calculated using the charge and the path length through the sensitive volume). Effectively, the primary ion with an LET of 1.79 MeV-cm^2/mg can be involved in an indirect ionization event that deposits as much charge as a primary ion with an LET of 50 MeV-cm^2/mg.

MRED allows the user to specify a sensitive volume within the simulation structure, which is simply the volume specified in the previous section. The TCAD device simulations showed that slightly more than 1 pC of charge deposited in the sensitive volume can cause the SRAM to upset. A filter was set in MRED, which saved all information pertaining to any events stemming from the primary species of 523 MeV^{20}Neon that deposited at least 25 MeV in the sensitive volume. Using 22.5 (MeV/pC) as the conversion factor (assuming 3.6 eV per electron-hole pair), these events will result in the deposition of at least 1.1 pC in the sensitive volume.

V. TCAD Simulations With Nuclear Events

At Vanderbilt, additional code has been developed to allow the simulation of these nuclear reaction products. The code takes the physical description of the nuclear event, and creates a mesh suitable for device simulation. The code is also used to generate the correct number of electron-hole pairs during the simulation that represent the charge generated by the nuclear event.

The description of a nuclear reaction and its products is the output of MRED, or the input for device simulation in the form of energy deposited as a function of location and time. The results of a nuclear event in a device simulation can be seen in Fig. 7. Similar to the previously described results, the high and low bit lines are shown, and in this particular instance, enough charge is deposited to cause the SRAM to flip states. This particular nuclear event deposited 25 MeV into the sensitive region of the SRAM, or 1.1 pC of charge, and it occurred as a response to a primary ion with $\mathrm{LET} = 1.79$ MeV-cm^2/mg. This event also originated in a tungsten plug directly above the sensitive region.

VI. Conclusion

The simulations demonstrate that the presence of tungsten and other materials over the sensitive region of the circuit can interact with the primary heavy ion being used during irradiation

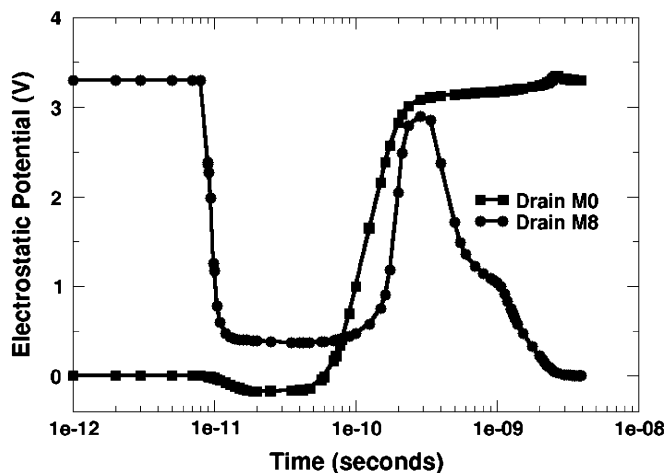

Fig. 7. Shown is the output voltage swing of the bit lines in the 10-T SRAM cell. The reaction products of 523 MeV neon ($\mathrm{LET} = 1.79$ MeV-cm^2/mg) resulted in the deposition of 25 MeV, or 1.1 pC of charge, in the sensitive region, causing the cell to upset.

to produce secondary particles whose combined stopping power in the sensitive volume exceeds that of the primary species.

In this study, we reviewed the scattering products of 523 MeV neon on materials contained within a specific SRAM process and found that the most significant events arose from interaction with tungsten, a commonly used interconnect material. The most extreme events deposited 25 MeV of energy in the sensitive volume; a factor of 27 greater than that calculated by the standard stopping power of 23 MeV neon in silicon for the same volume

A standard interface between the MRED toolkit and the TCAD simulation software was developed and used to demonstrate that the high-energy events were sufficient to cause SEU in the circuit under study. Consequently, we have shown that SEU may still be measured under circumstances in which the stopping power of the primary species is substantially below the upset threshold. This effect should be considered when interpreting SEU broad-beam data, especially when small cross sections are measured which cannot otherwise be attributed to inter-cell variations in SEU upset threshold.

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Task #2: Radiation Effects in Texas Instruments CMOS Devices – related articles.

Effect of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron CMOS

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***Abstract*—Simulations are used to characterize the single event transient current and voltage waveforms in deep submicron CMOS integrated circuits. Results indicate that the mechanism controlling the height and duration of the observed current plateau is the redistribution of the electrostatic potential in the substrate following a particle strike. Quantitative circuit and technology factors influencing the mechanism include restoring current, device sizing, and well and substrate doping.**

***Index Terms*—Field funneling, potential modulation, pulse shape, pulse width, single event, TCAD.**

I. Introduction

THE fraction of the area of an integrated circuit affected by an ion strike has changed as device feature size has decreased with technology scaling. For example, in CMOS technologies where the minimum feature size is on the order of a micrometer, the single event charge cloud generated due to a heavy ion strike predominately affects only the node that is hit, as shown in Fig. 1(a). The changes in carrier concentrations result in a distortion of the potential distribution that is sometimes described as a *funnel* and charges from the entire funnel region contribute to the transient waveform [1]–[5]. In these larger devices, changes in potential in the region of interest for most single-event strikes are confined to the drain-substrate junction of the hit transistor. For deep submicron technologies however, a single event strike may produce a charge cloud over a region that encloses the entire hit device, nearby well contacts, and possibly nearby devices, as shown in Fig. 1(b). This simultaneously affects the electric fields and potentials associated with all the nodes contained within the charge cloud. Due to the interaction of the potential modulation process with multiple contacts or junctions, a change in the current pulse shape is observed in highly scaled technologies, both experimentally [6]–[8] and through Technology Computer Aided Design (TCAD) simulations [9], [10].

Manuscript received July 20, 2007; revised September 24, 2007. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA)/Boeing Radiation Hardened by Design (RHBD) Program.

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Digital Object Identifier 10.1109/TNS.2007.910863

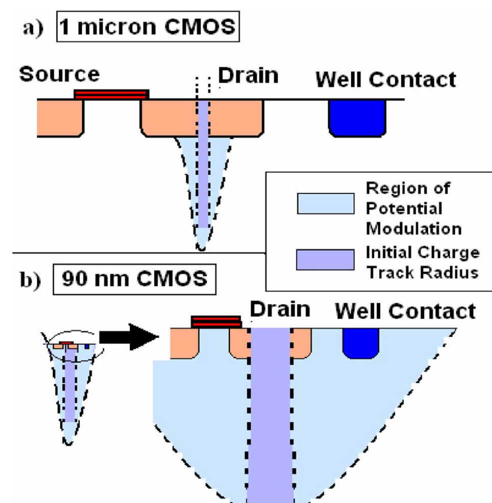

Fig. 1. Relative range of the "field funnel" in a 1-micron and a 90 nm technology. Top figure (a) shows the "funnel" creating a potential perturbation only on a small portion of the drain. Bottom figure shows a strike with the same radius covering the source, drain and well contact.

A "plateau" in the single event current pulse following the prompt response has previously been observed and explained in [9], [10] for both bulk and SOI CMOS processes. In this paper the plateau is studied using mixed-mode (combining TCAD and compact model) simulations to study the fine structure of a single event current pulse, properly accounting for device loading and complementary device restoring currents. We characterize the pulses in 130 and 90 nm bulk CMOS devices, operating at $V_{dd} = 1.2$ V and 1 V respectively, in terms of circuit parameters and substrate profiles, and propose mechanisms explaining the detailed features of the plateau. Earlier simulations have shown that the limit set by the restoring current drive loading the irradiated device determines the presence of the plateau [9]–[11]. Our simulations suggest that the specific levels of the plateau must be refined by taking into account the boundary condition on the potential modulation imposed by a well contact.

Our discussion of the plateau effect falls into three parts: We first discuss the current and voltage waveshapes in detail for low and high-energy particle strikes. Second, we examine the circuit factors that influence the plateau formation. Finally, we look inside the device to examine how the potential redistribution caused by the charge generation affects the drain potential and charge collection.

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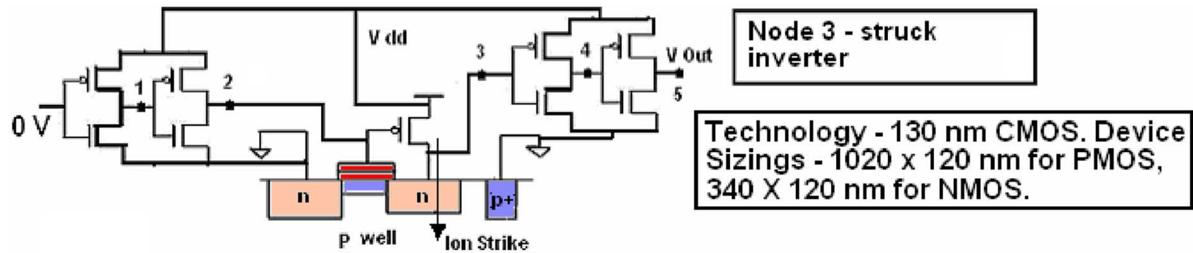


Fig. 2. 5-inverter chain for simulation setup.

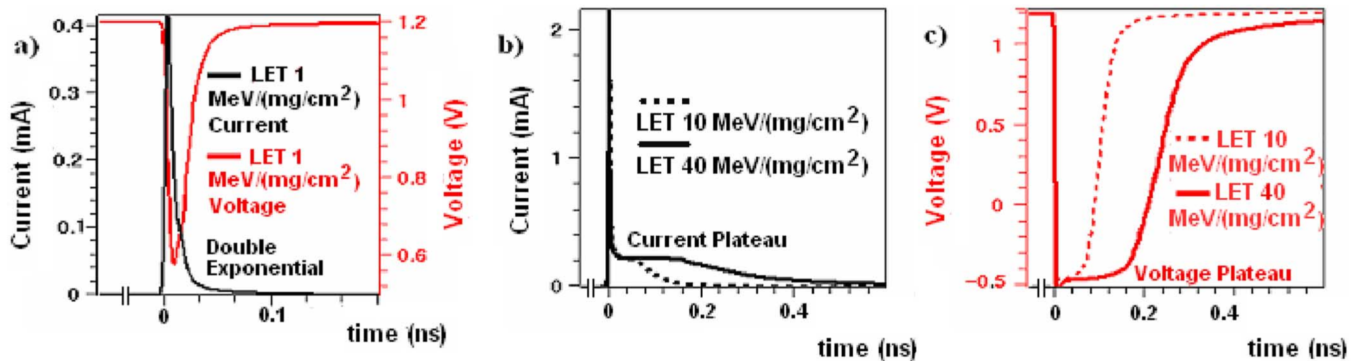


Fig. 3. Distinctly different pulse shapes for (a) an LET of 1 MeV/(mg/cm^2) (double exponential) and (b)–(c) one of 10 MeV/(mg/cm^2) or above (exponential plus plateau). (b) Hit current transient. (c) Voltage transient. Current plateau is equal to the drive of the restoring PFET at $V_{ds} = V_{dd}-$ Plateau Voltage.

II. Major Pulse Shape Features

Mixed-mode simulations were performed using Synopsis' Dessis simulator [12]. Three-dimensional TCAD device models and SPICE compact models for the simulated devices were calibrated to a Process Design Kit (PDK). Some of the results presented here are for the high performance version of a commercial 90 nm technology, others for a 130 nm process. The simulations reported in this work were carried out on a 5-stage inverter chain with the n-channel transistor of the middle inverter modeled in TCAD, as shown in Fig. 2. The third inverter NMOSFET was the device that was irradiated and the radius of the heavy ion charge filament was 50 nm. A radius of 30 nm gave very similar results.

Current and voltage waveforms from mixed-mode TCAD simulations of the inverter chain of Fig. 2 are shown in Fig. 3. At a low LET of 1 MeV/(mg/cm ^{2}), the current pulse has a double exponential shape, as shown in Fig. 3(a). At an LET of 10 MeV/(mg/cm^2) or higher, however, the current pulse has a high peak current for a few picoseconds, followed by a distinct "plateau" region where the current is relatively constant for a much longer time than that of the initial prompt peak response (Fig. 3(b)). The corresponding voltage curve reveals that the length of the plateau in the current waveform, rather than the prompt response, determines the actual voltage pulse width (Fig. 3(c)). The plateau voltage can be negative, depending on factors such as contact size, location, and doping. (In this paper only topside contacts are used.) The plateau current equals the drive current of the restoring PFET at $V_{ds} = V_{dd}$-plateau voltage, as shown earlier by simulation results [9]–[11].

TABLE I
Device Sizes for Inverters Used in Fig. 4

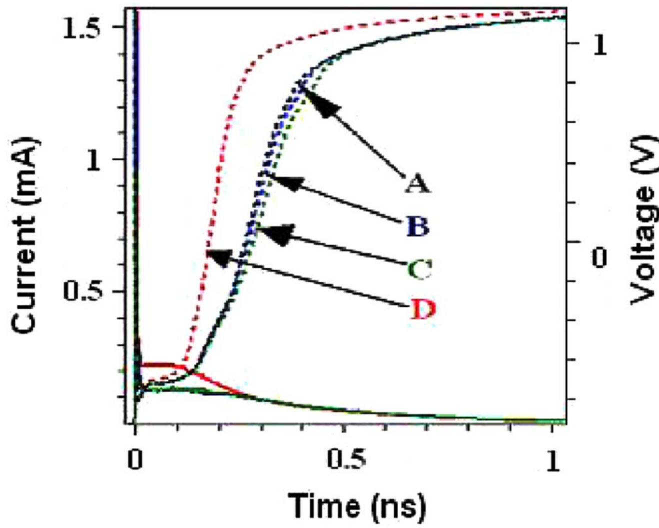
Case	Hit Inverter (nm)	Loading Inverter (nm)
A	NMOS- 240 x 120, PMOS- 600 x 120	NMOS- 240 x 120, PMOS- 240 x 120
B	NMOS- 240 x 120, PMOS- 600 x 120	NMOS- 400 x 120, PMOS- 1000 x 120
C	NMOS- 240 x 120, PMOS- 600 x 120	NMOS- 240 x 120, PMOS- 600 x 120
D	NMOS- 240 x 120, PMOS- 1000 x 120	NMOS- 240 x 120, PMOS- 600 x 120

III. Circuit Effects of Load and Restoring Device on Shape of the Plateau Region

The circuit parameters affecting the single event response of a circuit node are the nodal capacitances and the size (drive current) of the devices responsible for restoring the struck node to its original voltage. Two different sets of TCAD simulations were carried out to explore these parameters using the inverter chain shown in Fig. 2.

In the first set of simulations, the devices in the inverter being hit (3rd inverter) are kept the same size as the original inverters, but the load capacitance is changed by changing the size of the fourth inverter (Table I). For the second set of simulations, the size of the restoring PMOS transistor (p-channel transistor in the 3rd inverter) was made smaller or larger, while the fourth inverter remained at its original size.

The effects of loading capacitance on the voltage pulse width are minimal, as shown in Fig. 4. However, the restoring PMOS transistor size has a significant effect on the voltage pulse measured. Consider the portion of the SET between 50 and 100



Case	3rdInverter PMOS pull up	4th stage inverter sizing	Case	3rdInverter PMOS pull up	4th stage inverter sizing
A	Matched	Small	C	Matched	Identical
B	Matched	Large	D	Large	Identical

Fig. 4. Effect of node capacitance and restoring PMOS drive current on pulse width of struck node from a two-inverter simulation with struck NMOS in TCAD. Dimensions of devices are shown in Table I. All lengths are in nanometers.

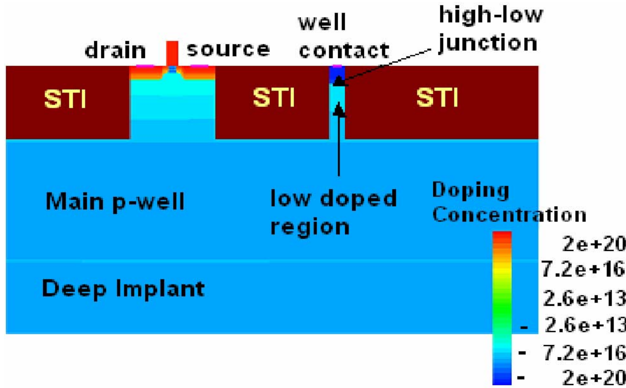


Fig. 5. Well contact, well, and substrate doping profile of the simulated 3-D TCAD structure, along a cut line taken at the center of the drain.

ps. The gate capacitance for all cases remains relatively small (about 5 fF to 20 fF) and the changes in node voltage also remain small during the plateau interval. As a result, the current for charging or discharging the capacitor during the plateau interval, C × (dV/dt) ∼ 10 nA, is very small. On an inverter node, there are three current components: SET current, load capacitor current, and restoring current. Since the capacitor current is very small, the SET transient current (roughly constant during this interval at about 100 μ A), must flow through the restoring PMOSFET.

IV. Device Mechanism Effect on Plateau Waveshape

As Fig. 1 shows, one factor differentiating the response in deep-submicron technologies from larger structures is that the entire drain and well contact region is small enough so that the carrier concentrations in and around the transistor are significantly altered by the charge generated by the heavy ion almost

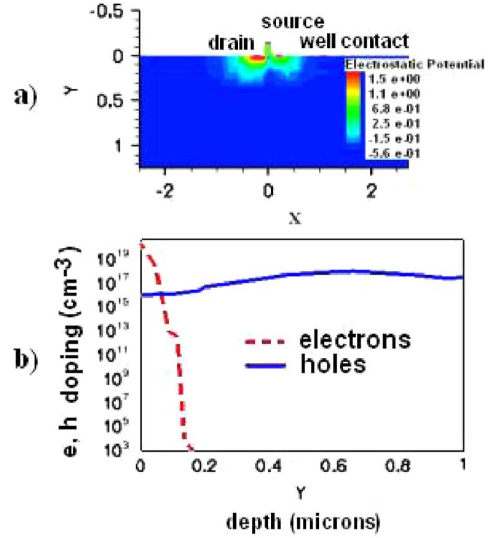


Fig. 6. Equilibrium contour plot of electrostatic potential. There is a high potential gradient at the source-well and drain-well junctions, and very negligible potential gradient at the well contact. Doping levels of the drain-body junction are also shown.

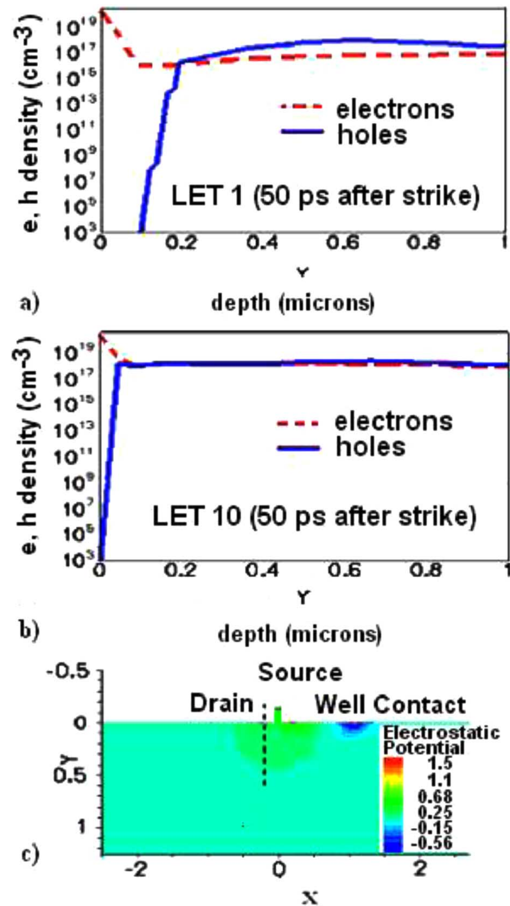


Fig. 7. Density of charge in the metallurgical junction region exceeds background doping for (b) LET 10 MeV/(mg/cm^2), unlike in the case with (a) LET 1 MeV/(mg/cm^2). (c) Potential pushout from the drain-substrate junction to the highly doped well contact, 25 ps after a strike of LET 10 MeV/(mg/cm^2).

immediately following the strike. The strike radius used for the single-event simulations was 50 nm, the device width was 340 nm, the drain length was 300 nm, and the distance to the well contact was less than 1 μ m. Simulations show that 20 ps after

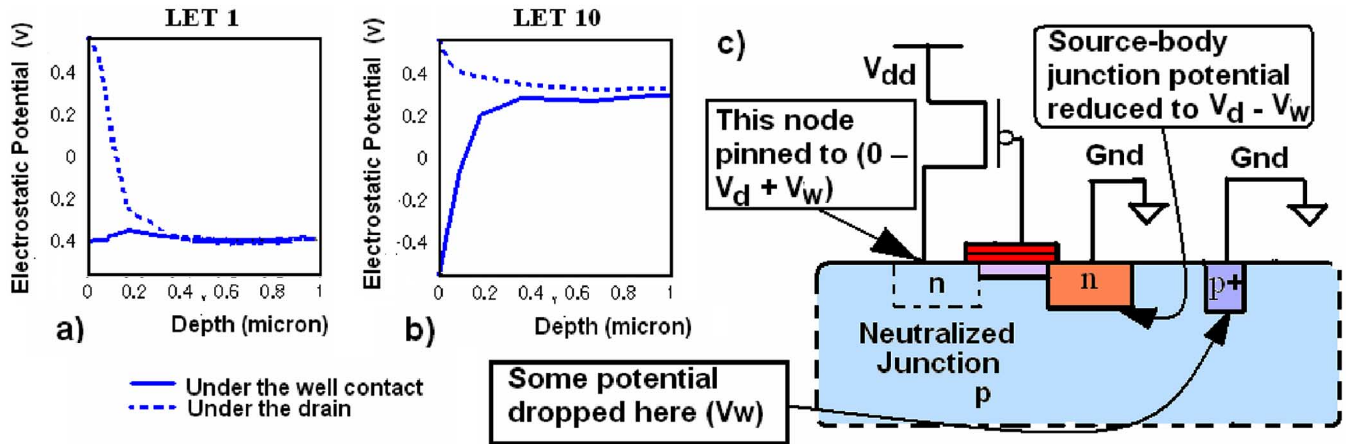


Fig. 8. Diagram of the mechanism of potential collapse and 1-D plots of potentials under the drain and well contact for LET= 1 and 10 MeV/(mg/cm^2) (25 ps after strike). Cartoon (circuit explanation) potentials referenced to Fermi level in metal ($V(x) = E_{fm}/q - \phi_s(x)$)). In 1-d plots, potentials referenced to E_i. ($V(x) = \phi_s(x) - E_i/q$) As we go from LET 1 (a) to 10 (b), region of high potential drop can be seen to shift from drain to well contact. Drop at the well contact affects the drain terminal voltage (c).

the strike, the entire drain and contact region are enclosed in a mobile charge carrier cloud whose hole and electron concentrations exceed the well and substrate doping concentrations, as shown schematically in Figs. 5–7. Fig. 5 shows the device and substrate doping profiles of the simulated 3-D TCAD structure along a vertical cutline at the center of the drain. Electrostatic potential and the 1-D views of the doping in the drain-body junction region are shown in Fig. 6.

After an ion strike, the depletion region between the drain and the well is neutralized by the abundance of free carriers, and the conductivity of the well region becomes very high. Consequently, the potential becomes nearly uniform in the entire region of the drain and the P-well (except for the source-substrate junction, which is pinned) all the way to the P-well contact, where the $P+$ doping of the contact is still above the concentration of the mobile charge due to the strike and can sustain a voltage drop. A similar effect has been observed previously in SiGe heterojunction bipolar devices [13].

This effect is illustrated in Figs. 7 and 8 for LETs of 1 and 10 MeV/(mg/cm ^{2}). In the low LET case, the mobile charge concentration produced by the strike is lower than the doping concentration (Fig. 7(a)). As a result, the potential drop can be sustained between the N-drain and the P-well resulting in the conventional field-driven charge collection (Figs. 7(a) and 8(a). Such charge collection will yield a double-exponential current pulse shape. One-dimensional (1-D) cuts of the potential normal to the drain surface and the P-well contact surface indicate that the drain junction is sustaining a potential drop. Conversely, in the LET of 10 MeV/(mg/cm^2) case, the mobile charge density is higher than the doping concentration, (Fig. 7(b) so the drop across the drain junction is reduced and the drop across the contact doping increased, resulting in "push-out" of a nearly constant potential to the P-well contact region. The 1-D cuts show that the potential is nearly constant under the drain, but that a significant voltage drop occurs at the $P+$ contact to the P-well (Figs. 7(c) and 8(b).

The high potential drop (high electric field) at the highly doped P+ contact in the NMOSFET is very similar to the fields near junctions and contacts leading to second breakdown in power diodes, as described in [14] and [15]. Application of very high voltages to a power diode leads to injection of charges into the low-doped regions, which causes the high-field region to migrate from the junction to the highly doped contacts. During an NMOS single event the same situation arises due to elimination of charge gradients (and hence, electric fields) from the intermediate region between the drain and well contact by the excess deposited charge. A simplified 2-D representation of this effect is given in the Appendix.

In the case of deep-submicron CMOS, since the 1-D cut in Fig. 8(b) shows the potential to be nearly constant underneath the drain for a high LET case, the potential in a region of the well close to the source-substrate junction translates to the potential at the drain terminal. In the NMOS device the path for the shift of potential is from the $N+$ source, through the P-well, to the $P+$ well contact. The drop of potential at the well contact affects the potential of the source-substrate junction. If a potential of V_d is present across the equilibrium source-substrate junction, then an increase in the $P+$ contact potential of magnitude V_w reduces the built-in potential of the source-substrate junction to $V_d - V_w$, because both the well contact and the source are pinned to ground, so the total potential drop in this path must be zero. Therefore, the drain terminal of the irradiated transistor, which now has very little drop of its own, is pulled down to $V_d - V_w$ below the ground, as shown in Fig. 8(c). Consequently, if the NMOSFET drain voltage is pinned during the plateau, and the gate voltage of the restoring PMOSFET is fixed at ground during the event, then the gate-to-source and drain-to-source voltages of the PMOSFET are constant. Thus, the PMOSFET current is constant throughout this interval, resulting in the observed plateau in the current waveform.

The mechanism of the potential modulation and saturation of the potential push out against a very heavily doped well contact is similar to the field-funneling model developed by Hu and Hsieh [1], [16]. Validity of Hu's model requires a lightly doped substrate on the side of the funnel extension into the substrate. The situation described here can be visualized as a funnel reaching a hard boundary due to the highly doped contact, and all the strong fields accumulating at the funnel boundary.

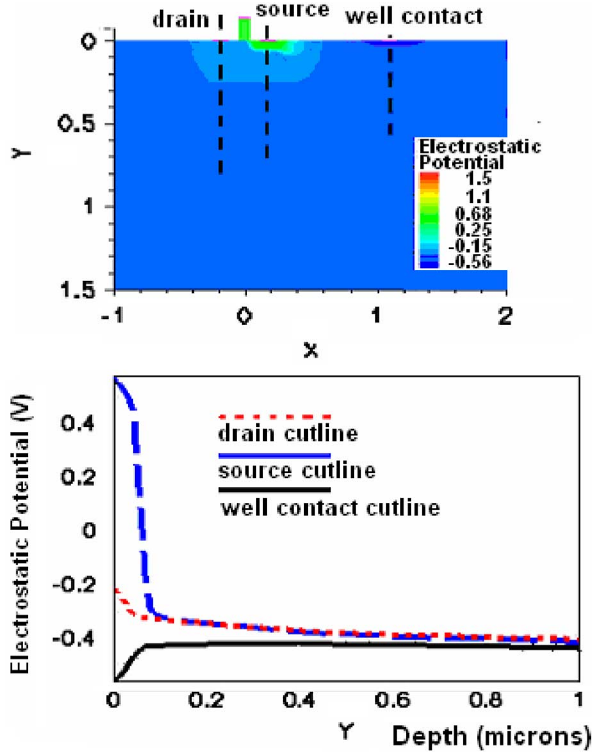


Fig. 9. Contour plot of potential (top) and 1-D profile of potential (bottom) underneath the drain, source and well contact for a heavily doped (5×10^{17} cm^{-3}) substrate. Negligible potential drop at well contact leads to high source-substrate junction potential, which translates to a large excursion of the drain voltage below the rail (Table II). Doping depth of well contact is 80 nm. Cutlines have been obtained 25 ps after a strike of LET 10 MeV/(mg/cm^2). Potentials are referenced to E_i, i.e., $V(x) = \phi_s(x) - E_i/q$.

V. Effect of Substrate and Well Contact Doping on Plateau Level

To test the hypothesis regarding the relation of the "plateau" potential to the potential drop at the well contact (as demonstrated in Fig. 8(c), we consider the results from a set of simulations in which we vary the background substrate doping, which is the uniform doping of the die before the well dopings are implemented. This primarily changes the doping immediately underneath the source, drain or well contact diffusions. This is because the well doping is a fairly steep Gaussian profile that falls off to be lightly doped right below the diffusions (Fig. 5), and the doping level in those regions only is given primarily by the background substrate doping. We also consider the case in which the background doping remains constant but the depth of the heavily doped well contact varies. The results reinforce our earlier hypothesis described at the end of Section V, illustrated in (Fig. 8(c). As shown in Fig. 9, for a highly doped substrate (background doping of 5×10^{17} cm^{-3}), resulting in a weak high-low junction at the well contact, there is hardly any drop at the well contact (well-contact cut line of Fig. 9), and the source-well junction has a potential as high as 0.8 V (source cut line of Fig. 9).

Consequently, the "plateau" potential drops 0.75 V below the ground (shown in Table II). On the other hand, for a lightly doped substrate (nominal background doping of 10^{16} cm^{-3}), a stronger high-low junction at the well-contact supports a much higher potential gradient from the push out (well contact cut line in Fig. 10), resulting in a smaller potential drop across the source-well junction, and a much smaller excursion of about 0.4 V below the rail

TABLE II
Plateau Voltage as a Function of Substrate Doping Concentration

Substrate Doping Concentration (cm^{-3})	Plateau Voltage (V)
10^{14}	-0.03 V
10^{15}	-0.18 V
10^{16}	-0.41 V
5×10^{17}	-0.75 V

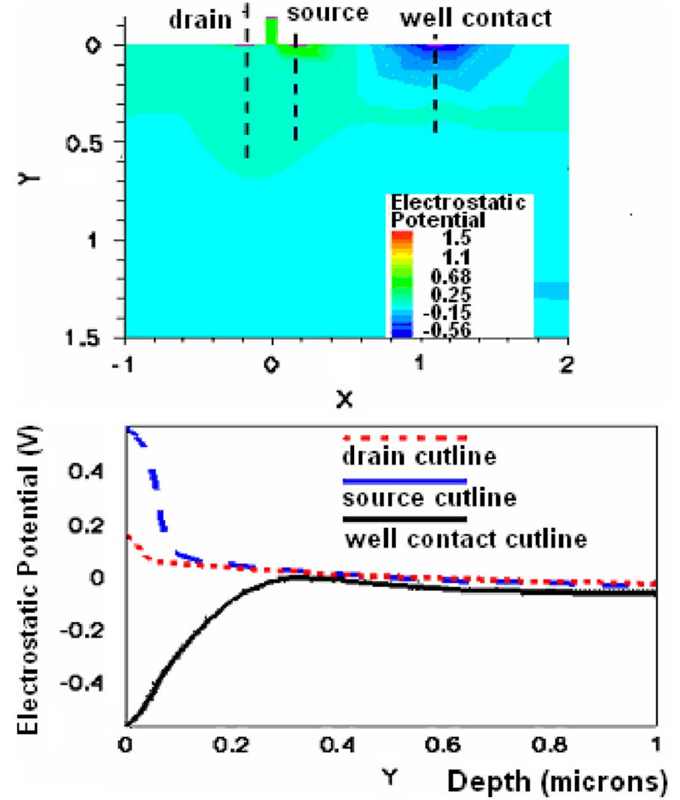


Fig. 10. Contour plot of potential (top) and 1-D profile of potential (bottom) underneath the drain, source and well contact for a lightly doped (10^{16} cm^{-3}) substrate. Significant potential drop at the well contact leads to low source-substrate junction potential, which translates to a small excursion of the drain voltage below the rail (Table II). The depth of the heavily doped well contact in this case is 80 nm. Cutlines have been obtained 25 ps after a strike of LET 10 MeV/(mg/cm^2). Potentials are referenced to E_i, i.e., $V(x) = \phi_s(x) - E_i/q$.

TABLE III
Plateau Voltage as a Function of P-Well Contact Doping Depth

Well Contact Doping Depth (nm)	Plateau Voltage (V)
80	-0.41 V
250	-0.53 V
350	-0.61 V
450	-0.71 V

(Table II). Very similar trends are seen due to an increase in the depth of the heavily doped well contact (Table III).

VI. Conclusion

Mixed-mode TCAD simulations of deep submicron (130 or 90 nm) SET waveforms in inverter strings reveal that although low LET pulses ($\sim$ 1 MeV/(mg/cm^2)) still have a classical

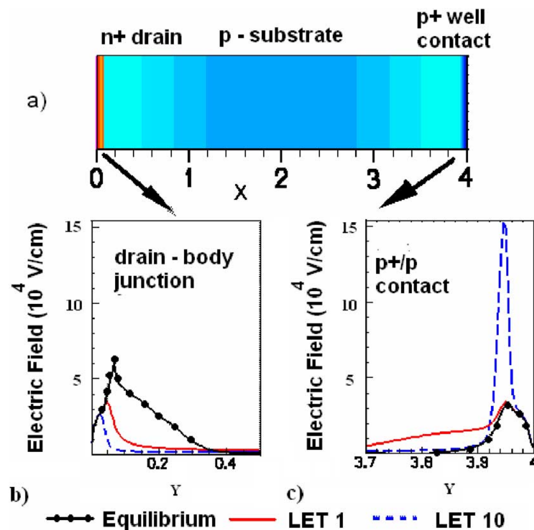


Fig. 11. (a) 2-D simulated diode with highly doped P+ contact. As the structure is injected with mobile charges of both types, the high field location shifts from drain to contact. Magnified views shown in (b) (drain-body junction) and (c) (well contact junction). Area under curve denotes potential drop.

double exponential waveform in these technologies, for higher LETs ($>$ 10 MeV/(mg/cm^2)) the current pulses have a plateau region in addition to the double exponential waveshape. The voltage pulses likewise have a plateau, which may be lower than V_{ss}, depending on the doping of the substrate and well contact. Simulations also show that the inverter single event waveforms are insensitive to capacitive loading (for the range of loads, device to contact spacing and sizes examined), and the plateau current corresponds exactly to the drive strength of the restoring MOSFET with its drain voltage pinned to the plateau voltage. Further TCAD simulations indicate that the mechanism for the plateau behavior for higher LET particles is related to the shift in the location of the strongest potential gradient from the drain-substrate junction to the highly doped primary well contact in the struck device. Since the total depletion charge (which controls the equilibrium potential in the device and the surrounding substrate) and the minimum spacing to the well contact diminish with scaling, the potential pushout at the irradiated junction is more evident in deep submicron technologies. The substrate and well contact doping affect the plateau shape by changing the push-out of the potential profile, confirming our hypothesis about the details of the plateau shape.

Appendix

The potential pushout effect discussed in Section IV, has been previously observed with power diodes and MOSFETs, during avalanche breakdown. An analytical study of the effect has been presented in [14], for avalanche breakdown, and in [17] for single event breakdown in power diodes. We demonstrate very similar effects in this Appendix by studying a simplified situation, almost equivalent to the injection conditions we have presented for our earlier results.

A simple 2-D diode structure with a length of 4 μ m (Fig. 11) is injected with mobile charges uniformly (creating uniform charge generation throughout the volume). The quantity of interest here is the area under the field curves in Fig. 11(b), which denotes the potential drop. The rapid disappearance of the junction potential at the N^+/P junction is demonstrated very clearly as we go from equilibrium to an LET of 10 MeV/(mg/cm^2) (Fig. 11(b)). As the potential at the drain-substrate junction decreases, the potential builds up rapidly at the P^+ well contact (Fig. 11(c)).

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Application of RADSAFE to Model the Single Event Upset Response of a 0.25 μm CMOS SRAM

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***Abstract*—The RADSAFE simulation framework is described and applied to model SEU in a 0.25 μm CMOS 4 Mbit SRAM. For this circuit, the RADSAFE approach produces trends similar to those expected from classical rectangular parallelepiped models, but more closely represents the physical mechanisms responsible for SEU in the SRAM circuit.**

***Index Terms*—GEANT4, heavy-ion, RADSAFE, SEU, TCAD.**

I. Introduction

OVER THE PAST two decades a series of publications ([1]–[14], for example) has given experimental and simulation evidence showing that Single Event Effects (SEE) analysis techniques akin to the rectangular parallelepiped (RPP) [15] model fail to provide accurate reliability/survivability estimates for certain technologies. This is because today's technologies have been scaled to dimensions where phenomena challenge some of the basic simplifying assumptions of these radiation effects models, which were developed for technologies fabricated in the late 70s and early 80s.

The underlying physical mechanisms for SEE response are: 1) ionizing radiation-induced energy deposition within the device, 2) initial electron-hole pair generation 3) the transport of the charge carriers through the semiconductor device and 4) the response of the device and circuit to the electron-hole pair distribution and subsequent transport. Each of these mechanisms occurs on a different time scale and they are often assumed to be sequential, i.e., energy deposition determines the initial electron-hole pair generation, which in-turn impacts device and circuit response.

The goal of the RPP model is to provide a simple, approximate model for the processes described above. This approach has been very successfully applied to space missions over several decades. In this work a new modeling approach aimed at overcoming some of the limitations of the RPP model is presented. The concept is called RADSAFE.

The RADSAFE concept is presented and the approach is demonstrated by applying it to modeling Single Event Upsets (SEUs) in a commercial 0.25 μm CMOS SRAM observed during ground-based testing.

Manuscript received October 6, 2006; revised December 13, 2006. This work was supported in part by the NASA Electronics Parts and Packaging Program and the Defense Threat Reduction Agency (DTRA).

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Digital Object Identifier 10.1109/TNS.2006.889810

II. RADSAFE Concept Overview

The RADSAFE approach is focused on the end goal of developing a fully-automated, first-principles predictive tool that is based on the best available physics for radiation transport and microelectronic device performance. This is a Monte Carlo technique that combines three distinct concepts: 1) transport of the radiation environment though the component and relevant surrounding materials; 2) approximation models to estimate the response of the technology to radiation exposure; and 3) deterministic simulation of the detailed component response to radiation exposure.

The first segment builds on existing, reliable, and well-calibrated computational physics models for the transport of radiation through matter. The Monte Carlo code used in this segment is a Geant4 [16] application called the Monte Carlo Radiative Energy Deposition (MRED) (developed by researchers at Vanderbilt University). Geant4 is a library of c++ routines assembled by an international collaboration for describing radiation interaction with matter. MRED includes a model for screened Coulomb scattering of ions [17], tetrahedral geometric objects [18], a cross section biasing and track weighting technique for variance reduction, and a number of additional features relevant to semiconductor device applications. The Geant4 libraries frequently contain alternative models for the same physical processes and these may differ in level of detail and accuracy. Generally, MRED is structured so that all physics relevant for radiation effects applications is available and selectable at run time.

The second segment of RADSAFE is accomplished by first uncovering the basic mechanisms for the device/circuit SEE response using detailed mixed-mode (TCAD coupled to SPICE) simulators and ground-based experimental data. From this understanding, an approximation model for the response (called a Quasi-Device Physics model or QDeP) is developed.

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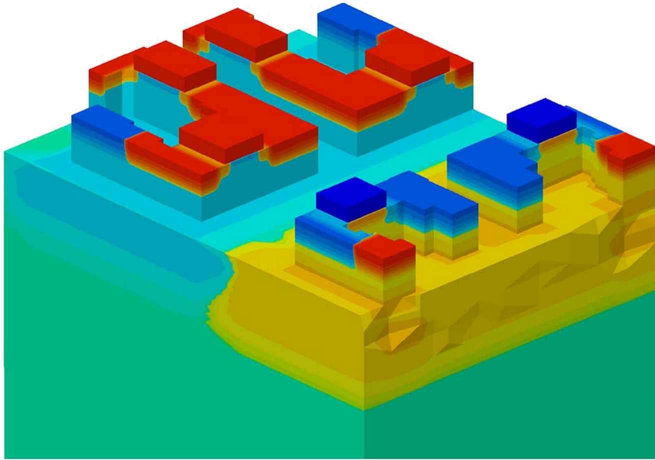

Fig. 1. TCAD model of the full SRAM cell (isolation oxide not shown). Red areas indicate n-type dopants, blue indicate p-type dopants.

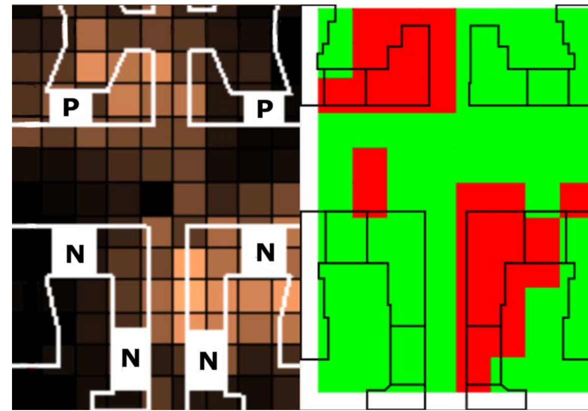

Fig. 2. Top view of the microbeam test results (left) and TCAD simulation results (right) showing the areas that produce an SEU for ion $\mathrm{LET} = 6$ MeV-cm^2/mg. The lighter regions in the microbeam image and the red regions of the TCAD image represent the location of upsets. The cross-section at this LET is estimated by the sum of the red colored areas.

QDeP models are technology dependent; they can be analytical or Monte Carlo models that account for both the energy deposition in the semiconductor by the radiation event and the device/circuit response to this event. While not a requirement, the QDeP models can be included in MRED. An example of a QDeP model is provided below for the SRAM used in this study. The QDeP estimate allows for timely and accurate computational analysis of the device response by selecting only those events that have a high probability of causing an effect.

The third segment of RADSAFE combines segments one and two to allow for a deterministic estimate of the response of the circuit to a particular radiation environment (ground test or space). The approach is to generate selected events from the radiation environment in detailed geometric structures representative of the entire component, including structures like the metallization layers. The energy deposition is computed in detail. An event selection process is used to predict the component response. The process flows from lowest fidelity, fast simulation time to highest fidelity, long duration simulations. Each event is analyzed at various levels of detail, e.g., energy deposition in simple RPP structures, QDeP, and/or full 3-D mixed-mode simulations. Once fully developed, the QDeP model for each technology is the workhorse for event selection. In this simulation flow, this process replaces the classical models like those used in the CREME96 routines for heavy-ion effects.

In the next two sections, the application of the RADSAFE concept to predict the ground-test SEU response of a 0.25 μm CMOS 4 Mbit SRAM is presented.

III. Calibration of TCAD Simuations to Experiment

Detailed full 3-D TCAD simulations were performed on one cell of the 4 Mbit SRAM (Fig. 1) and the entire cell was modeled in mixed-mode simulations, with all of the active semiconductor regions contained in TCAD. The TCAD model was developed via calibration of their electrical characteristics to known device characteristics, e.g., $I_d - V_g$ data. To ease the burden of device simulation, the local interconnect and large portions of polysilicon were replaced with SPICE-level components. Detailed device cross-section and doping profile information were provided by the vendor and SEM analysis.

The purpose of the TCAD simulations was to understand the topology of the SRAM cell's sensitive area and how it varies as a function of LET. For comparative purposes, the Sandia Focused Heavy-ion Microprobe Facility [19] was used to identify regions of the circuit that were sensitive to SEU.

TCAD simulations were performed using two different values for LET: 2.0 and 6.0 MeV-cm^2/mg. The former was chosen as it is near the experimental upset threshold and the latter because it is the same as that used in microbeam testing. The SEU simulations were performed by rastering incident particles over the entire surface of the cell at normal incidence. For each of the two LET, the steps were 0.25 μm in the x (8 steps) and y dimensions (11 steps), totaling 176 simulations. Fig. 2 shows SEU results for $\mathrm{LET} = 6$ MeV-cm^2/mg for both the microbeam exposures and from TCAD simulation. The upper right region shows the drain and gate of the off PMOS device to be a portion of the sensitive area, while the bottom left region gives the contribution to the sensitive area of the drain and gate of the off NMOS device.

The experimental values for the SEU cross-section were measured at Brookhaven National Lab's Tandem Van de Graaff accelerator. Table I compares the broad-beam heavy-ion experimental cross-section data to the estimated sensitive area determined from TCAD simulations for two LET. There is very good agreement between the experimental values and the simulations. From these results it is obvious that a single RPP volume does not accurately represent the sensitive volume structure of the memory cell in detail. However, in practice, the RPP model has been successfully applied to describe a device response similar to this one, albeit in a less physically correct way.

IV. Development of QDeP Model for 0.25 μM CMOS SRAM

A novel approach to defining the sensitive volumes of the circuit was implemented in MRED. The overall deposited en-

TABLE I
COMPARISON OF EXPERIMENTAL CROSS-SECTION TO ESTIMATE FROM TCAD

LET ($MeVcm^2/mg$)	Supply voltage (V)	Experimental cross-section (μm2)	TCAD estimate of sensitive area (μm2)
2.0	2.0	≈0.88	0.75
6.0	1.4	≈1.5	1.6

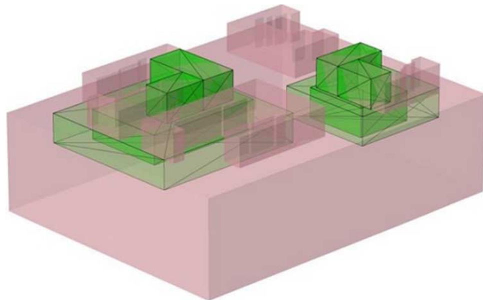

Fig. 3. SRAM cell layout showing the sensitive location of the volumes.

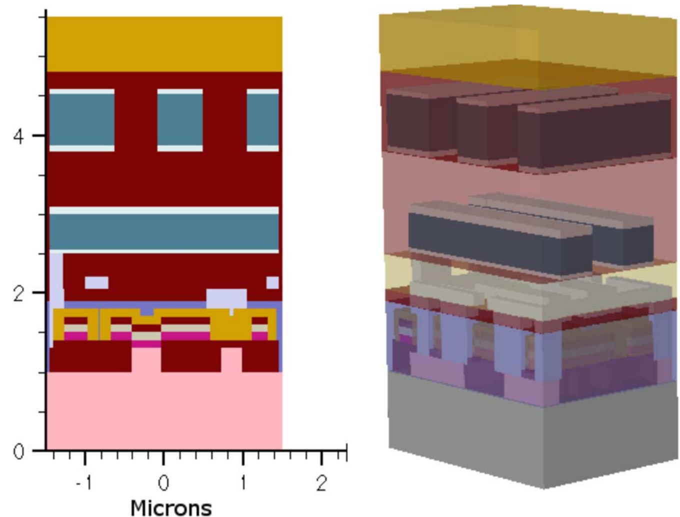

Fig. 4. 2-D cut plane (left) and full 3-D solid model (right) of a single bit of the SRAM. Transport and calorimetry simulations were performed on the 3-D model.

ergy was calculated in terms of a linear combination of weighted sensitive volumes within the TCAD object rather than the customary single volume used in RPP calculations.

The concept is illustrated in (1). If one interprets the weighting coefficient, α, as a measure of charge collection efficiency, it becomes a means of approximating the quantity of collected charge, Q, from the deposited energy, E. Therefore, the total collected charge can be viewed the sum of the weighted contributions of deposited energies in all N volumes. Note that if one chooses a single volume $(\mathrm{N}=1)$ with an α of unity, (1) reduces to the standard RPP model.

$$Q \approx \frac{1\ \mathrm{pC}}{22.5\ \mathrm{MeV}} \sum_{i=1}^{N} \alpha_i E_i \tag{1}$$

The locations of the sensitive regions were determined by examination of the layout and process, as well as TCAD simulation results. Six volumes (Fig. 3) were used to describe the sensitive regions of the circuit. The depths of the volumes extended to the bottom of the n- and p-wells (0.3 μm beneath the STI). By inspection of the TCAD results, the highest values of α were found to be in the active silicon region of the off-state transistors' drains. Efficiencies were substantially less for regions beneath the STI and far from the transistor drains.

For Monte Carlo simulations in MRED, electronic stopping, as well as nuclear reactions, were simulated as discussed in [20]. To further improve the fidelity of the simulations, a complete 3-D solid model of the SRAM was generated from layout information and scanning electron microscope (SEM) cross-sections (Fig. 4). Each material within the real process is represented accurately, both from a spatial and compositional standpoint.

A histogram, T(E), was generated for each ion simulated. T(E) is the number of events in a given energy range (dN(E)/dE) as a function of the sum of total weighted energy. The per-bit cross-section, as a function of the weighted deposited energy, was calculated according to (2) where A is the area of the irradiated bit, and N is the total number of simulated events. An example calculation of σ(E) for the case of 99 MeV ^{12}C is shown in Fig. 5

$$\sigma(E) = \frac{A}{N} \int_{E}^{\infty} T(E')dE'. \tag{2}$$

Equation (2) can be used to estimate the upset cross-section if the lower limit of the integration interval is the circuit critical charge, Q_{crit}. To determine Q_{crit}, SPICE simulations were performed. Double exponential current sources approximating the charge collection pulse were used to source and sink current on the off-state P- and NMOS transistor drains, respectively. Baseline parameters for the double exponential function were derived from TCAD SEE simulations. The total charge associated with the double exponential was modified by adjusting the magnitude of the current pulse in order to find the minimum charge required to cause an upset (Q_{crit}). A mean Q_{crit} of 10 fC and a standard deviation of 1 fC were determined using nominal and corner SPICE models provided by the vendor. A normal distribution of Q_{crit} across the 4 Mbit device was assumed for subsequent simulations.

Assuming an energy to charge conversion of 22.5 MeV/pC, the average per-bit cross-section as a function of Q_{crit} was calculated according to (3) where N(Q') the probability density function of bits with critical charge Q' and σ (Q') is the cross-section associated with collecting that charge

$$\sigma(Q_{\mathrm{crit}}) = \frac{\int_{Q_{\mathrm{crit}}}^{\infty} N(Q')\sigma(Q')dQ'}{\int_{0}^{\infty} N(Q')dQ'}. \tag{3}$$

The predicted cross-section curve for a 4 Mbit device with a mean Q_{crit} of 10 fC and a standard deviation of 1 fC was calcu-

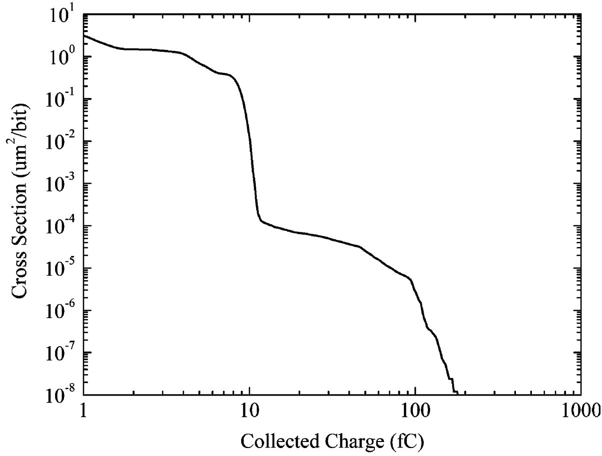

Fig. 5. MRED computed cross-section as a function of the estimated collected charge for 99 MeV ^{12}C.

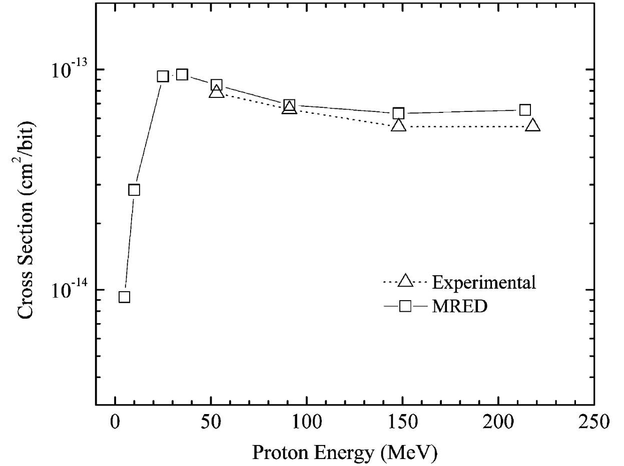

Fig. 7. Experimental and simulated proton SEU cross-section data for the SRAM. Data were taken at the Northeast Proton Therapy Center.

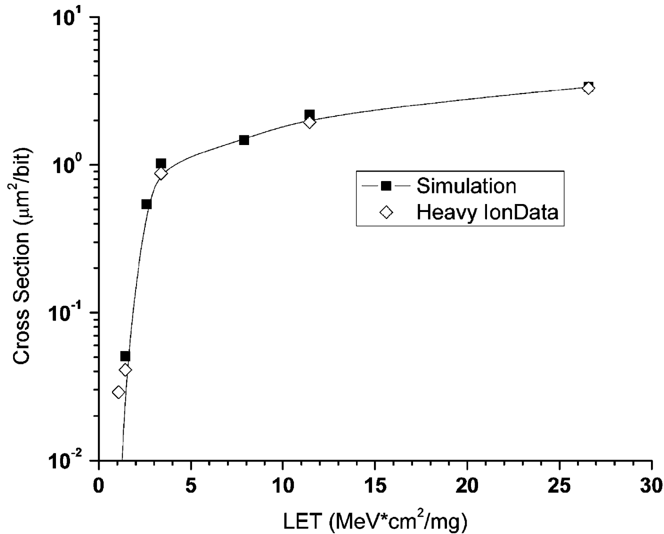

Fig. 6. Measured and simulated cross-section versus LET curves at normal incidence.

TABLE II
IONS USED IN RADSAFE SIMULATIONS AND HEAVY-ION TESTING

Species	Energy (MeV)	LET (MeV-cm²/mg)
^{7}Li	56	0.38
^{11}B	84	1.07
^{12}C	99	1.44
^{19}F	140	3.38
^{28}Si	187	7.90
^{35}Cl	210	11.40
^{58}Ni	265	26.58

lated for various ion species available at Brookhaven National Lab (Table II) and is shown in Fig. 6.

V. MODEL EXTENSIBILITY

The purpose of the simulation methodology presented in this work is to demonstrate a process that provides the highest fidelity simulation framework possible with the ultimate goal of a developing comprehensive rate prediction tool. It has been demonstrated that the construction of a multiple sensitive volume model produces results that agree well with measured heavy-ion SEU cross-sections. However, it is desirable to have the same model be predictive in other radiation environments.

To test the extensibility of the model to other primary particles, proton test results from the Northeast Proton Therapy Center [21] and simulations of proton cross-sections using the identical sensitive volume properties (Fig. 3) and materials (Fig. 4) applied to the broad-beam simulations were compared. In essence, the only difference from a user standpoint between the broad-beam and the proton simulations was the choice of particle type and energy. The results are shown in Fig. 7. The simulation results agree extremely well with the experimental data.

VI. EMPIRICAL MODEL

The level of process, layout, and circuit detail used in this study may not always be available. If one's objective is to derive a model of the sensitive volume suitable for rate predictions in a Monte Carlo simulator based upon heavy-ion data alone, it is possible to reverse engineer a set of weighted sensitive volumes in a purely analytical manner by assuming the following.

1) The shape of the cross-section curve is entirely due to intra-cell variations in charge collection efficiency and the surface area of the volume can be related directly to the heavy ion cross-section;
2) Sensitive volumes are arranged concentrically and each volume is centered about the same point as illustrated in Fig. 8;
3) The depth of each volume is identical;
4) The combined efficiency of all α is unity (where all volumes overlap, $\alpha = 1$).

By assumption 1, the area of the sensitive region, A_n, at LET E_n, can be described by (4) where $E_o, \sigma_{\rm sat}$, s, and w are the Weibull fitting parameters (other functions, such as the log-normal distribution can be substituted)

$$A_n = \sigma(E_n) = \sigma_{\rm sat}\left[1 - e^{-\left[\frac{E_n - E_0}{w}\right]^s}\right]. \quad (4)$$

The choice of points at which to evaluate A_n is arbitrary, however, a uniform spacing of N values in logarithmic space over the

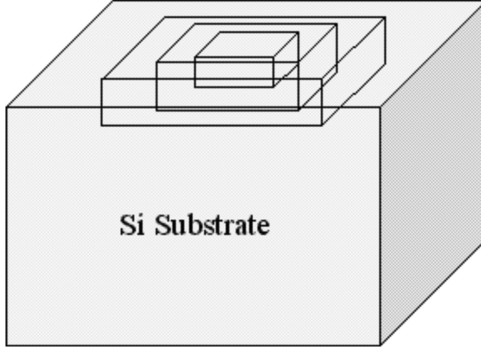

Fig. 8. Illustration of three sensitive volumes ($N = 3$) arranged concentrically within a $10 \times 10 \times 15\,\mu\mathrm{m}^3$ volume of silicon. The centermost region where the three volumes overlap has a combined α of 1.

range of E_o to E_m is convenient and can be chosen according to (5) with n valid from 0 to N-1.

$$E_n = E_0 \left[\sqrt[N-1]{E_m/E_0} \right]^{\frac{2n+1}{2}}. \tag{5}$$

The number of points, N, corresponds to the number of sensitive volumes used in the simulation. The efficiency of the nth volume, α_n, is described by (6) where u is the unit step function, and E_c is the energy value between E_n and E_{n+1}, which is calculated in (7). The addition of the unit step function to (6) satisfies assumption 4 where α_n has the property of summing to unity (8)

$$\alpha_n = \frac{E_0}{E_c}\left(1 - u(N-n-2)\left[\sqrt[N-1]{E_m/E_0}\right]^{-1}\right) \tag{6}$$

$$E_c = E_0 \left[\sqrt[N-1]{E_m/E_0}\right]^n \tag{7}$$

$$\sum_{n=0}^{N-1} \alpha_n = 1. \tag{8}$$

Since the volumes are arranged concentrically, and by (8), the net charge collection efficiency at the 0th volume ($n = 0$) is 100%. This is because all N volumes overlap with the volume $A_{n=0}(E_o)$ as illustrated in Fig. 8. Therefore, D_{sv} is related to the critical charge (in fC) at threshold, LET_o, by (9), where LET is in units of MeVcm^2/mg and the depth is in micrometers. In this case, one must make an assumption about either the depth or the critical charge depending on the available information

$$Q_{\mathrm{crit}}(fC) = 10.35 \cdot LET_o \cdot D_{\mathrm{sv}}. \tag{9}$$

The reverse engineering approach was applied to the 4 Mbit SRAM. The broadbeam data were fit to a Weibull function as shown in Fig. 9. Ten sensitive volumes ($N = 10$) were chosen with E_o and E_m equal to 2.0 to 30.0 MeVcm^2/mg respectively. Equations (4) and (6) were used to generate the corresponding A_n and α_n. The discretization of the Weibull function and efficiencies are plotted in Fig. 10. Square volumes having equal length and width were assumed.

By (9), and a known Q_{crit} of 10 fC, a charge collection depth of 0.48 μm was calculated for all volumes. For MRED simulation, the volumes were placed in a 10×10 um^2 by 15 μm deep block of silicon. The surface of the volumes was coplanar

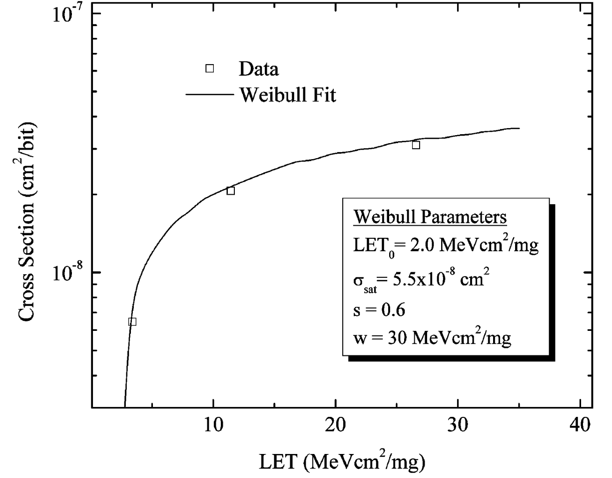

Fig. 9. Heavy-ion SEU cross-section data fit to Weibull function for the 4 Mbit SRAM.

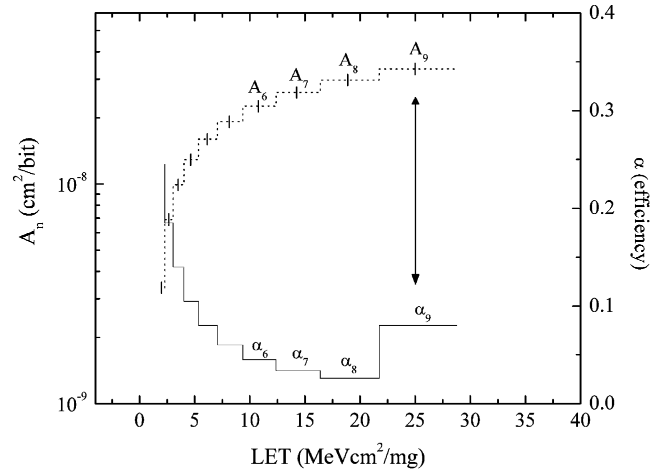

Fig. 10. Areas, A_n, and efficiencies, α_n using the Weibull fit parameters. Note that the increase in efficiency for $n = 9$ is due to discontinuity introduced by the step function in (6) and ensures that the condition in (8) is met.

with the surface of the substrate. Simulations were performed for several of the heavy-ion species. The cross-sections, shown in comparison to the experimental data, are plotted in Fig. 11.

The simple analytical sensitive volume model derived from the broad-beam results agrees well with the experimental data. At LET beyond the threshold, the MRED results track the Weibull function. Because the target structure was nothing more than silicon, interactions of the beam species with over-layer material are not modeled. Previous studies have shown that nuclear reactions in over-layer material can affect cross-section results at threshold and sub-threshold regions [21]. No attempt was made to include inter-cell variation in the critical charge. Despite the simplifications, the Monte Carlo results produce a cross-section curve that tracks the heavy-ion broad-beam data. Adjustments of D_{sv}, Q_{crit}, α, or sensitive volume aspect ratios are possible to improve the fit to data. For example, it may be necessary to modify aspect ratios to account for angular and rotational variations in SEU cross-section.

VII. Conclusion

We have demonstrated that describing the collected charge, as a linear summation of energy deposited within an array of

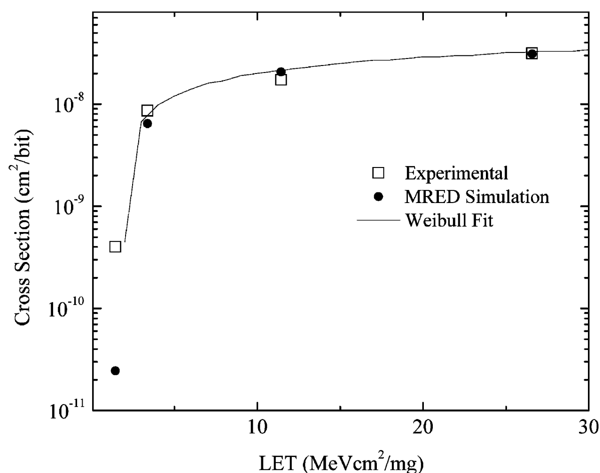

Fig. 11. Comparison of the MRED derived SEU cross-sections using the empirically derived sensitive volume parameters with experimental data.

sensitive volumes, is an effective way to model the broad-beam SEU response of the SRAM circuit in a Monte Carlo simulator. This technique captures intra-cell variations in charge collection efficiency and can be carried a step further by including inter-cell variations in critical charge as determined from Spice corner model simulations.

The extensibility of MRED to simulate more complicated phenomena such as high-energy proton induced SEU based on the same model used for broad-beam simulation is a good indication of the model's fidelity. The RADSAFE software suite is being expanded to allow the user to sample particles from a true environment spectrum for direct SEU rate predictions. In instances where only broad-beam data are available, it may be possible to provide a reasonably accurate error rate prediction based on the analytical fitting described herein. Although the target was modeled as nothing more than a silicon cube, over-layer materials can be included depending on the level of process knowledge if they are deemed significant to the part's SEU response [20], [22].

ACKNOWLEDGMENT

The authors wish to offer special thanks to Lew Cohn of the Defense Threat Reduction Agency (DTRA) for financial support. The computational portion of this work was performed with the resources of Vanderbilt University's Advanced Computing Center for Research and Education (ACCRE).

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The Effects of Angle of Incidence and Temperature on Latchup in 65 nm Technology

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***Abstract*—Single event latchup (SEL) in a 65 nm CMOS technology is examined with respect to strike angle of incidence and variations in device temperature. A significant difference in device sensitivity is observed with a change in the orientation of grazing angle strikes. The impact of an extremely high aspect ratio sensitive volume on SEL rate is discussed. It is suggested that SEL experiments should be conducted at various lateral orientations when near-grazing beam angles are tested.**

***Index Terms*—Radiation effects, single event latchup, 65 nm.**

I. Introduction

SINGLE EVENT LATCHUP (SEL) has been a significant reliability concern for CMOS devices in radiation environments for the last twenty to thirty years [1]–[9]. As devices have scaled to smaller dimensions, with a concomitant decrease in the amount of deposited charge necessary to perturb electric fields into a possible latching condition, there is the concern that circuits may become more susceptible to SEL [9]–[13]. In contrast to this trend toward increasing vulnerability, the scaling trend of electrical characteristics relevant to latchup for new technology nodes works in the system designer's favor [14]. With the reduction in the gain product of the two parasitic transistors involved in the latchup process and with the supply voltage scaling below the electrical holding voltage, latchup may be of less concern in future technologies. It should be noted that for reliability concerns, a simple test of the electrical holding voltages, gain products, and holding currents at room temperature may not be sufficiently rigorous to allay all concerns about latchup [15]–[17]. For a given application, the range of environment temperatures must be considered.

Recent publications have examined the effects of temperature and angle of incidence for protons and heavy ions on latchup [12], [15]. The experimental results showed both the influence of temperature and angle of incidence on latchup cross section in SRAMs. Latchup cross section was seen to increase with both increases in temperature and incident angle rotation towards a more grazing angle. In these tests and other typical tests [12], [15], [18], devices are tested at two temperatures and the angle of incidence is rotated along only one axis to achieve a grazing angle. Because SRAMs are very asymmetric in their layout, grazing angle tests in only one lateral direction may be insufficient to characterize device latchup vulnerability fully.

Here, we present the results of SEL simulations of a 65 nm structure recommended for use in determining latchup sensitivity. The effects of both temperature and heavy ion angle of incidence are examined. In addition to this, a second device with a different width is also characterized for SEL vulnerability. Devices were found to have strong SEL threshold dependence on the orientation of grazing angle strikes. A discussion regarding the impact of a high aspect ratio sensitive volume on SEL rates follows the simulation results.

II. Device Structure

The device examined in this work is an NPNP structure from a test chip fabricated in a 65 nm CMOS technology. This device was created using the IEEE standard for latchup process characterization [19]. Devices of this type use long strip-contacts across a wide device that allow for easy high-current DC measurements and minimize edge effects that may dominate smaller devices. This is an interesting device because the fundamental mechanisms for latchup in a process can be studied without interference from other active devices. The understanding from the standard test device can then be applied to more highly integrated devices. The anode (P-source) to cathode (N-source) spacing in devices of this type is the minimum allowed by the process. A cross section of the active part of the device is shown in Fig. 1(a). The layout is shown in Fig. 1(b). The device was simulated and calibrated using measured electrical characteristics and doping profiles from vendor process simulations. The well contact is 10 μm from the anode and the substrate contact is 20 μm from the cathode. The anode and cathode represent the P-source and N-source in a CMOS structure, respectively. The N-well and the contacts for the N-well, P-anode, N-cathode, and P-substrate are 20 μm wide. Fig. 1(c) shows the corresponding 3-D TCAD device. To reduce computational time and memory constraints, the device is cut in half in TCAD to take advantage of the symmetrical properties of the structure. For all the biasing and temperature conditions in these simulations, the product of the two bipolar transistors' current gains is

Manuscript received July 20, 2007; revised September 26, 2007. This work was supported by the Defense Threat Reduction Agency and the National Aeronautics and Space Administration.

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Digital Object Identifier 10.1109/TNS.2007.910330

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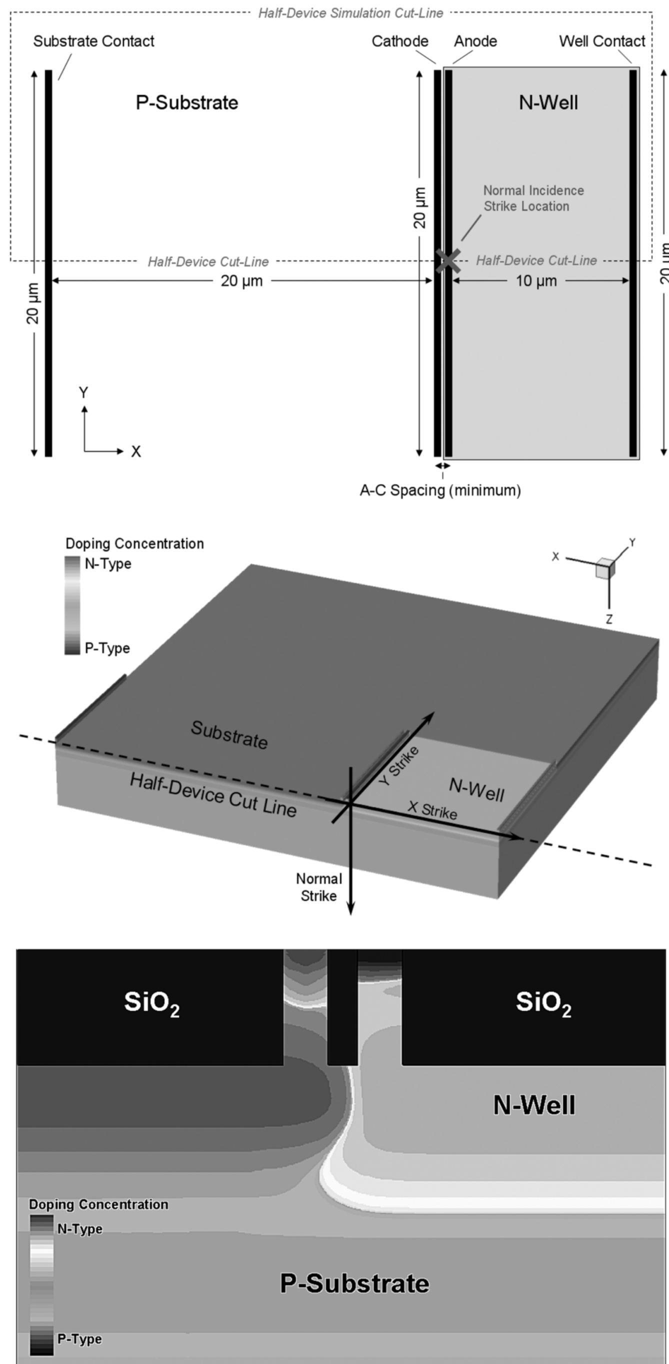

Fig. 1. (a) Layout of physical 20 μm wide SCR structure in 65 nm technology with a 10 μm long N-well and 20 μm cathode-P-tap spacing. (b) TCAD structure for simulations. Strike orientations for simulations are indicated. (c) Zoomed-in cross section of active parts of the SCR structure.

above unity. With that requirement for latchup satisfied, holding voltage and holding current are examined.

III. TCAD Simulations and Results

Boselli *et al.* have shown that for the 65 nm technology examined here, holding voltage exceeds the nominal operating voltage at room temperature [14]. However, modern commercial processors can operate within specifications up to almost 400 K and military spec requires devices to be tested up to 425 K. Fig. 2 shows (a) the difference between holding voltage

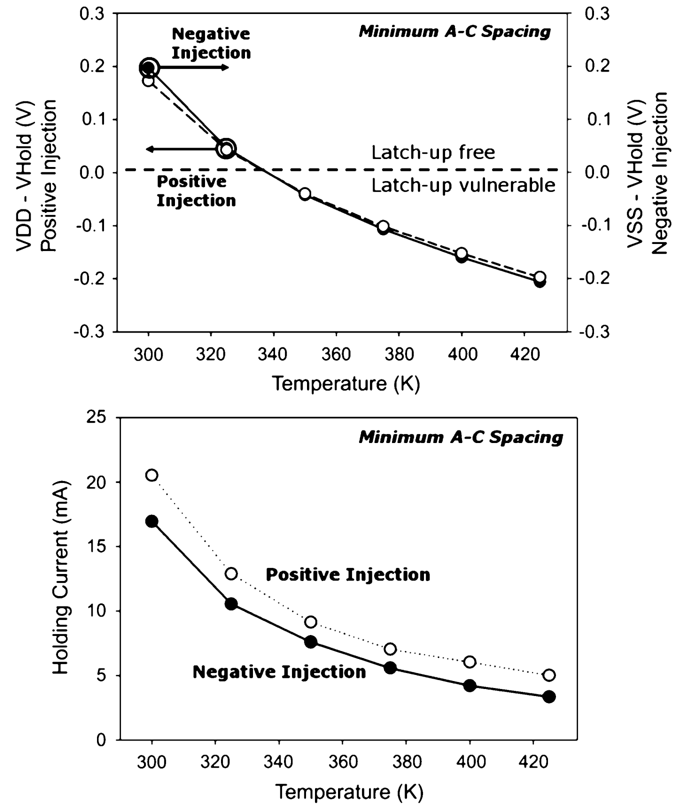

Fig. 2. Latchup vulnerability for 65 nm NPNP device with minimum A-C spacing. (a) Difference in holding voltage and operating voltage versus temperature. The plot is divided into latch-up free and latch-up vulnerable regions. (b) Holding current versus operating voltage.

and operating voltage and (b) the holding current versus device temperature for the simulated structure operated at the nominal core voltage of 1.2 V.

It is important to understand how these electrical characteristics relate to the single event latchup vulnerability. Response from localized interactions at the junction inside the structure due to collected charge are potentially quite different than the electrical response created from voltages and currents at the terminals of the structure. Initial SEL simulations were carried out using an LET of 80 MeV-cm^2-mg^{-1}, normally incident to the surface at the edge of the simulated region (corresponding to the middle of the physical device) and directly through the anode contact. It has been shown that the portion of the N-well farthest away from the well contact is the most sensitive region of the structure for initiating latch-up [6], [7]. All simulated ion track lengths are 20 μm long. This length was chosen as it is the longest physical dimension of the device and long strikes with constant LETs are useful for characterizing the change in device sensitivity as charge is placed in different areas within the volume of the N-well. For simulations with varying temperature, the temperature is uniformly set at the desired operating temperature. This is useful for examining trends due to device self-heating, but does not capture a detailed thermal profile of the device that would include increased temperatures at active junctions. Simulation boundary conditions are reflective, which assists in preserving the symmetry properties along the half-device cut line. Because we are mainly interested in charge

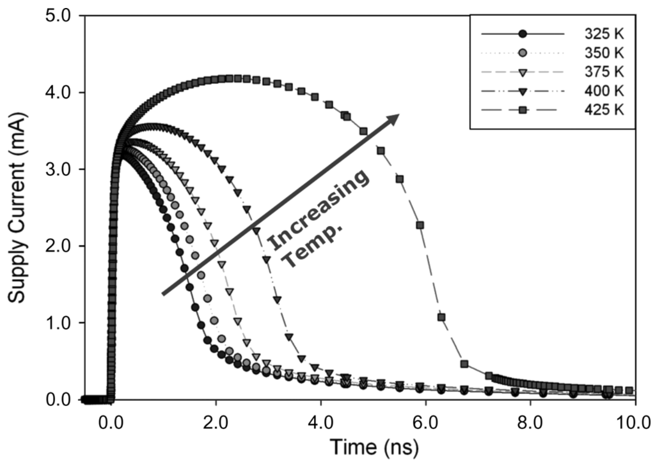

Fig. 3. Single event response current versus time for varying temperatures at nominal operating voltage (1.2 V). The current at the tied anode/N-well contacts is plotted.

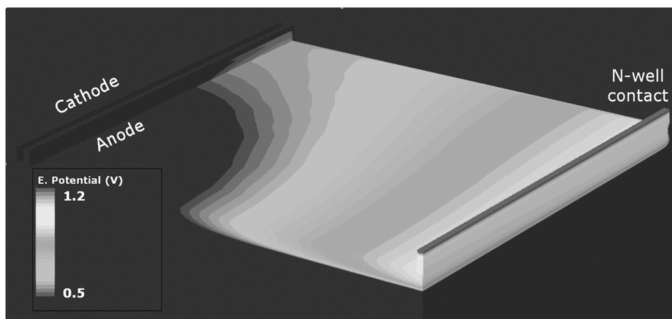

Fig. 4. Potential plot for 425 K temperature pulse seen in Fig. 3(b) at $t = 2.0$ ns. The N-well contact is at 1.2 V. The left side of the anode is a 0.7 V potential difference (diode drop) from that contact. About 6 μm (out of 10 μm) of the width of the device have the proper biasing for latchup.

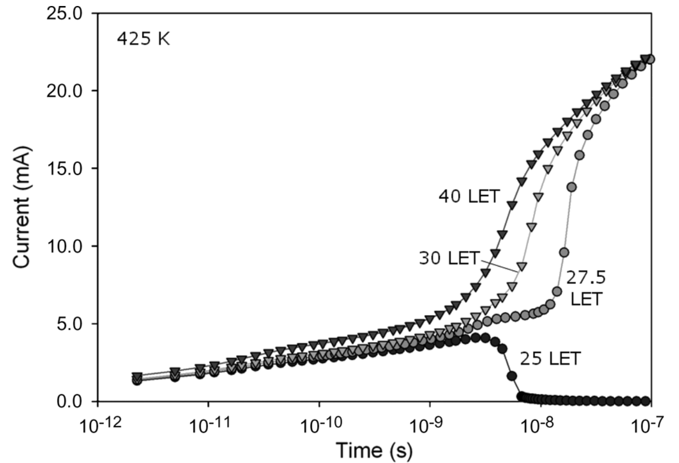

Fig. 5. Single event response current versus time for varying temperatures at nominal operating voltage (1.2 V) and 425 K for varying LET at grazing angle perpendicular to the anode [X direction in Fig. 1(b)]. The current at the tied anode/N-well contacts is plotted. LET is in units of MeV-cm^2-mg^{-1}.

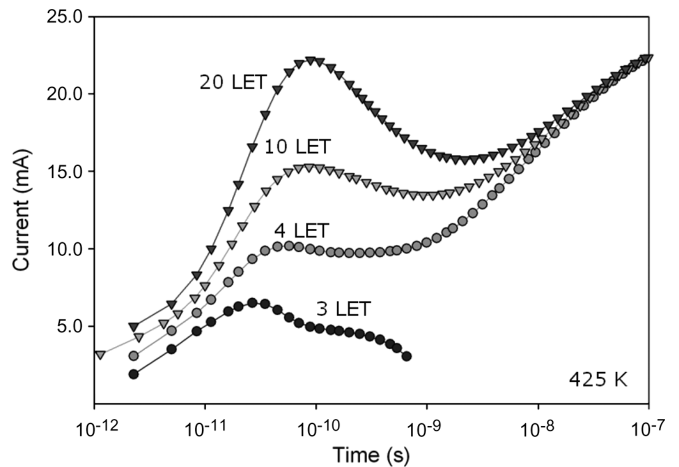

Fig. 6. Single event response current versus time for varying temperatures at nominal operating voltage (1.2 V) and 425 K for varying LET at grazing angle parallel to the anode [Y direction in Fig. 1(b)]. The current at the tied anode/N-well contacts is plotted. LET is in units of MeV-cm^2-mg^{-1}.

collection in the N-well near the anode contact, the reflective conditions near the N-well contact and the edges of the P-substrate (10 μm away from the N-well) will not result in a tangible change in latchup sensitivity. These single-event simulations were performed at nominal voltage for the technology (1.2 V) at various temperatures. The results are shown in Fig. 3, which displays the supply current versus time.

Fig. 3 shows that the structure does not latch up even for 80 MeV-cm^2-mg^{-1} normally incident strikes. At first glance, this could be assumed to be because the device currents are below the holding currents for their respective operating conditions. The very long pulse seen in the 425 K test at nominal (1.2 V) operating voltage is an example of the structure almost reaching the potentials required to enter a latching state. However, examination of the potentials for that event shows that about two-thirds of the width of the structure (closest to the strike) reaches a potential sufficient to cause latchup. Fig. 4 shows the potential in the N-well referenced from the N-well contact 2.0 ns after the 80 MeV-cm^2-mg^{-1} particle strike. It can be seen that even for this very high LET strike, the structure does not reach the potential necessary for latchup along the entire junction and can recover. The feedback in the regions of the structure where the device has the proper potentials for latchup contribute to the long pulse seen in Fig. 3. Normally incident strikes at 90 MeV-cm^2-mg^{-1} were sufficient to latch the structure.

To further investigate the vulnerability of the structure, an extreme grazing angle simulation was performed. For these tests, an ion strike parallel to the surface (90° from normal) was placed either in the X or Y direction [identified in Fig. 1(b) and (c)] directly below the STI layer. These simulations were performed at 425K and nominal (1.2 V) voltage. Fig. 5 shows the results for strikes in the X direction along the length of the N-well. For this orientation, lower LET particles than the normally incident ions discussed above are sufficient to latch the device. The latchup threshold is between 25 and 27.5 MeV-cm^2-mg^{-1}. The 25 MeV-cm^2-mg^{-1} strike does not latch the device, as the holding current seen in Fig. 2(b) is not achieved. This result is reasonable since the N-well tends to be the most sensitive region with regards to latchup and the majority of the charge deposition from the strike goes directly into the N-well.

Second, a strike was simulated in the Y direction parallel to the orientation of the anode. Fig. 6 shows this result. It can be

seen that the structure is substantially more sensitive to latchup in this direction with the latchup threshold between 3 and 4 MeV-cm^2-mg^{-1}. The majority of the charge is deposited directly under the anode at the furthest distance possible from the N-well contact while still remaining in the N-well.

This marked increase in sensitivity can be explained in two ways that are related to one another. First, with a long (narrow and shallow) sensitive volume underneath the length of the anode with the distance from the STI to the N-well/substrate boundary as the vertical dimension, even a low LET strike of 4 MeV-cm^2-mg^{-1} at a grazing angle deposits more energy over the 10 μm width than a normally incident strike with an LET of 80 MeV-cm^2-mg^{-1}. This is also true for the grazing angle strike in the X direction. If the sensitive volume is near the anode, most of the charge is deposited in the N-well outside of the sensitive volume. The second explanation is that latching is a localized phenomenon. While an 80 MeV-cm^2-mg^{-1} strike can deposit a significant amount of charge even in a shallow N-well, it only reaches the potential required to latch the PNPN structure within several micrometers of the strike. The Y-direction strike requires the minimum amount of deposited charge to provide the potential drop needed to forward bias the vertical PNP bipolar transistor and initiate latchup. The result is that the device is 6–7× more sensitive to strikes that are oriented along the N-well/P-substrate junction near the anode contact than to strikes with the same LET that are incident in the X-direction along the length of the N-well. Not only does it matter how much energy is deposited in a sensitive volume, the spatial distribution of that energy is critical in determining whether latchup occurs.

Although the test structure considered here has a more extreme aspect ratio than those considered in other studies, the results seen in Fig. 7 are consistent with work by other researchers that shows large increases in latchup cross section with temperature and angle [4], [15], [20]. For proton radiation, nuclear reactions with device materials (particularly higher Z metals and vias) may be the dominant mechanism for SEL [4], [6], [12], [15], [21], [22]. Reed *et al.* examined the relationship between proton energies and the directionality and range of spallation products from nuclear reactions [23]. In [15], significant increases in cross section at grazing angle are seen at proton energies where the reaction products are forward directed. The results described above demonstrate that reaction products with low LETs do not latch the SRAMs unless they are oriented along the N-well/substrate boundaries near the P-source contacts. Therefore, for predictive TCAD simulations it is crucial to understand and correctly model the physical processes and statistical distribution of proton fragmentation products at varying energies.

Due to the large aspect ratio of the sensitive volume in these structures, the change in SEL threshold is more pronounced with angle than the results in [15], but the trend is the same. This leads to the conclusion that the magnitude of the change in SEL threshold with angle is related to the width of the devices. This conclusion can be substantiated by performing tests on a narrower device. Another simulation structure was created with N-well width and contacts 5 μm wide instead of the previous 20 μm. Again, only half of the device was simulated and tests were performed at 425 K and 1.2 V to maintain a consistent simulation methodology. Fig. 7 shows the change in threshold LET between normal incidence to the surface and grazing strikes for both device widths. Both devices are much more sensitive to a grazing angle strike that occurs parallel to the N-well/substrate boundary underneath the anode than to a grazing angle strike perpendicular to the anode contact. While the numerical difference in threshold between grazing angle strikes in the X and Y directions is reduced for the smaller device, there is still more than a factor of 2 difference between the threshold LETs. Fig. 7 suggests that an extra axis of rotation is needed in SEL tests to characterize the effects of angle properly. Simply tilting the device under test to grazing angle will usually orient ions and forward directed secondary particles either parallel or normal to the longest component of the individual sensitive volumes in an SRAM. Given a typical layout for an SRAM, there is a clear sensitive orientation if the most sensitive areas of the device lie along the N-well/P-substrate boundaries. This is exhibited by the simple layout of multiple SRAM cells shown in Fig. 8.

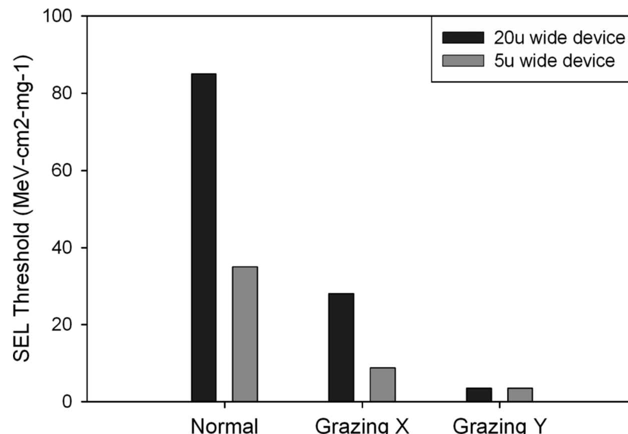

Fig. 7. Plot of threshold LETs for TCAD devices of different width. Both devices show a difference in sensitivity between grazing angle strikes in different directions as well as a greater sensitivity between normal incident and grazing angle strikes. In both cases, strikes oriented along the N-well/P-substrate junction near the anode require minimum charge deposition for latchup.

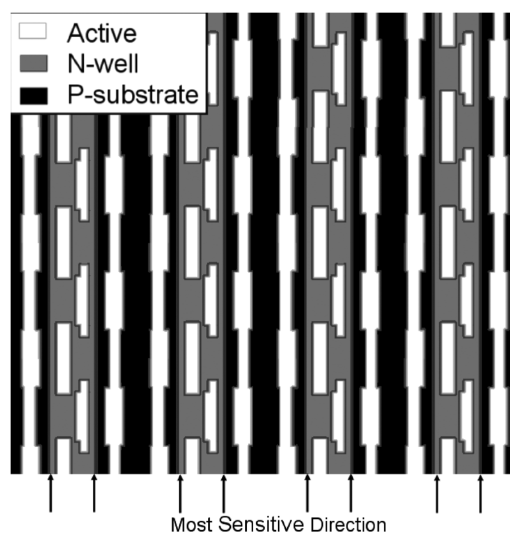

Fig. 8. Example of a typical CMOS SRAM layout. Active, P-substrate, and N-well regions are marked. The N-wells arranged in long columns present a likely most sensitive lateral directionality for SEL.

From this, it would be expected that when a beam is oriented at a grazing angle to the test device, rotating the test fixture laterally by 90° will likely change the threshold and cross section. For most deep submicron technologies, such a test will also need to be performed with the die above room temperature in order to see latchup. It is important to note that even when latchup is observed at room temperature, elevated temperatures within the operating range of the device must still be tested. Many structures operate using a dual voltage scheme: a higher voltage for I/O circuitry and a lower core voltage. Due to the higher voltage, I/O circuitry is typically more sensitive to SEL. It is likely that the I/O circuitry of modern highly-scaled devices may be the only SEL-sensitive area (if any) of a device at room temperature. Thus, a significant increase in the SEL cross section of a part could be observed at a temperature where the areas of the device with lower operating voltages become vulnerable.

IV. SEL Rate Issues

The device used in this work has an extraordinarily high aspect ratio sensitive volume (the N-well) in both lateral dimensions. The top view can be seen in Fig. 1(b) with the dimensions of the N-well being 10 μm × 20 μm. The depth of the sensitive volume (from the STI to the bottom of the N-well) is on the order of 0.5 μm. In order to cause latchup with anything but the highest LET particles, the energy deposition from all but the highest LET particles must be distributed primarily in the lateral direction. Ions in an isotropic space environment have a considerable probability of intersecting devices at severe grazing angles. Approximately 50% of ions in an isotropic environment intersect a device at 60° or greater from normal incidence. The ions with these trajectories are the most likely to trigger a SEL. When considering the effects of ions passing through such a long, wide, and shallow sensitive volume, basic assumptions for ions depositing charge along their trajectory will likely be invalid.

A large portion of the cosmic ray spectrum contains ions whose path lengths in Si are shorter than that of the lateral dimensions of the sensitive volume. The complications involved in the energy distributions from ions that actually stop in the sensitive volume must be considered and a Monte Carlo tool is necessary for these calculations. Nuclear reactions caused by ion and proton interactions with device materials also demonstrate the need for such a tool. Dodd *et al.* show that ion–ion nuclear reactions with high Z materials in devices strongly affect the SEL rate [24]. As discussed in Section III, the energy of protons plays a role in the directionality and path length of spallation products from reactions with high Z materials in devices. To predict a SEL rate accurately, both these effects require correct physical modeling and realistic statistical distribution in a Monte Carlo simulation.

V. Summary

We have demonstrated here both the effects of temperature and angle in determining the vulnerability of PNPN structures to SEL. Due to the large aspect ratio of the test structure, a significant change in threshold LET was observed with variable angle of incidence for simulated heavy ion strikes. It is suggested that researchers should examine the effects of angle using two axes in tests since particles not moving parallel to the edges of the N-well near P-sources are less likely to instigate latchup. Refining the techniques discussed here will allow development of a quantitative model for SEL sensitivity with angle, given the specific cell layout, process information, and desired operating temperatures. This model can then be used for predictive simulations using Vanderbilt University's MRED tool as seen in [25]–[31].

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Applications of heavy ion microprobe for single event effects analysis

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Available online 20 April 2007

Abstract

The motion of ionizing-radiation-induced rogue charge carriers in a semiconductor can create unwanted voltage and current conditions within a microelectronic circuit. If sufficient unwanted charge or current occurs on a sensitive node, a variety of single event effects (SEEs) can occur with consequences ranging from trivial to catastrophic. This paper describes the application of heavy ion microprobes to assist with calibration and validation of SEE modeling approaches.
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PACS: 61.82.Fk

Keywords: Radiation effects in semiconductors; Focused ion beam

1. Introduction

Ionizing-radiation can have dramatic effects on microelectronic circuit operation [1]. A class of effects, called single event effects (SEEs), is initiated when a single ionizing particle moves through a microelectronic component. The result can be a loss of stored information, erroneous transients at the circuit output, or even catastrophic circuit failure.

The underlying mechanisms for most SEE responses are: (1) ionizing radiation-induced energy deposition within the device, (2) initial electron–hole pair generation, (3) thermalization of charge carriers, (4) transport of thermalized carriers within the semiconductor and (5) the response of the device and circuit to carrier movement and recombination processes. Heavy ion microprobes have been used to support analyses and modeling of some of these mechanisms [2].

Ionization (mechanism 1) can result either from the direct interaction of incident particles with the integrated circuit (called direct or primary ionization) or from ionization induced by scattered particles or reaction products (called indirect ionization). These interactions can be modeled using radiation transport tools like Geant4 (described in more detail later). Conversion of energy deposition into thermalized electron–hole (e–h) pairs (mechanisms 2 and 3) is modeled by assuming that the ion must lose, on average in silicon, 3.6 eV of its energy to generate one e–h pair. Transport of the charge carriers (mechanism 4) and the resulting response of the device and circuit (mechanism 5) is modeled using technology computer-aided design (TCAD) tools [3].

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doi:10.1016/j.nimb.2007.04.163

In this paper, we discuss some recent applications of the microprobe at Sandia National Laboratories to uncover important charge collection properties of an emitter coupled logic (ECL) circuit based on silicon germanium (SiGe) heterojunction bipolar transistors (HBTs), validation of TCAD simulation of single event upsets (SEUs) in a 0.25 μm CMOS SRAM and calibration of sensitive volume dimensions for analysis of multiple bit upset (MBU) in a 130 nm CMOS SRAM.

2. Charge collection properties of an ECL circuit fabricated using SiGe HBTs

SiGe based technology is widely recognized for its potential to impact the high speed microelectronic industry by monolithic incorporation of low power complementary logic with extremely high speed SiGe HBT logic. Accessibility to SiGe through an increasing number of manufacturers adds to the importance of understanding its intrinsic SEE characteristics. IBM is now manufacturing its third generation of their commercial SiGe HBT processes and access is currently available to the first, second and third generation HBT processes (known as 5HP, 7HP and 8HP) through the MOSIS shared mask services. The data presented in this paper were collected on a simple ECL circuit fabricated in the 7HP HBT process (0.20 μm emitter and an f_T of 120 GHz).

Fig. 1(a) shows a diagram of the physical layout of an IBM SiGe HBT and identifies the location of the base, emitter and collector contacts. The transistor is manufactured almost entirely from silicon; the only germanium used is a small fraction of the material confined in the base region. The transistor area is totally contained inside two insulating trenches – a shallow trench (STI) and a deep trench (DT).

Previous investigations have examined the SEE response of 5HP and 7HP HBT circuits through both circuit testing [4,5] and modeling [6]. Charge collection modeling and measurement [7] studies in the 5HP process have also been conducted. The basis for most of the modeling and analysis in all of these papers has been ion beam induced charge collection (IBICC) measurements with emitter, base and collector contacts grounded and the substrate biased between −3 and −5.2 V. To date, no measurements have been reported that show charge collection properties of a SiGe HBT biased and loaded, as it would be in an active circuit.

The text that follows is a description of our use of Sandia National Laboratories' IBICC facility to interrogate the amount of charge collected by each terminal of a single SiGe HBT transistor that was configured as the "off" leg of an ECL differential pair, as shown in Fig. 1(b).

The target transistor was a $0.20 \times 1.14\ \mu m^2$ HBT. The surface area of the silicon volume contained within the DT is $2.12 \times 2.88\ \mu m^2$, called the active area. A physical analysis of the overburden was done using SEM images taken after irradiation. There was approximately 13 μm of dielectric and metallization (nearly 12 μm of this was dielectric) and 4 μm of polyimide.

A four probe IBICC measurement was used to simultaneously measure the charge induced on the collector, emitter, base and substrate terminals due to ion strikes occurring in and around the transistor area. The flux was set sufficiently low to ensure that no more than one ion was incident on the die at each step. The IBICC measurements were made using 36 MeV ^{16}O ions that have a range of 25.5 μm in silicon. For all tests, the ion beam "spot" size was approximately $1.6 \times 1\ \mu m^2$. This spot was stepped through a 1600 μm^2 area that contained the transistor with a step size of about 0.1 μm. The data cube is built up by thousands of scans and consists of the location (x, y coordinate) of the ion "spot" and the charge collected by each probe for each ion strike.

The data plotted in Fig. 2 show a 1 μm slice through the data cube in the y-direction. It shows the charge collected on the collector and the base as a function of position. The data are collapsed on a y-plane and were selected to contain events inside the DT. These data were also selected to be representative of events that traverse a cross-section through the device like that shown in Fig. 1(a).

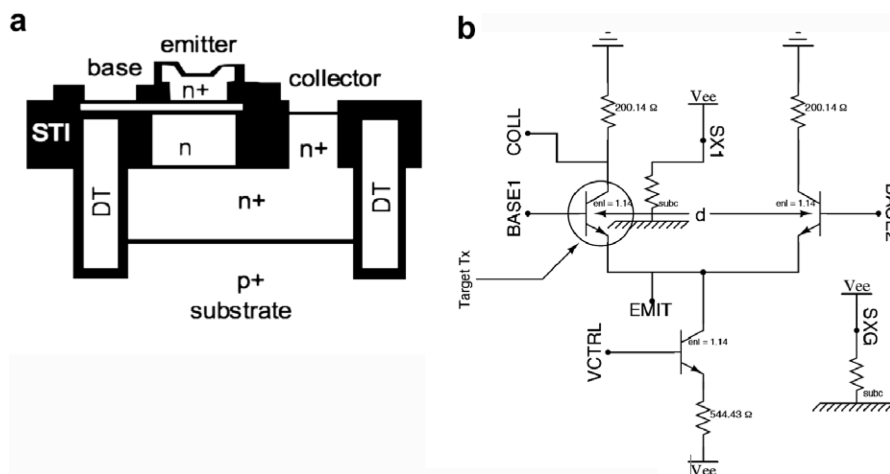

Fig. 1. (a) Cross-section of SiGe HBT. (b) ECL circuit used for microbeam irradiation of target HBT.

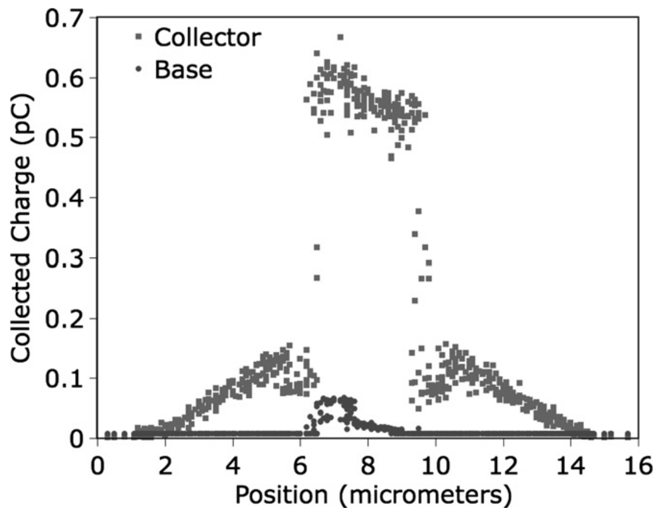

Fig. 2. Charge collection by the collector and base of the target HBT for various microbeam spot locations.

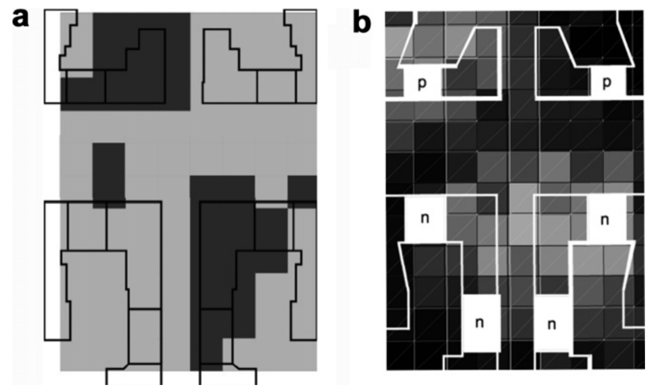

Fig. 3. (a) TCAD simulation results showing the areas (in dark gray) that produce an SEU for ion LET = 6 MeV cm^2/mg. (b) Measured average SEU results from microbeam testing showing the areas (in light gray) that produce an SEU for 36 MeV oxygen ion.

The charge collection on the collector is significantly higher than that on the base and the physical area for collector charge collection is much large than that for the base. Given the overburden describe above, approximately 12 MeV will be deposited in the silicon, or 0.53 pC of charge will be liberated. Note that this is near the maximum value collected by the collector. These data are very similar to those published on single HBTs with fixed bias on each contact and represent a validation of the analysis and modeling in several papers [4–7, and references within].

3. Validation of TCAD simulations of single event upsets (SEUs) in 0.25 μm CMOS

Detailed 3D mixed-level TCAD simulations were performed on one cell of a commercial 4 Mbit SRAM. Most of the memory cell transistors were modeled in a single TCAD description, i.e. a large fraction of the active semiconductor was built in TCAD. The TCAD model was developed via calibration of electrical characteristics of 2D and 3D discrete transistor models to known device characteristics, e.g. I_d–V_g data. To ease the burden of device simulation, the local interconnects and large portions of polysilicon were replaced with SPICE components. Device cross-section and doping profile information were provided by the vendor and SEM analysis.

Over 176 TCAD simulations were performed. The purpose of the TCAD simulations was to understand the topology of the SRAM cell's SEU sensitive area to 36 MeV ^{16}O ions normally-incident to the cell surface. The SEU simulations were performed by rastering a particle strike over the entire surface of the cell. The steps were 0.25 μm in both the x and y dimensions. For each x–y pair, a TCAD simulation was done to determine if the ionizing-radiation-induced a SEU. Fig. 3(a) shows SEU results for a stopping power of 6 MeV-cm^2/mg (the radiation effects on microelectronics community typically refers to stopping power as linear energy transfer or LET). The dark gray areas define the x–y position for events that caused errors, while events in the light gray areas did not cause a SEU. The lower right region shows the drain and gate of the off NMOS device to be a portion of the sensitive area, while the top left region gives the contribution to the sensitive area of the drain and gate of the off PMOS device. These results are consistent with the classical understanding of SEUs in this type of SRAM.

Heavy ion induced SEU data were taken at SNLs microprobe facility. The probe was focused to be incident within a 1.6×1 μm^2 area. The accelerator was tuned to deliver 36 MeV ^{16}O ions on the target. The incident LET was approximately 5.2 MeV-cm^2/mg in silicon. We approximate the LET at the sensitive regions to be 6 MeV-cm^2/mg. The data are presented in Fig. 3(b). Also shown are the n- and p-regions of the cell. Note that the data show similar characteristics to those given by the TCAD simulations. This comparison provides experimental verification of the TCAD simulations, allowing for higher confidence in simulations done with other ion species.

4. Calibration of SEU sensitive volume dimensions for analysis of MBUs in a 130 nm CMOS SRAM

SNL's IBICC facility was used to help define the geometric volume used as input to a Monte Carlo radiation transport code that predicts energy deposition in multiple volumes due to an ensemble of single radiation events (more on the code later). A single transistor from IBM's 8RF 130 nm process was irradiated using the 36 MeV ^{16}O focused ion beam much like that described in the Section 2. The gate length was 1.6 μm and the gate width was 10 μm. The structures had less than 1 μm of overburden above the active region.

Fig. 4 gives the induced charge collection at the drain terminal for normally-incident ^{16}O ions for various ion spot locations. As before, a 1 μm slice of the data was

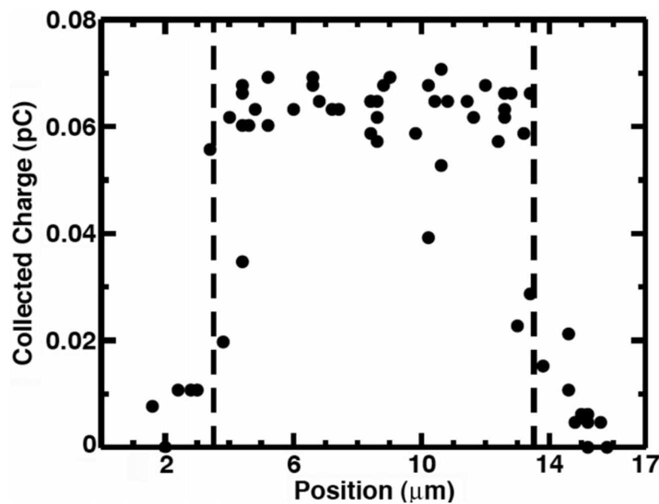

Fig. 4. Charge collected by drain of the target NFET for various microbeam spot locations.

collapsed on this plane. The data were selected to represent a cut line through the drain region parallel to the gate width. The dotted lines enclose the drain diffusion region of the device. Charge collection in this region peaks near 0.065 pC and quickly falls to zero outside the drain diffusion. The linear energy transfer (LET) of 36 MeV ^{16}O ion is near 5.2 MeV-cm^2/mg in silicon. Using the density of silicon and the fact that one e–h pair will be created when the ion loses 3.6 eV to ionization allows for conversion of this LET to a charge generation per micrometer rate, i.e. 0.052 pC/μm. From the maximum collected charge and the charge generation rate, we can determine the thickness of the collection volume region by determining the ion path length required to deposit an amount of energy equivalent to a charge generation of 0.065 pC, e.g. 0.065 pC/0.052 pC/μm = 1.2 μm. Of course this method assumes that the ion stopping power is constant over a range longer than the path length of interest, which is true for a 36 MeV ^{16}O ions moving through 1.2 μm of silicon. This result is consistent with TCAD device simulations given in [8].

Given this collection volume depth and the physical area of the drain diffusion, we defined a set of sensitive volumes that represent an array of memory cells in an SRAM [9]. The details of the cell size and layout were developed from proprietary information provided by IBM. We used this as input to our virtual irradiator call MRED (Monte Carlo radiative energy deposition, developed by researchers at Vanderbilt University). MRED is a Geant4 application. Geant4 is a library of c++ routines assembled by an international collaboration for describing radiation interactions with matter. MRED was structured so that all physics relevant for this radiation effects application was available at run time. In [9], we used MRED to determine the probability of proton-induced MBUs in an SRAM designed in the 130 nm IBM 8RF process. The simulations predict a single event response that has a strong dependence on the angle of proton incidence.

5. Conclusion

We demonstrate several uses for SNL's microprobe facility to support modeling efforts to assess SEEs in modern technologies. The ion microprobe has been shown to be a valuable tool for model calibration and validation. As microelectronic technologies advance, the current microprobe facilities must change to allow for these types of assessments to continue. One major limitation is the ion energy that is available at current facilities. Microelectronic fabrication processes are moving towards much thicker overburdens, e.g. nine metal layers that are over 16 μm thick. Overlying metallization and dielectric stacks of this thickness severely limit the penetration range of ions into the active silicon, reducing the signal induced on the circuit nodes in question, making accurate measurements difficult or impossible.

Acknowledgement

Sandia is a multi-program Laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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Multiple-Bit Upset in 130 nm CMOS Technology

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***Abstract*—The probability of proton-induced multiple-bit upset (MBU) has increased in highly-scaled technologies because device dimensions are small relative to particle event track size. Both proton-induced single event upset (SEU) and MBU responses have been shown to vary with angle and energy for certain technologies. This work analyzes SEU and MBU in a 130 nm CMOS SRAM in which the single-event response shows a strong dependence on the angle of proton incidence. Current proton testing methods do not account for device orientation relative to the proton beam and, subsequently, error rate prediction assumes no angular dependencies. Proton-induced MBU is expected to increase as integrated circuits continue to scale into the deep sub-micron regime. Consequently, the application of current testing methods will lead to an incorrect prediction of error rates.**

***Index Terms*—Energy deposition cross section, multiple-bit upset (MBU), MRED, single event upset (SEU), SRAM, proton effects.**

I. Introduction

THE scaling of integrated circuits has decreased the amount of charge required to cause single event effects (SEE) in highly-scaled technologies. However, the total sensitive volume has also decreased, which tends to reduce the SEE cross section. These competing effects have led to a variety of SEE responses in highly-scaled technologies. For proton interactions in bulk CMOS technologies, little or no change in single-event upset (SEU) rates has generally been observed, while multiple-bit upset (MBU) has increased [1]. Multiple errors in the same word may reduce the effectiveness of traditional error detection and correction (EDAC) codes [2]. Additionally, proton ground testing does not account for device orientation or angle of incidence. It has been shown that proton-induced SEE may depend on angle of incidence, which must be taken into account for accurate error rate prediction [3].

Recent studies have looked at characterizing the nature of MBU for memory designs [4]–[6]. The effectiveness of EDAC, process variations, and cell interleaving to mitigate MBU have been investigated for the 90 nm and 130 nm technology nodes. The probability of MBU has been shown to increase for smaller technologies [5], [7], [8].

II. Background

The mechanisms for proton-induced SEE differ from those of heavy ions. While ionization from the incident particle is primarily responsible for SEU due to heavy ions, protons are too lightly ionizing to be of concern. Rather, proton SEE response is dominated by nuclear reactions and recoils that produce more ionizing secondary products. These proton-induced nuclear events have been shown to produce an increase in MBU cross section for dynamic random access memory (DRAM) at large angles of incidence [9]. A scaling study using a nuclear high energy transport code suggested that nucleon-induced MBU in static random access memory (SRAM) would increase as feature size decreased [8].

Fig. 1 is an example of a 63 MeV proton-induced nuclear reaction generated by MRED (Monte Carlo Radiative Energy Deposition) in a memory array. MRED is a GEANT4 based tool [10]–[14]. The shaded boxes represent sensitive regions of the silicon, each corresponding to one bit in a memory array. The incident proton enters at a grazing angle and reacts with the silicon to cause a nuclear event. A 14 MeV oxygen ion is emitted from the reaction that traverses six, darker shaded, sensitive volumes. The amount of charge generated in each sensitive volume is included in the figure; if this charge is greater than the critical charge, all of the cells may upset. The other nuclear-reaction products also are labeled in the figure.

Integrated circuits in current technologies have feature sizes smaller than the track size of these radiation events. Therefore, accounting for the microstructure of these nuclear events is critical. Cell spacing in highly scaled technologies is now less than the range—the distance traveled—of these secondary products and an increase in MBU is expected.

Using the MRED code, it was previously shown that metallization can significantly impact radiation response by the presence of high-Z materials near the sensitive volume [10]–[12].

Manuscript received July 14, 2006. This work was supported by the NASA Electronic Parts and Packaging Program and Defense Threat Reduction Agency Radiation Hardened Microelectronics Program under IACRO06-4012I to NASA. Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000. The computational portion of this wok was conducted through Vanderbilt University's Advanced Computing Center for Research and Education (ACCRE), Nashville, TN 37235.

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Digital Object Identifier 10.1109/TNS.2006.884789

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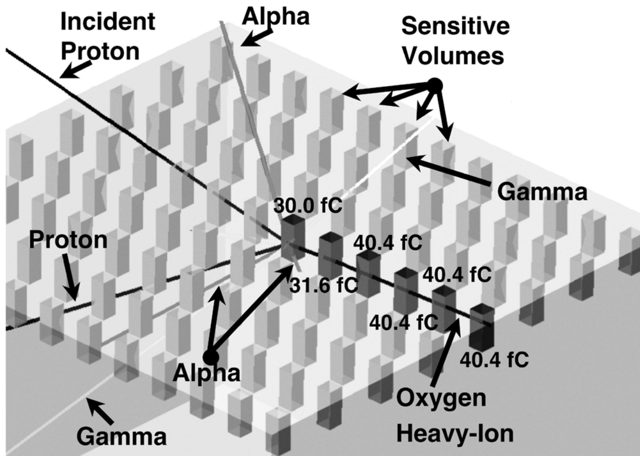

Fig. 1. TCAD representation of an MRED generated nuclear event for a 63 MeV proton at a grazing angle in silicon with the appropriate sensitive volumes. The overlayers have been omitted. The secondary products from the reaction are a 14 MeV oxygen ion, a proton, gamma rays, and alpha particles. The oxygen heavy-ion transverses six sensitive volumes and the charge generated in each volume is labeled.

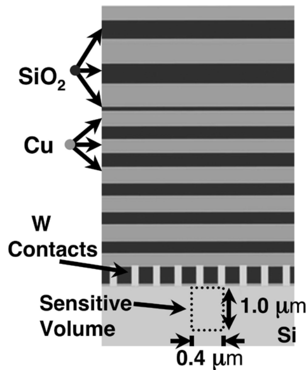

Fig. 2. TCAD representation of the device overlayers. This structure was imported for MRED simulations.

Neglecting the overlayers leads to incorrect prediction of the upset cross section. In this work, we analyze proton-induced energy deposition in a 130 nm SRAM and correlate it to MBU cross section. We show that proton-induced MBU cross section is expected to increase significantly with angle and the probability of MBU for this technology is sufficiently high to be of concern.

III. Device and Circuit Characteristics

The IBM 8RF 130 nm process was selected for this study. A 3-dimensional technology computer aided design (TCAD) structure was created based on a high-density SRAM in this process. The structure contained all metal and passivation overlayers with accurate dimensions taken from [15]. This structure, shown in Fig. 2, was then imported into MRED for energy deposition simulations.

A. Sensitive Volume Definition

The process was characterized to determine the sensitive volume size and spacing. Sensitive volume characteristics were derived from layout information, experimental data, and device simulation [15], [16].

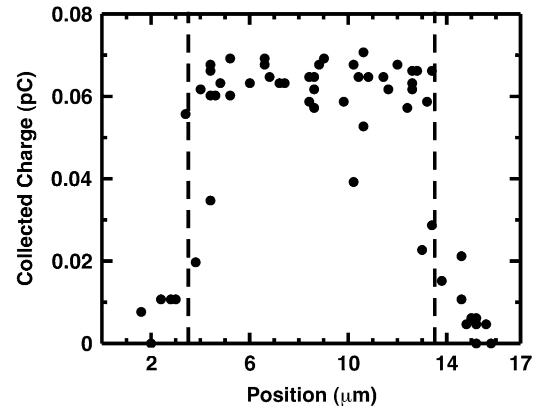

Fig. 3. Collected charge at the drain for 36 MeV oxygen ions normally incident to the surface. The active diffusion is bounded by the dotted lines and extends from 3.5 μm to 13.5 μm. Charge collection drops off quickly outside the diffusion region of the device and a well defined sensitive volume is assumed. From these data, a charge collection depth of 1 μm was estimated.

Transistor test structures were used to determine charge collection depth and charge collected by diffusion at Sandia National Laboratory's ion beam induced charge collection (IBICC) facility as in [17]. This method involves irradiating the devices at a known position (± 1 μm) and monitoring the charge collected at each terminal. From these data the depth of charge collection can be calculated.

The microbeam data on these structures were taken with 36 MeV O ions. The gate length was 1.6 μm and the gate width was 10 μm. The test structures had minimal overlayer materials above the active regions.

Fig. 3 shows the charge collected at the drain terminal for normally incident oxygen ions as a function of strike location. The dotted lines enclose the diffusion region of the device parallel to the gate width. Charge collection in this region peaks at 0.07 pC and quickly drops off outside the active region. The collection volume is well defined by the device geometry. The linear energy transfer (LET) of 36 MeV oxygen ion is 7 MeV$\cdot$ cm^2/mg at normal incidence. From the maximum collected charge of 0.07 pC, a worst case collection depth of 1 μm was estimated, which is consistent with device simulations in [16].

The corresponding sensitive volume was defined to represent the most vulnerable node of the SRAM cell. The sensitive volume for this process was estimated to be $0.4\mu\text{m} \times 0.4\mu\text{m} \times 1.0\mu\text{m}$. The $0.4\mu\text{m} \times 0.4\mu\text{m}$ dimensions were derived from the minimum active diffusion area of the process and the 1 μm depth from the charge collection measurements of the transistor test structures.

B. Charge Sharing

A charge collection mechanism at multiple well contacts has been identified in this technology and reported in [16]. This charge sharing mechanism occurs when charge generated by heavy ion interactions in silicon induces charge collection on nearby passive nodes not struck by the incident particle. Fig. 4 (taken from [16]) shows the charge collected by the nearest sensitive node in this process. These results demonstrate that the proton-induced secondary products are not sufficiently ionizing to produce charge sharing effect in this technology. The charge

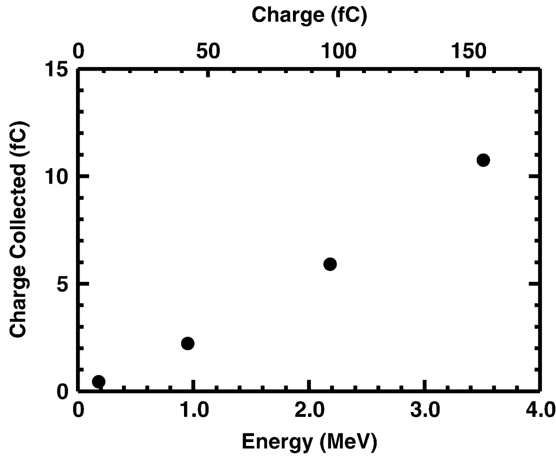

Fig. 4. Charge sharing for an SRAM in this 130 nm process. Charge collection on nearby nodes is negligible for energy deposition due to protons.

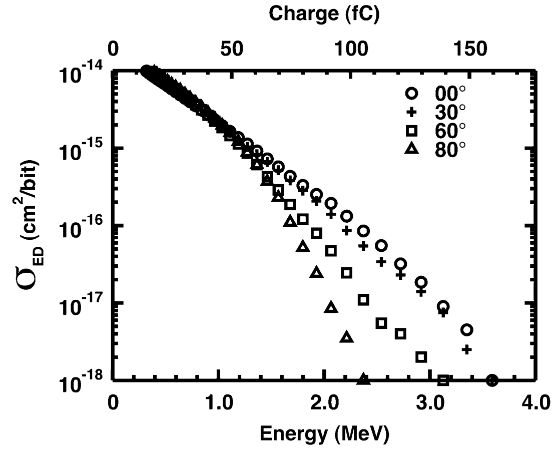

Fig. 5. Single volume energy deposition cross section for 63 MeV protons. An angular dependence is seen at E greater than 1 MeV.

sharing effect is also reduced by the spacing of the sensitive volumes. For the highest—and least probable—energy deposition events, energy deposition of 4 MeV on a node would result in charge collection of only 11 fC on the nearest sensitive node. For less energetic—and more probable—events, only 5 fC of charge would be collected at the nearest sensitive node. Thus, proton induced upsets due to charge sharing phenomena are not a concern for this technology.

IV. Energy Deposition

The simulation tool MRED is a Monte-Carlo, Geant4 based transport code used to model energy deposition in semiconductor devices. The code was used to simulate ionization and nuclear processes in these devices to create a statistical energy deposition profile as in [10]–[12].

A. Simulation Method

The TCAD model was imported into MRED. An array of 204 sensitive volumes, equivalent to the sensitive volumes in a 20μm $\times$ 20μm area, was placed in the structure. The spacing of the sensitive volumes was based on the SRAM cell dimensions of 1.9 μm $\times$ 1.3 μm.

MRED was used to simulate irradiation of the structure with protons at 63 MeV and 200 MeV, two common test energies. For each proton event, MRED tracked the energy E in each sensitive volume by the primary proton and secondary particles. The device was exposed to a simulated fluence of 1×10^{14} protons/cm^2. This is equivalent in the number of events to a 1×10^{10} protons/cm^2 fluence for a 2 Mbit SRAM. The corresponding data for each event were post-processed to calculate the energy deposition cross section.

B. Results

The energy deposition cross section $\sigma_{\rm ED}(E)$ is the cross section to deposit energy E or greater in the sensitive volume and is calculated by (1), where N is the number of events that deposited energy of E or greater and ϕ is the fluence [18]

$$\sigma_{\rm ED}(E) = \frac{N}{\phi}. \tag{1}$$

The relationship between $\sigma_{\rm ED}(E)$ and the SEU cross section $\sigma_{\rm SEU}$ is given by (2), where the critical charge $Q_{\rm Crit}$ is the charge collection on the sensitive node required to induce upset. That is, $\sigma_{\rm ED}(Q_{\rm Crit})$ is the measured $\sigma_{\rm SEU}$ during testing

$$\sigma_{\rm SEU} = \sigma_{\rm ED}(Q_{\rm Crit}). \tag{2}$$

Fig. 5 shows $\sigma_{\rm ED}(E)$ for 63 MeV protons. The energy deposition cross section is independent of angle for energies below 1 MeV, but shows an angular dependence at higher energies. Devices with low upset threshold, such as DRAMs, would show no angular dependence during proton testing, consistent with previous observations [3], [9]. The decrease in $\sigma_{\rm ED}(E)$ at increased angles of incidence is due to the aspect ratio of the sensitive volume and the scattering direction of the most energetic secondary products. The most energetic secondary products at this energy tend to scatter in the direction of the incident proton [3]. The aspect ratio creates an elongated sensitive volume with a longer depth dimension. The longer path lengths through the sensitive volume are achieved at near-normal incidence while the shortest is in the lateral direction at grazing angles. A longer path length allows more charge to be generated and collected. The shape of the sensitive volume strongly influences the single volume charge collection response. For SOI devices, increasing SEU cross section with respect to angle of incidence has been observed [3]. The shape of SOI sensitive volumes are different than the one presented here. In those volumes, the lateral dimension is longer than the depth and SEU response should be expected to increase.

The multiple volume energy deposition cross section $\sigma_M(E)$ is the cross section to deposit E or greater in two or more sensitive volumes. The relationship between $\sigma_M(E)$ and the MBU cross section is given by (3), where $Q_{\rm Crit}$ is assumed to be the same for each cell

$$\sigma_{\rm MBU} = \sigma_M(Q_{\rm Crit}). \tag{3}$$

Fig. 6 shows $\sigma_M(E)$ at various angles of incidence for 63 MeV protons. The computed $\sigma_M(E)$ for a fixed E increases

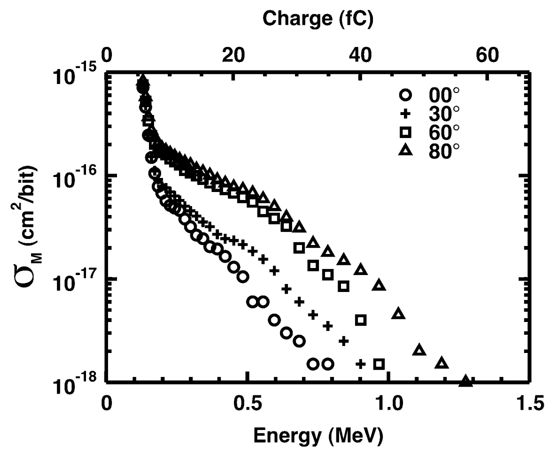

Fig. 6. Multiple volume energy deposition cross section for 63 MeV protons. The cross section shows a strong angular dependence that can vary over an order of magnitude from normal incidence to grazing angles.

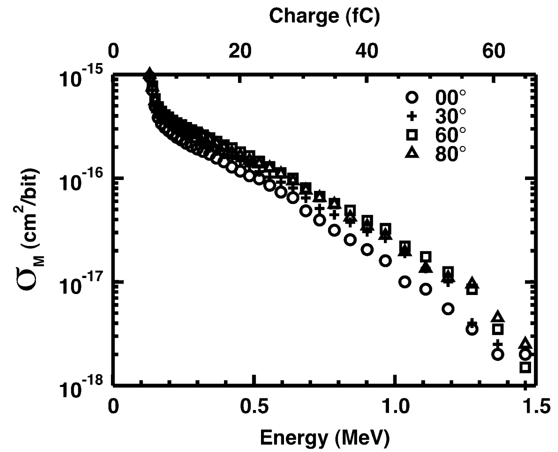

Fig. 8. Multiple volume energy deposition cross section for 200 MeV protons. The cross section has no angular dependence.

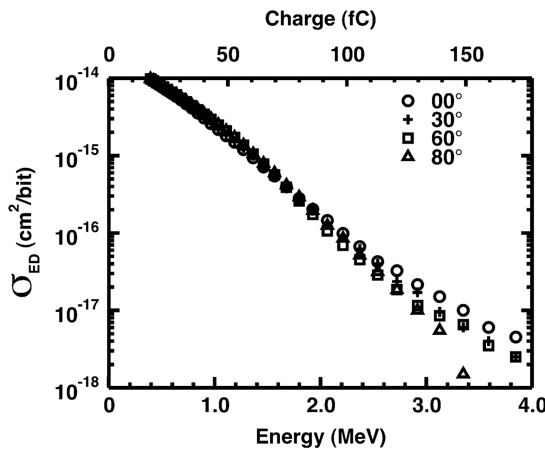

Fig. 7. Single volume energy deposition cross section for 200 MeV protons. Only a slight dependence with angle can be seen at high energies.

with angle due to the longitudinal scattering of secondary products in the sensitive volume plane. For this energy, protons normally incident to the sensitive volume plane produce secondary particles that travel into the silicon bulk and away from the sensitive region, traversing a minimal number of sensitive volumes. As the angle of incidence increases, the scattered products travel through the plane of sensitive volumes and $\sigma_M(E)$ increases.

Fig. 1 is a typical example of MBU for 63 MeV protons. The event was generated in the TCAD structure by MRED. The proton is incident at 80° and the nuclear reaction produces a 14 MeV oxygen heavy-ion. The secondary heavy-ion moves in the direction of the incident proton and traverses six sensitive volumes. The charge generated in the sensitive volumes have a range of 30–40 fC. In addition to the heavy-ion, a proton, gamma rays, and alpha particles are produced. Each of these particles deposits energy, but only the oxygen ion is sufficiently ionizing to induce upset.

Fig. 7 shows $\sigma_{\rm ED}(E)$ for 200 MeV protons. The cross section is independent of angle, with only a slight separation of the curves for energies above 2 MeV. This trend is consistent with previous observations for higher energy protons in [3] and [19]. For 200 MeV protons, transversally directed residual nuclei are more energetic and less angular dependence is expected [3].

The $\sigma_M(E)$ for 200 MeV protons is shown in Fig. 8. These cross sections do not vary with angle, again consistent with the distribution with respect to angle of secondary products.

V. Discussion

A. Critical Charge

Critical charge, the amount of charge required to induce upset, is specific to each cell design. For an SRAM cell, charge collected on the drain of a transistor changes the node potential and inverts the logic state. The value of critical charge can be found through device simulation, circuit simulation, or heavy-ion testing. Heavy-ion data collected on this SRAM cell suggest $Q_{\rm crit}$ is approximately 20 fC [20]. Figs. 9 and 10 show the correlated SEU and MBU cross sections due to 63 MeV protons, respectively, for several values of $Q_{\rm Crit}$. There is no SEU angular dependence for protons at this $Q_{\rm Crit}$ value, but the MBU cross section depends on angle. There is nearly an order of magnitude difference in $\sigma_{\rm MBU}$ for normally incident protons compared to those at grazing angles.

An SRAM hardening technique makes use of resistive and capacitive elements in the feedback network. This method is effective at increasing the $Q_{\rm Crit}$ of the cell with little area penalty. As can be seen in Fig. 9, hardening this cell to increase $Q_{\rm Crit}$ to 100 fC would result in reduced $\sigma_{\rm SEU}$, but introduce angular dependence. Given the longest path length through this sensitive volume, 1.15 μm, an LET threshold of 9 MeV $\cdot$cm^2/mg would be required for upset. Note that for this value of critical charge, no MBU would be expected.

B. Multiple Volume Probability

The probability of MBU is defined as the proportion of SEUs that result in MBUs. It has been shown for a 65 nm CMOS technology that 10% of nucleon-induced upsets may result in MBU [1]. While circuit hardening and EDAC are highly effective at correcting SEU, MBU for several bits will render the methods

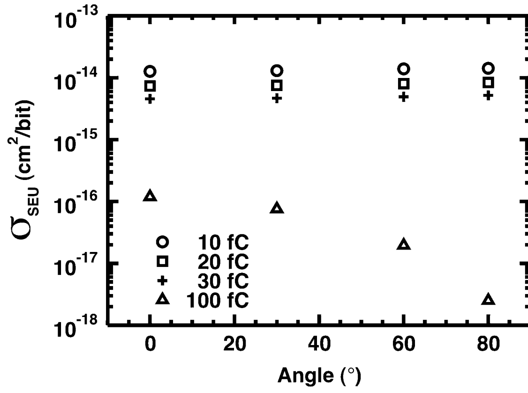

Fig. 9. Correlated $\sigma_{\rm SEU}$ versus angle of incidence for $Q_{\rm Crit}$ for 63 MeV protons. Hardening this cell to a $Q_{\rm Crit}$ of 100 fC would result in an angular dependence.

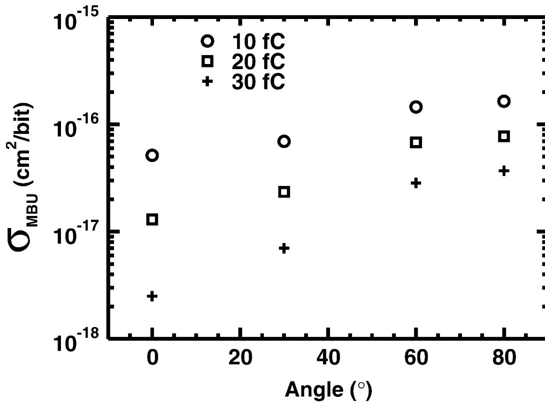

Fig. 10. Correlated $\sigma_{\rm MBU}$ versus angle of incidence for $Q_{\rm Crit}$ for 63 MeV protons. Hardening this cell to a $Q_{\rm Crit}$ of 100 fC would result in no MBU.

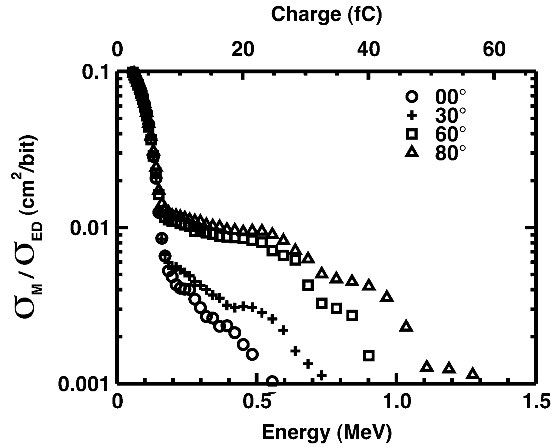

Fig. 11. Probability of multiple volume energy deposition for 63 MeV protons. The probability increases with increasing angle of incidence.

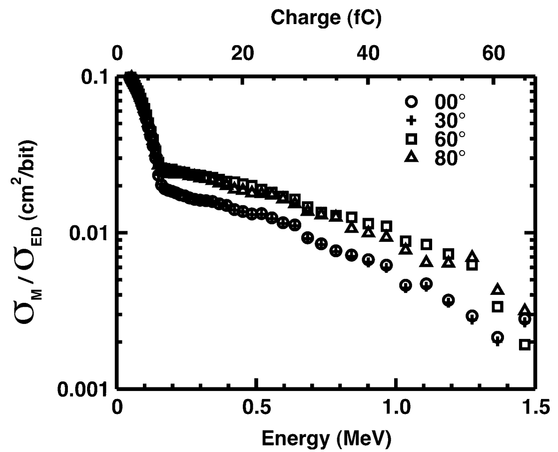

Fig. 12. Probability of multiple volume energy deposition for 200 MeV protons. The slight difference in cross sections is within the margin of error.

less effective. As a result, circuit hardening techniques, memory design, and process all are factors in memory reliability.

Figs. 11 and 12 show the computed ratio of $\sigma_M(E)$ to $\sigma_{\rm ED}(E)$ for 63 MeV and 200 MeV protons, respectively. From these data the probability of MBU can be correlated for a known $Q_{\rm Crit}$. The ratio increases as the angle of incidence increases for the 63 MeV case, but the ratios across all angles for the 200 MeV case are within the margin of error. These data suggest that the probability of MBU for $Q_{\rm Crit}$ of 5–20 fC is approximately 1%, consistent with the trends observed in [1] for both energies. For devices with a lower $Q_{\rm Crit}$, the probability of MBU approaches 10%.

C. Testing

Proton testing traditionally assumes that upset cross section does not depend on the angle of incidence. Data taken from proton testing at different energies is usually fit using Bendell or Weibull methods. CREME96 uses these fits, along with proton fluxes in a specific environment, to calculate error rates. However, since this method makes the assumption that the proton cross section does not depend on angle, the resulting error rate prediction may be inaccurate. As shown for the SRAM considered here, devices with high critical charge may exhibit angular dependency for both SEU and MBU.

VI. Conclusion

Simulation using MRED has been used to characterize energy deposition in a 130 nm SRAM for 63 MeV and 200 MeV protons. The device models include all metallization layers and geometries specific to the process. For events depositing low to moderate energy, SEU does not depend on the angle of incidence for proton irradiation. For higher energy events, the SEU angular response is dominated by the aspect ratio of the sensitive volume. The MBU response is dominated by the trajectories of secondary products produced by proton irradiation and the MBU probability increases with increasing angle of incidence.

The probability of MBU at the 130 nm technology node approaches 1%. The trend toward an increasing proportion of MBU is expected to increase as device scaling pushes feature sizes well below the range of most heavy-ion nuclear reaction products. This probability will change significantly with the angle of incidence of proton irradiation. Ground based proton testing must account for angle of incidence to correctly predict soft error rates.

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High Energy Neutron Multiple-Bit Upset

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***Abstract*— Neutron-induced multiple-bit upsets (MBU) in a 90nm CMOS SRAM are examined using Monte-Carlo simulations. While the single-bit upset (SBU) cross section is nearly independent of angle, the probability of MBU increases for neutrons incident at grazing angles.**

***Index Terms*— multiple-bit upset, neutron, soft error, radiation effects**

I. INTRODUCTION

Advanced integrated circuits are susceptible to upsets initiated by neutrons [1]. Neutron-induced nuclear reactions produce showers of ionizing particles that may change the state of one or more cells within the circuit. An event that changes the state of one cell is described as a single-bit upset (SBU), while an event that affects more than one cell is designated as a multiple-bit upset (MBU).The combined effects of changes in sensitive volume size and supply voltage have generally resulted in an approximately constant SBU cross section for different complementary metal-oxide-semiconductor (CMOS) process generations [2]. However, the fraction of incident particles that result in multiple-bit upsets has increased in recent technology generations [3]. For static random access memory (SRAM), scaling has decreased the distance between sensitive volumes, making MBU more likely. The increasing problem of MBU also must be considered in the context of memory architecture, layout, and design for state-of-the-art and future technology nodes.

In this work we examine neutron-induced MBU for a 90 nm CMOS technology. The physical mechanisms for MBU are examined using the MRED (Monte Carlo Radiative Energy Deposition) code [4, 5]. MBU in this technology shows increased probability for neutrons incident at grazing angles.

Manuscript received February 15, 2007. This work was supported in part by the NASA Electronic Parts and Packaging Program and the Defense Threat Reduction Agency Radiation Hardened Microelectronics Program under contract IACRO06-4012I to NASA.

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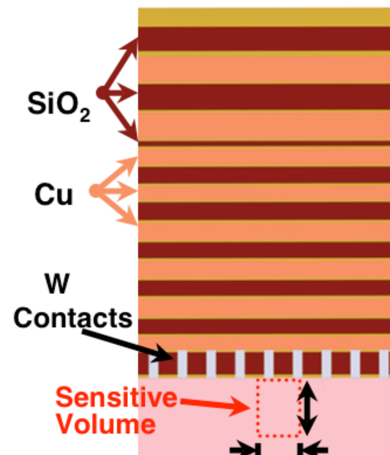

Fig. 1. Cross section view of the TCAD model used for radiation simulation. The model includes overlayers with materials and dimensions specific to the process under study. The location of a single sensitive volume is highlighted in the silicon bulk.

II. SIMULATIONS

All results presented here were obtained for a 90 nm CMOS technology. A 3-dimensional technology computer aided design (TCAD) structure was created based on a high-density SRAM that was fabricated in this process. The simulation structure included all metal and passivation overlayers present in the physical circuit. The structure cross section is shown in Fig. 1.

The simulation tool MRED was used for this study. MRED is a Monte Carlo, Geant4-based high energy transport code used to model energy deposition in semiconductor devices [4, 5]. The code simulates ionization and nuclear processes in electronic devices using detailed descriptions of the device structure. The code generates a detailed energy deposition profile [6].

The TCAD structure was imported into MRED and neutron irradiation was carried out using the Los Alamos WNR beam flux spectrum. Neutron transport through the TCAD structure was simulated in MRED. Corresponding sensitive volumes for an array of 400 SRAM cells were included in the structure. The dimensions of each sensitive volume were 0.4 µm × 0.4 µm × 1.0 µm, based on the drain size of an off-state NMOS transistor.

For each neutron event, MRED tracked the energy E in each

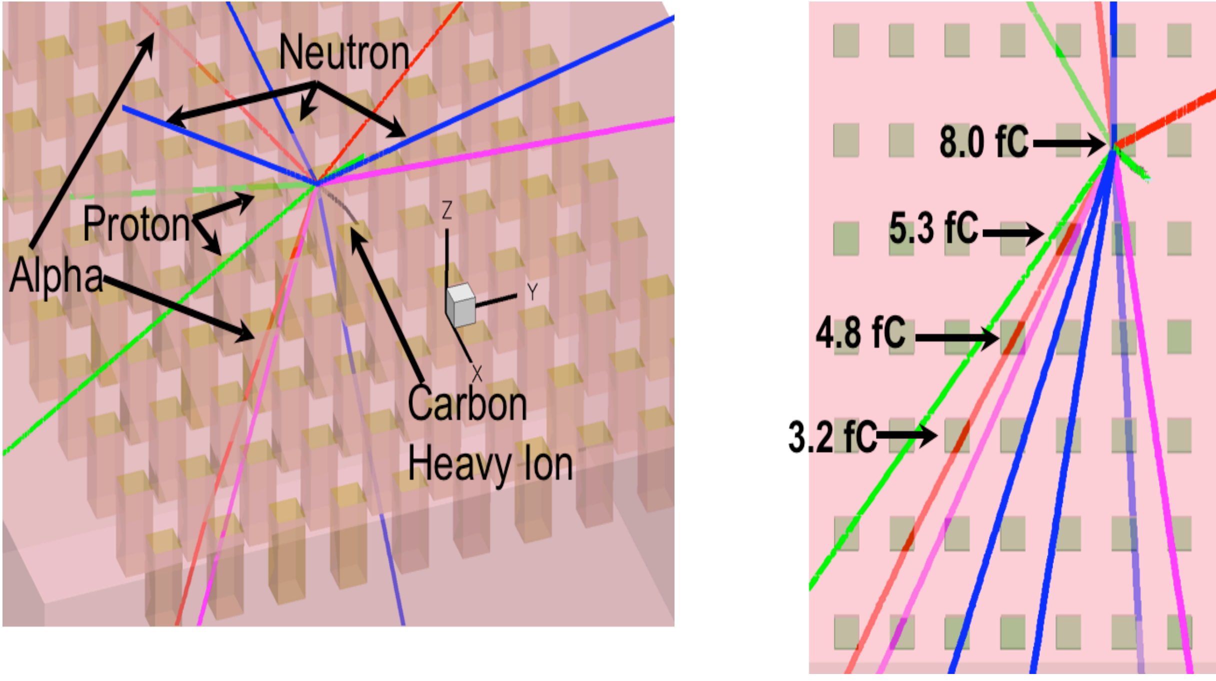

Fig. 2. A TCAD representation of an MRED generated nuclear event. The gold volumes represent the sensitive volumes of the device. The incident neutron enters and induces a nuclear event. The shower of secondary particles include alpha particles, protons, neutrons, and an carbon heavy ion. In the top-down view on the right, generated charges for sensitive volumes with more than 1 fC of charge are labeled.

sensitive volume though all physical processes by the incident neutron and the resulting secondary particles. The device was exposed to a simulated fluence of 10^{14} neutrons / cm^2. The recorded energy deposition for each neutron event and the overall energy deposition cross section were calculated based on the methods described in [6]. Simulated irradiations were performed at 0°, 45°, and 90° angles of incidence.

III. Results

Neutrons cannot produce upsets directly because they are not ionizing. The mechanism for neutron-induced upsets is through neutron-nucleus interactions. The reaction products may induce upset. Fig. 2 shows a typical nuclear event as obtained from MRED.

Simulation results were processed to create statistical energy deposition profiles. The single volume energy deposition cross section σ_{ED} and multiple volume energy deposition cross section σ_M are given by

$$\sigma_{ED}(E) = \frac{N_i}{\phi} \tag{1}$$

$$\sigma_M(E) = \frac{N_m}{\phi} \tag{2}$$

where N_i is the number of sensitive volumes with energy E or greater and N_m is the number of neutron events inducing MBU for energy E or greater. For this study, MBU is defined as any single neutron event inducing upset in more than one sensitive volume. σ_{ED} and σ_M are shown in Fig. 3 and Fig. 4 respectively for various angles of incidence.

From the σ_{ED} and σ_M, SBU and MBU cross section can be calculated for a known critical charge. Critical charge Q_{CRIT} is the amount of charge required to induce upset. The value Q_{CRIT} for a given circuit is primarily a function of nodal capacitance [7]. Sufficient charge must be collected at a node to induce upset. The MRED-calculated σ_{ED} evaluated at Q_{CRIT} would be the expected σ_{SEU}. Likewise, the MRED-calculated σ_M evaluated at Q_{CRIT} would be the expected σ_{MBU}.

σ_{ED} exhibits a small decrease at grazing angles while σ_M increases with increasing angle of incidence. The fraction of MBU is defined by

$$\text{Fraction of MBU} = \frac{\sigma_M}{\sigma_{ED}} \tag{3}$$

and is shown in Fig. 5. The probability of MBU increases for neutrons as the angle of incidence increases. MBU can account for 5-10% of soft errors. The fraction of MBU for several values of Q_{CRIT} is shown in Fig. 6.

IV. Discussion

Neutron test methods that assume cross section does not depend on the angle of incidence will not correctly predict MBU error rates. As shown for the technology considered here MBU shows an angular dependence. Ground based test methods must account for these dependencies.

MBU should be considered in design and layout. For memory devices, bit interleaving can mitigate MBU in a single byte. The minimum distance for this must exceed the distance of secondary products from neutron irradiation.

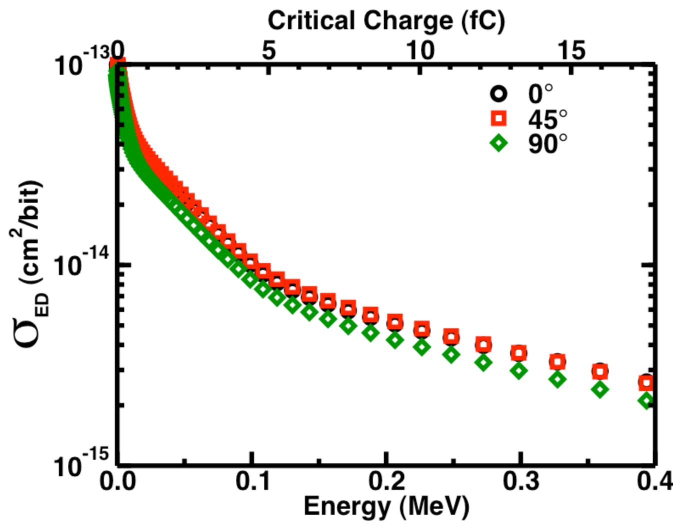

Fig. 3. The MRED single volume energy deposition cross section σ_{ED} from neutron irradiation. The cross section for a single volume decreases at grazing angles.

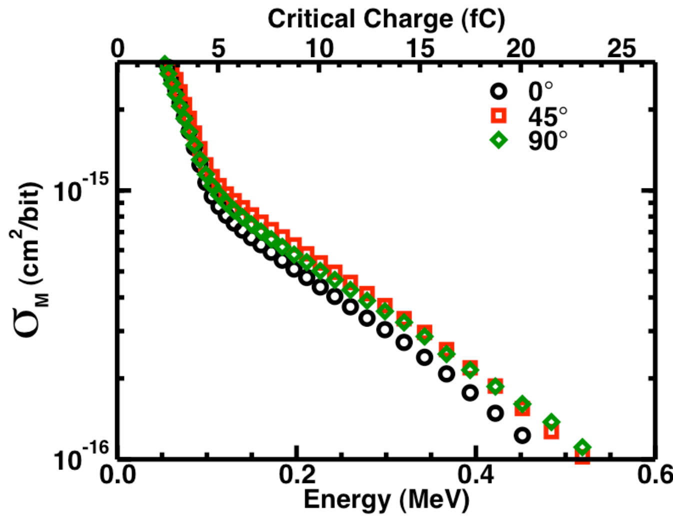

Fig. 4. The MRED multiple volume energy deposition cross section σ_M from neutron irradiation. The cross section for multiple volumes increases at grazing angles.

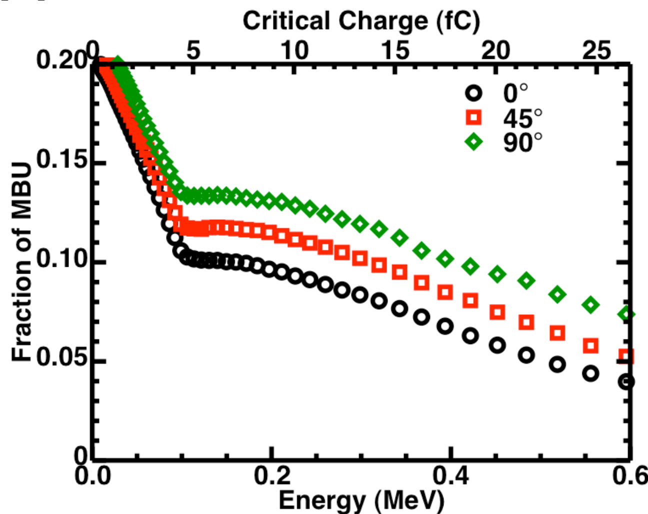

Fig. 5. The MRED fraction of MBU from neutron irradiation.

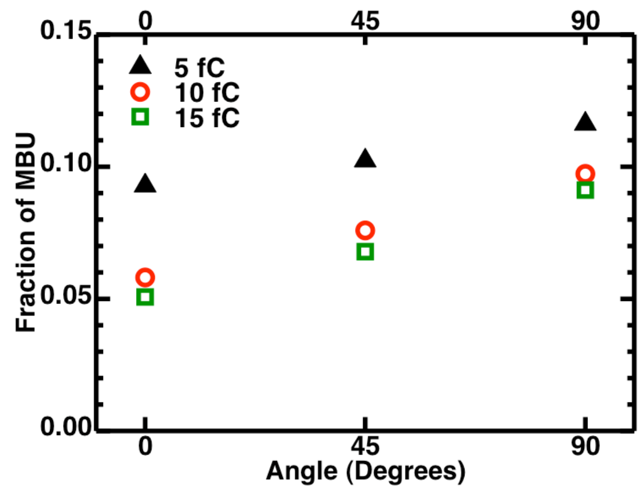

Fig. 6. The fraction of MBU for various Q_{CRIT}. The fraction of MBU events increases as the angle of irradiation increases.

V. Conclusion

Simulation of neutron irradiation for a 90 nm CMOS technology has been performed in MRED. The fraction of MBU from neutron-induced reactions tends to increase at grazing angles. As CMOS technology continues to scale, the fraction of MBU will increase.

Acknowledgements

The computational portion of this work was conducted through Vanderbilt University's Advanced Computing Center for Research and Education (ACCRE), Nashville, TN 37235.

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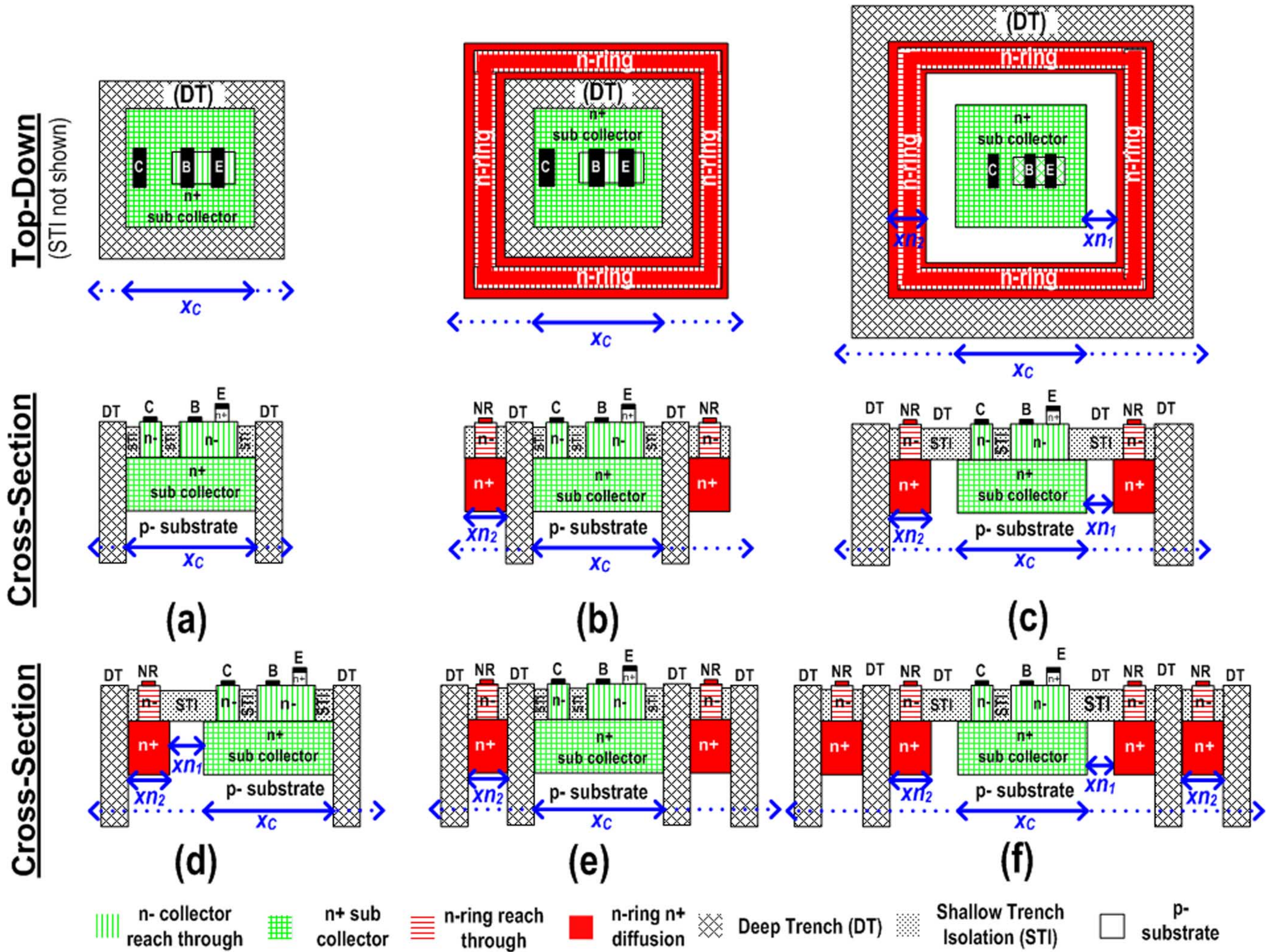

Fig. 1. Top down and cross-section views of the: (a) nominal-HBT (unhardened); (b) external R-HBT; (c) 3, 6, 8 μm R-HBT; and cross-section views of the (d) 1-sided 3 μm R-HBT, (d) 1NR, 2DT (3 μm R-HBT) (f) 2NR, 2DT (3 μm R-HBT). The key lateral dimensions x_C, xn_1 and xn_2 are shown.

II. Devices Under Test

A. RHBD Layout Variations

The SiGe HBT evaluated in this work features an $f_T/f_{\rm MAX}$ of 200/285 GHz, a $BV_{\rm CEO}$ of 1.7 V, and is offered alongside 130 nm CMOS in the commercially-available IBM 8 HP, seven metal layer (7 LM) SiGe BiCMOS process [10]. The device is fabricated on an 8–10 Ω-cm p-type substrate with an *in-situ* doped polysilicon emitter, raised extrinsic base, a conventional (5 to 7 μm) deep-trench (DT), and shallow-trench (ST) isolation. All devices are implemented in a single stripe CBE configuration, as opposed the larger double-collector, double-base stripe CBEBC configuration, featuring an emitter area (A_E) of 0.12×3.0 μm^2. The CBE configuration has a smaller internal trench area as discussed in [2]. The top down and cross section views of RHBD layout devices featuring a variety of n-ring placement and spacing are shown in Fig. 1(a)–(f). The lateral distance across the device is denoted as x_C, the width of the n-ring is denoted as xn_2, and the spacing between the internal n-ring and the device sub-collector is denoted as xn_1. The devices tested feature an n-ring width of 2 μm and a spacing varying from 3 to 8 μm. In the 8 HP process, a spacing less than 3 μm could result in an n-ring to sub-collector short as a result of dopant out-diffusion during device fabrication. A smaller n-ring spacing, allowing for a more compact and effective design, may be possible in other technology platforms with reduced doping levels. In this work we focus on the measured and simulation charge collection of the nominal-HBT, external R-HBT and the internal 3 μm R-HBT which have shown to be the most effective in SEE mitigation. Measured charge collection of alternate n-ring schemes such as the 1-sided 3 μm R-HBT (reduced $A_{\rm DT}$), 1 NR, 2 DT 3 μm R-HBT (external R-HBT + 2nd outside DT), and 2 NR, 2DT 3 μm R-HBT (internal + external R-HBT devices with a 2nd outside DT) are used to understand the charge collection dynamics.

The inclusion of the n-ring in the device layout affects neither the *dc* nor *ac* performance of the device (regardless of the applied V_{NR} or xn_1), as evidenced by the overlay of the forward-mode Gummel and f_T versus I_C characteristics shown in Fig. 2(a) and (b). In the case of the internal R-HBT devices, the maximum applicable V_{NR} (occurring when the substrate to n-ring depletion region contacts the device sub-collector) is proportional to xn_1, being reduced from 25 V at $xn_1 = 8$ μm to 9 V at $xn_1 = 3$ μm, for $V_C = V_B = V_E = 0$ V.

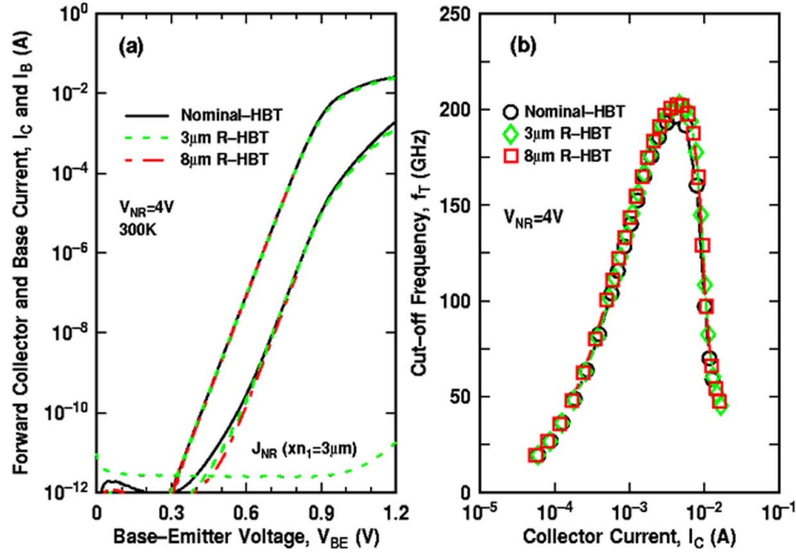

Fig. 2. RHBD impact on device performance: (a) Forward-mode Gummel comparison for the nominal-, 3 μm-and 8 μm R-HBT devices and, (b) f_T versus I_C characteristics of the nominal 3-and 8-μm R-HBT devices.

B. Experiment Details

Total ionizing dose (TID) tolerance of the 8 μm R-HBT device was evaluated via proton testing at the Crocker Nuclear Laboratory, the dosimetry system of which has been previously described in [11], [12]. Irradiations were performed to a cumulative dose of 3 Mrad (SiO_2) for $V_{NR} = \pm 3$ V with all device terminals grounded. The post-irradiation ΔJ_B for the 8 μm R-HBT is comparable to that of the nominal-HBT, indicating that TID tolerance has been maintained. This result follows from the fact that the inclusion of the n-ring does not alter the location of the emitter-base (EB) spacer and shallow trench isolation (STI) Si/SiO_2 interfaces, where radiation induced interface trap density $(D_{\rm it})$ is expected to be highest [13].

Ion microbeam testing was performed at Sandia National Laboratory's ion beam induced charge collection (IBICC) facility [14]–[16]. 36 MeV ^{16}O ions, with a 1 μm spot size, a range of 25.5 μm in Si, surface LET of 5.2 MeV-cm^2/mg and a Bragg peak of 7.5 MeV-cm ^{2}/mg were stepped across a 100×100 μm^2 field encompassing the device active area. Charge collection on the 5 terminals (C, B, E, SX and NR) were monitored for $\theta = 0^\circ$ and 15° strikes. Prior to ion exposure, a non-destructive, fluorine-based reactive ion etch (RIE) was used to selectively remove several microns of inter-metal dielectric above the device, thereby increasing charge deposition in the substrate underlying the device active area. There was no measured degradation in the device performance characteristics.

III. Microbeam Results

The 3-D charge collection data was reduced by taking a 1 μm wide slice in the y-axis direction about the peak collector collected charge (Q_C) in the x-y plane and projecting it onto the x-axis (x_C in Fig. 1). A 1 μm slice was chosen to avoid sampling too many external DT events (slice widths >1 μm), and not capturing the charge collection profile (slice widths <1 μm). The peak Q_C and the path integral of Q_C along x_C ($Q_{C,\rm INT}$) in (1) will be used as the key performance figure-of-merit for comparing the SEE mitigation capability of the various RHBD layout schemes. The peak Q_C is representative of collection resulting from an emitter center strike, whereas $Q_{C,\rm INT}$ is representative of the sum of the collection resulting from strikes across the entire length (x_C) of the 1 μm slice

$$Q_{C,\rm INT} = \int_a^b Q_C(x_C)dx_C. \quad (1)$$

Q_C is illustrated as a function of x_C, for the nominal-, 8 μm, 3 μm-, and external-HBT devices at $V_{NR} = 4$ V and $\theta = 0^\circ$ in Fig. 3. 36 MeV ^{16}O ions deposit 26 MeV of energy, generating 1.1 pC of charge in Si. Prior investigations (on IBM 7 HP), have determined a peak Q_C of approximately 1.0 pC, representing a 90% charge collection efficiency [17]. A normal incident emitter center strike will result in the largest amount of charge deposition, thereby corresponding to the observed peak Q_C. The nominal-HBT has a peak Q_C of 0.95 pC for strikes within the DT and over 0.1 pC of collector collection for external DT strikes. For the internal R-HBT device there was no observed reduction in the peak Q_C at 8 μm; however, as x_{n1} is scaled down to 3 μm, a slight reduction in peak Q_C is observed. The external R-HBT offers no immunity for strikes inside the DT but does an excellent job at reducing collection from external DT strikes.

A. N-Ring Bias

The value of V_{NR} for a given V_{SX} determines the reverse bias voltage of the substrate to n-ring junction and consequently the depletion width, electric field, electrostatic potential, and ultimately the drift-dominated charge collection volume. The path integrated collected charge for all device terminals as a function of V_{NR} is illustrated in Fig. 4(a) and (b) for the 3 μm R-HBT and external R-HBT, respectively. As expected from prior investigations [17] negligible charge collection is observed on the base and emitter. Charge collection on the remaining terminals is balanced ($Q_{C,\rm INT}+Q_{NR,\rm INT} = Q_{SX,\rm INT}$). Increasing V_{NR} yields a noticeable increase in $Q_{NR,\rm INT}$ and $Q_{SX,\rm INT}$ together

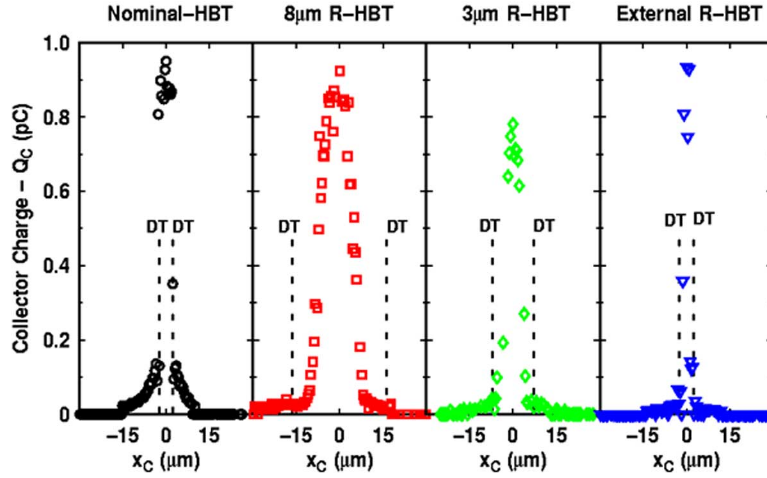

Fig. 3. Q_C as a function of x_C for the (a) nominal, (b) 8 μm, (c) 3 μm, and (d) external R-HBT. $V_{NR} = 4$ V for all R-HBT devices.

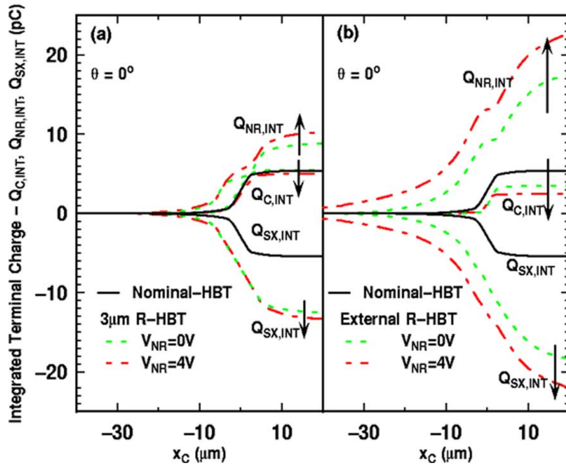

Fig. 4. Path integrated terminal charge ($Q_{C,\mathrm{INT}}$, $Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$) for the (a) 3 μm R-HBT and (b) external R-HBT for $V_{NR} = 0$ and 4V and $\theta = 0°$.

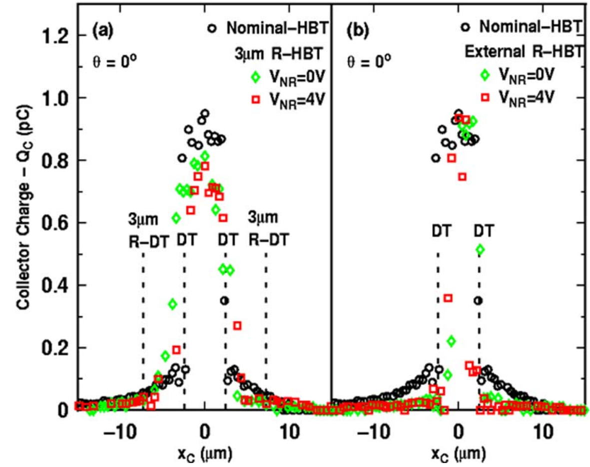

Fig. 5. Q_C as a function of x_C and V_{NR} for the (a) 3 μm R-HBT and (b) external R-HBT at $\theta = 90°$.

with a slight decrease in $Q_{C,\mathrm{INT}}$. The external n-ring collects approximately 2X more charge than the 3 μm internal ring, and demonstrates a larger percentage increase in $Q_{NR,\mathrm{INT}}$ as V_{NR} is increased. Q_C is depicted as a function of x_C at $V_{NR} = 0$ and 4 V for the 3 μm R-HBT and external R-HBT as shown in Fig. 5(a) and (b), respectively. Although the external n-ring collects 2X more charge than the 3 μm R-HBT, it offers no mitigation for emitter center strikes, while the 3 μm internal ring at $V_{NR} = 4$ V yields an 18% reduction in peak Q_C. Moreover, changes in V_{NR} have very little effect on the peak Q_C for both the internal and external ring devices.

B. *Strike Location and Angle of Incidence*

In addition to V_{NR}, the strike location (relative to the DT) and angle of incidence, θ, also impact the observed charge collection. Q_C is plotted on a logarithmic scale as a function of x_C for the nominal-, 3 μm R-HBT and external R-HBT devices at $V_{NR} = 4$ V for $\theta = 0°$ and 15° in Fig. 6(a) and (b), respectively. A strike through the center of the emitter presents the largest volume for charge deposition and un-recombined carriers are efficiently collected via drift and funneling [5]. Strike locations on the outside of the DT generate electron-hole pairs that must first diffuse under the DT before they can be collected via drift, resulting in a Q_C that is at least an order of magnitude smaller. The external n-ring provides up to 90% reduction in Q_C from strikes originating in this region, while the 3 μm ring device provides only a small reduction.

The nominal-HBT, external R-HBT, and 3 μm R-HBT all yield approximately 20% reduction in observed in peak Q_C for internal DT strikes and an increasingly asymmetric external DT collection component when θ is increased from 0° to 15°. External DT collection is also reduced, as evidenced by a rapidly decaying Q_C in the case of the nominal- and 3 μm R-HBT, and complete suppression for the external R-HBT as shown in Fig. 6(b). At $\theta = 15°$, $Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$ are also reduced (when compared to $\theta = 0°$), as illustrated in Fig. 7(a) and (b).

The effective LET, described by the inverse cosine law, ($\mathrm{LET_{eff}} = \mathrm{LET_0}/\cos\theta$) has traditionally been used to model enhanced charge collection at large θ. There have been, however, several experimental results that contradict the validity of

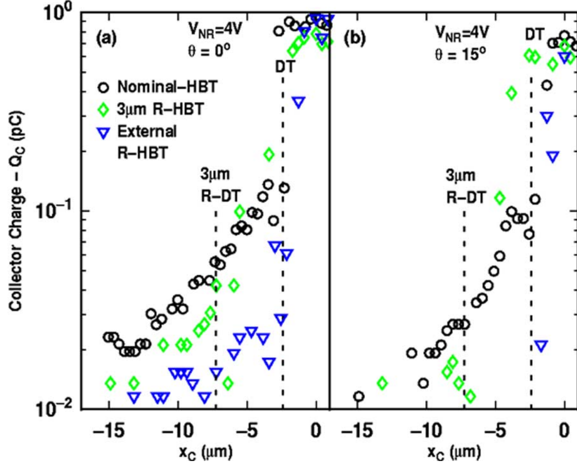

Fig. 6. External DT collection for the nominal-HBT, 3 μm R-HBT, and external R-HBT for $V_{NR} = 4$ V at (a)$\theta = 0°$ and (b) $\theta = 15°$.

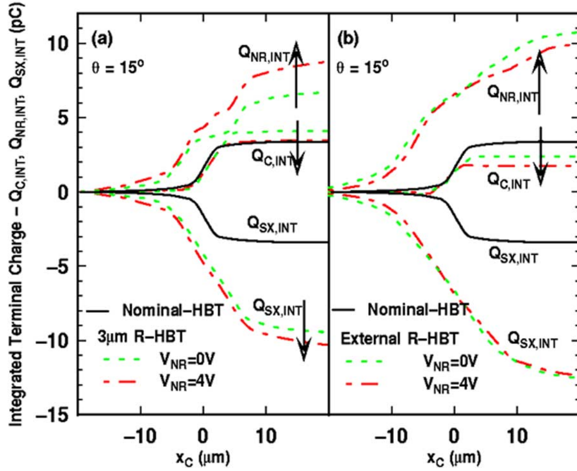

Fig. 7. Path integrated terminal charge ($Q_{C,\mathrm{INT}}, Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$) for the (a) 3 μm R-HBT and (b) external R-HBT for $V_{NR} = 0$ and 4 V and $\theta = 15°$.

this model, as discussed in [18] for the case of CMOS SRAMs. In the case of the 7 LM 8 HP process used here, a larger θ translates into an increased path length in the over-layer material, resulting in reduced ion energy (and charge deposition) in the substrate. Additionally, perturbation of the ion track through the DT may contribute to reduced internal DT collection.

C. Alternate N-Ring Schemes

One of the major drawbacks of the internal ring structure is the increase in the enclosed trench area (A_{DT}), and resulting increase in the drift dominated charge collection volume. To further reduce A_{DT}, the ring may be converted into a single- or double-tap structure, as illustrated in Fig. 1(d). Although A_{DT} is now smaller, these structures suffer from a reduction in the total n-ring area, and the resultant $Q_{NR,\mathrm{INT}}$ is reduced by almost 90% compared to the 3 μm R-HBT, as shown in Fig. 8(a). In this case the substrate to collector junction area is larger than the substrate to n-ring junction area, resulting in an increased $Q_{C,\mathrm{INT}}$. Charge balance is still maintained ($Q_{C,\mathrm{INT}} + Q_{NR,\mathrm{INT}} = Q_{SX,\mathrm{INT}}$)

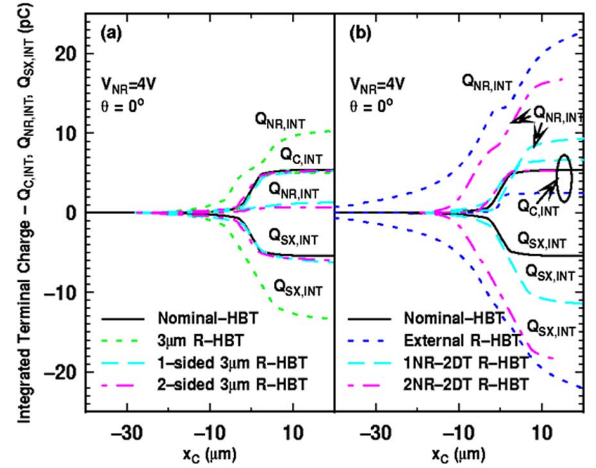

Fig. 8. Path integrated terminal charge ($Q_{C,\mathrm{INT}}, Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$) for the (a) reduced A_{DT} devices: 1-, 2-sided 3 μm R-HBT compared to 3 μm R-HBT and (b) double DT devices: 1NR-2DT R-HBT and 2NR-2DT R-HBT compared to external R-HBT. All comparisons at $V_{NR} = 0$ and 4 V and $\theta = 0°$.

The external R-HBT has demonstrated the largest reduction in external DT collection, but little mitigation in the event of an emitter center strike. The substrate to n-ring junction for this device is not bounded by DT, thereby enabling both vertical and lateral collection. Encapsulation of this external ring [i.e., going from Fig. 1(b) to Fig.1(e)] by a 2nd DT results in over 50% reduction in $Q_{NR,\mathrm{INT}}$, as shown in Fig. 8(b), as much of the lateral directed drift collection is now shut down. An obvious approach would be to combine external and internal rings in the same device. This is the case for the 2NR-2DT shown in Fig. 1(f). As shown in Fig. 8(b), $Q_{NR,\mathrm{INT}}$ increases significantly for this device with a corresponding decrease in peak $Q_{C,}$ and $Q_{C,\mathrm{INT}}$ approximately equal to that of the 3 μm R-HBT device, but at a 2X area penalty.

A summary of the observed charge collection is presented in Table I. In addition to peak Q_C and $Q_{C,\mathrm{INT}}$, the charge collected for strikes approximately 1 μm outside of the DT (the bounding trench for that specific device) is also tabulated (Q_C (DT+1)). As shown previously, the inclusion of the external n-ring results in a 90% reduction in the collected charge from events outside of the trench. This is the driving force behind the 53% reduction in the overall $Q_{C,\mathrm{INT}}$ for the external R-HBT (the best out of all devices tested). The addition of a 2nd DT on the outside of this structure [i.e., Fig. 1(e)] slightly reduces the advantage to 85% (although now events outside the trench are further away from the sub-collector).

IV. Charge Collection Simulations

3-D charge collection simulations were performed using the NanoTCAD simulation package [19], which has been previously been used to simulate radiation effects on a range of modern IC technologies [20]–[22]. Layout information, from substrate through to 1st level metal, was imported from Cadence, into a meshing utility, in GDS II format. Next, a solid geometry model of the transistor was constructed using a binary tree mesh represented as a $26 \times 26 \times 25$ μm^3 volume with local refinement of the mesh in the vicinity of

TABLE I
CHARGE COLLECTION FOR ALL DEVICES AT $\theta = 0^\circ$ AND 15°

Device	A_{DT} (μm^2)	A_{NR} (μm^2)	Q_C (E) (pC)	Q_C (DT+1) (pC)	$Q_{C,INT}$ (pC)
Nominal-HBT	11	NA	0.950	0.133	5.34
3 μm R-HBT	172	29	0.781	0.017	3.16
6 μm R-HBT	363	43	0.888	0.039	9.55
8 μm R-HBT	972	54	0.924	0.027	11.63
External R-HBT	11	59	0.935	0.012	2.48
1-sided R-HBT	24	1.2	0.878	0.115	5.36
2-sided R-HBT	37	2.4	0.845	0.102	5.36
1NR-2DT	69	16	0.978	0.021	6.68
2NR-2DT	326	68	0.749	0.020	5.33
at $\theta = 15^\circ$					
Nominal-HBT	11	NA	0.766	0.051	3.38
3 μm R-HBT	172	29	0.679	0	3.46
External R-HBT	11	59	0.602	0	1.74

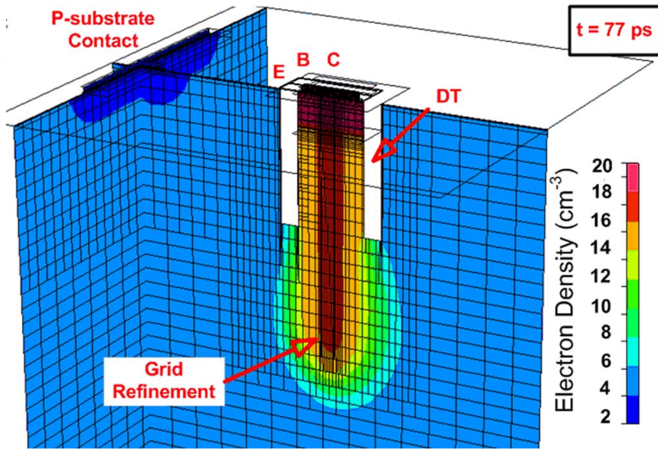

Fig. 9. X-cut through a 3-D solid geometry mesh of the nominal-HBT showing the electron density 77 ps following an emitter center strike.

the ion strike, as shown in Fig. 9. The EB spacer and DT oxide volumes were not meshed. In order to maintain such a relatively small volume (to be computationally efficient), and avoid reflective boundary conditions at the edges (which is non-physical), a "wrapping layer" with an artificially low lifetime ($\tau_{WR} = 50$ ns), encased the entire substrate volume. A standard substrate lifetime of 9 μs was used throughout the bulk region. Secondary ion mass spectroscopy (SIMS) data was used to reproduce the doping profiles, which are represented as a series of rectangular well regions with a constant dopant density enclosed by Gaussian distributed tails along the edges. Physical 3-D device models included doping-dependent carrier lifetimes, SRH and Auger recombination, and mobility models which accounted for doping, electric field and carrier-carrier scattering dependences.

Ion strike simulations were performed using a two step approach. First, steady-state conditions were established by the specification of initial boundary and volume conditions, and solution physics specific to the problem. Next, a transient ion strike simulation was performed using the steady-state solution as an initial condition. Normally incident ions were simulated at an LET of 0.07 pC/μm, a range of 13.72 μm (to account for 8 μm of dielectric), and Gaussian-distributed charge track peaking at 2 ps and with a *1/e* characteristic time scale of 0.25 ps and radius

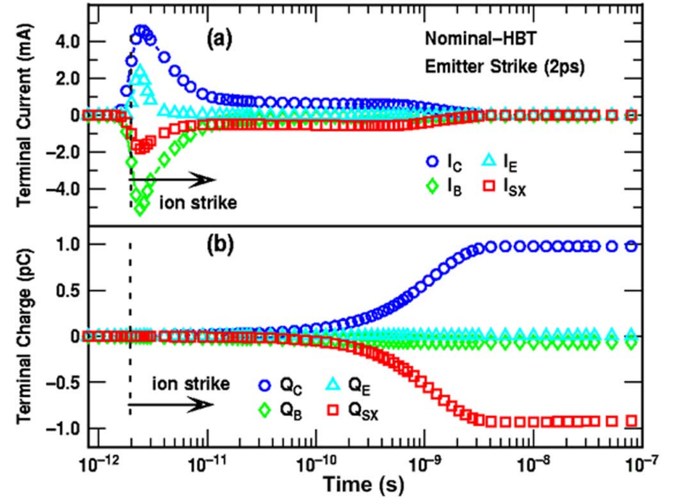

Fig. 10. Transient simulation results for an emitter centered ion strike to the nominal-HBT: (a) currents (I_C, I_B, I_E, I_{SX}), (b) charge (Q_C, Q_B, Q_E, Q_{SX}).

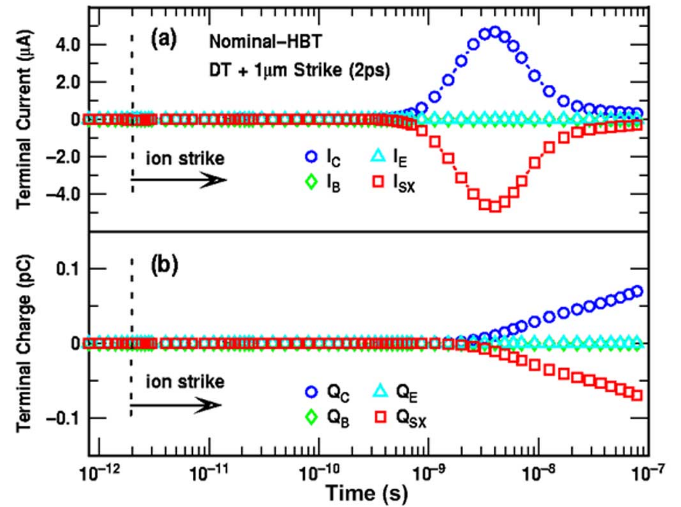

Fig. 11. Transient simulation results for an external DT ion strike to the nominal-HBT: (a) currents (I_C, I_B, I_E, I_{SX}), (b) charge (Q_C, Q_B, Q_E, Q_{SX}).

of 0.1 μm. To account for the potential impact of TID on charge collection, interface traps ($D_{IT} = 5 \times 10^{11}$ cm^{-2}) were placed along all SiO_2 interfaces. Trap densities that were typical for studying TID effects in BJTs [23] were selected to match experimental charge collection data. Ion strikes on the external R-HBT and 3 μm R-HBT devices utilized similar model parameters as the nominal-HBT, with the exception that the lateral size of the 3-D model was extended to 40 × 40 μm^2. NanoTCAD was used to solve the fundamental carrier continuity and Poisson equations using the finite volume numerical method and post-processing performed using CFD-View. A typical ion strike simulation (to 10 + μs) takes 3 hours on a 2.4 GHz Pentium PC.

Transient terminal current charge collection profiles from a normal-incident ion strike at 2 ps through the emitter center, and through the external DT, are shown in Figs. 10 and 11, respectively. The current waveforms are composed of a 5–10 ps long prompt component soon after the strike (drift dominated), followed by a time-delayed component (diffusion dominated)

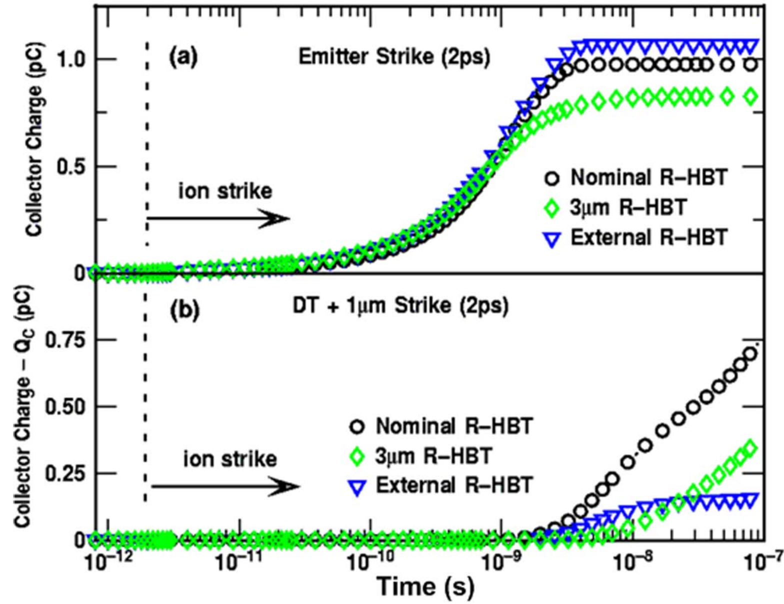

Fig. 12. Transient simulation results for nominal-, 3 μm R-, and external R-HBT showing Q_C (a) emitter centered (b) external DT strikes.

lasting up to 2 ns after the strike, as shown in Fig. 10(b). Prompt collection is observed on all terminals; however, delayed collection is only observed on the collector (electrons) and substrate (holes) terminals, which account for the majority of the collected charge, as shown in Fig. 10(b). These results are in reasonably good agreement with 3-D DESSIS ion strike simulations on 8 HP SiGe HBTs presented in [7] and [24]. In Fig. 11(a) an external DT strike result is shown to produce a delayed collection component observed only on the collector and substrate terminals. The peak of this delayed current component is observed 3–4 ns after the strike and is three orders of magnitude less than the prompt current component resulting in 0.07 pC collected after 100 ns (as opposed to 1 pC for the prompt current component), as shown in Fig. 11(b).

Transient Q_C for the nominal-HBT are compared with those of the 3 μm and external R-HBT devices, for an emitter center and external DT ion strike, as shown in Fig. 12(a) and (b). The inclusion of the substrate to n-ring junction results in the creation of a parasitic n(*collector*)-p(*substrate*)-n(*n-ring*) transistor. Under steady-state conditions ($V_{SX} = -4$ V, $V_{NR} = 0, 4$ V, $V_C = 0$ V), this device is in cut-off mode as both *pn* junctions are reverse-biased. In the aftermath of an ion strike, however, potential contours in the local vicinity of the strike are such that this parasitic BJT can be turned on (up to 0.5 ns after the strike) enabling a direct conduction path from the n-ring to the collector ($I_{NR} < 0$). In the case of the external DT strikes, the parasitic current flow is now from the collector to the n-ring ($I_{NR} > 0$) and also lasts up to 0.5 ns. A comparison of the measured and simulated Q_C is shown in Fig. 13(a) and (b), respectively. Each simulated Q_C represents a transient current integral over 14 μs. There is reasonably good agreement for drift-dominated strikes in the interior, while for strikes outside the DT there is some deviation between the simulated and measured results. Additional factors to consider include charge funneling

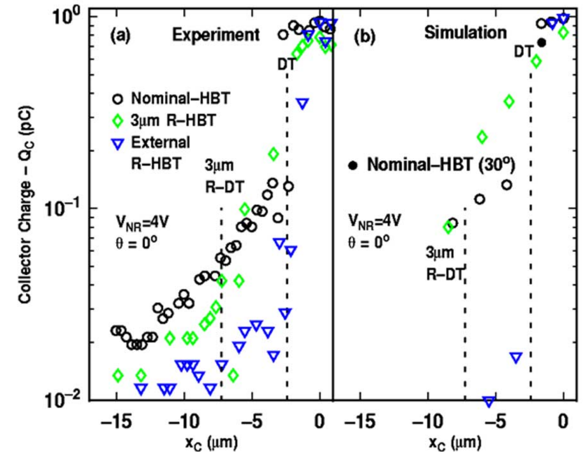

Fig. 13. Comparison of (a) experimental and (b) simulation results of Q_C as a function of x_C for the nominal-, 3 μm R-, and external R-HBT.

collection and the impact of secondary particles generated from nuclear interactions within overlaying metallization.

V. Discussion

An experimental evaluation of several layout-based RHBD techniques for SEU mitigation in SiGe HBTs has been presented and confirmed using 3-D transient ion strike simulations. In the best case scenario, reductions of 53% in $Q_{C,\mathrm{INT}}$ and 21% in peak Q_C have been demonstrated on two different R-HBT structures. These values compare well with the reductions achieved via employing varying epitaxial thicknesses [25], but are substantially lower than the reductions achieved via putting the SiGe HBTs on SOI [26], and ultimately still result in Q_C values much larger than the typical critical charge ($Q_{\mathrm{crit}} = 100$ fC) determined for SEU in high-speed SiGe BiCMOS circuits [9]. However, a strictly layout-based variation technique applied to

a bulk SiGe technology has the desirable advantage of being lower in cost compared to process changes (e.g., moving to SOI) for SEU robustness. Additionally, device layout approaches do not incur the increases in circuit area and power consumption common to many circuit hardening techniques. Similar layout-based approaches have been successful in SEU mitigation for CMOS, as demonstrated in [27] and such work for the SiGe HBT clearly warrants further investigation. Although the reductions in Q_C for emitter-center strike will not prevent an upset, the level of suppression of collection from external DT events is quite substantial. Assuming carrier diffusion lengths on the order of 100 μm or more (outside the DT), there is a considerable amount of charge that could potentially be diverted away from the transistor in a broad-beam environment, when there are a substantial number of strikes outside the DT.

Increasing the A_{NR}/A_{DT} ratio is critical in lowering Q_C, and to this end additional structures that increase n-ring width (thereby increasing A_{NR} within the same A_{DT}), while reducing xn_1 would be beneficial. We have demonstrated that in SiGe 8HP, an xn_1 of 2 μm results in an n-ring to collector short, quantifying the limitation of the technique as it applies to internal ring structures. This limitation may be overcome by reductions in the back end of the line (BEOL) thermal cycles and a reduction in the sub-collector doping levels. Another approach may be the combination of process driven hardening techniques (such as the epitaxial Si thickness [25] or SOI [26]), with the layout driven use of the n-ring. Alternatively a buried n-ring, analogous to the triple wells used in CMOS may be considered.

Ultimately, the success of any SiGe RHBD SEE mitigation technique will be determined by the cross-section (σ) versus LET response obtained via broad-beam heavy-ion analysis of actual circuits. The IBICC technique employed in this work gives a good indication, however, of the extent to which layout-based charge collection mitigation is effective, at least for shallow ion strikes. We believe that the ultimate SEU hardening success in SiGe will be achieved via a combination of layout-level RHBD and latch-level RHBD techniques implemented without excessive spatial or temporal redundancy techniques such as TMR. The external n-ring can extended to encompass several minimum spaced devices in a flip-flop or differential pair thereby minimizing the overall area penalty on the circuit level. Compared to TMR, this should yield a 60% reduction in circuit area. The circuit level power penalty will be minimal as the n-ring draws extremely low current (pA) when biased. The technique can also be adapted to mixed signal and analog applications by hardening, the input HBT pair in an operational amplifier for example. Pulsed laser analysis time resoled IBICC techniques could then be used to correlate RHBD charge collection mitigation on the single event transient characteristics.

VI. Summary

Transistor-based layout techniques for mitigating heavy ion triggered charge collection in SiGe HBTs, through the addition of internal and external n-rings, has been presented and validated using ion beam induced charge collection techniques together with 3-D transient ion strike simulations. Up to 90% reduction in collected charge for events outside the DT, and 21% reduction in collected charge for events inside the DT have been demonstrated.

Acknowledgment

The authors would like to thank L. Cohn, K. LaBel, P. Dodd, J. Nance, J.P. Comeau, and the IBM SiGe team for their contributions to this work.

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Task #3: Radiation Effects in SiGe HBTs – related articles.

3-D Simulation of SEU Hardening of SiGe HBTs Using Shared Dummy Collector

Muthubalan Varadharajaperumal, Guofu Niu, Xiaoyun Wei, Tong Zhang, John D. Cressler, Robert A. Reed, and Paul W. Marshall

***Abstract*—This paper presents a SEU hardening approach that uses a dummy collector to reduce charge collection in the main transistor. The dummy collector is obtained using the silicon space between adjacent HBTs. It is obtained without any process modification or area penalty. The simulations are performed for normal and angled strikes. The hardened device shows significant reduction in charge collection due to sharing of diffusive charge collection by the dummy collector. Multiple HBT arrays of regular and hardened HBT are simulated to study the simultaneous charge collection in multiple HBTs. With hardening, charge collection in multiple devices is suppressed considerably for normal and angled strikes as the shared dummy collector collects a large amount of charge.**

***Index Terms*—Critical charge, deep trench isolation (DTI), dummy collector, radiation hardening by design (RHBD), SiGe HBT, single event upset (SEU), SRH recombination.**

I. INTRODUCTION

SiGe HBT technology is a potential candidate for space applications because of its inherent robustness to total ionizing dose (TID) radiation [1]. Single Event Upset (SEU), however, is a concern, primarily due to charge collection through the collector-substrate (CS) junction [2], [3] and the relatively low substrate doping compared to digital CMOS processes. Various hardening techniques, like introduction of a back junction [4] or a heavily doped p-type buried layer [5] have been proposed to reduce charge collection. These techniques, however, require process changes. In this work, we propose a new SEU hardening approach that reduces charge collection through the use of a dummy collector/substrate (CS) junction and present 3-D simulation results. Like the RHBD techniques proposed earlier in [6], the hardening approach requires only layout changes. However, the new approach does not suffer area penalty when applied to integrated circuits, as the dummy CS junction can be obtained utilizing the silicon between adjacent devices. We will first examine charge collection in stand-alone HBTs, for both normal and angled deep strikes, and then examine simultaneous charge collection in multiple HBTs as found in circuits.

Manuscript received July 24, 2007; revised October 6, 2007. This work was supported by the Defense Threat Reduction Agency (DTRA) under the Radiation Hardened Microelectronics Program, NASA Goddard Space Flight Center (GSFC) under the NASA Electronic Parts and Packaging (NEPP) Program, the NASA Exploration Technology Development Program (ETDP), and the Alabama Microelectronics Science and Technology Center.

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Digital Object Identifier 10.1109/TNS.2007.910290

II. DEVICE STRUCTURE AND LAYOUT

Fig. 1(a) shows the cross section of a typical regular SiGe HBT showing the deep-trench isolation and the CS junction. Fig. 1(b) shows a schematic of the layout. The deep-trench (DT) encircles the active device, and the NS layer defines the N^+ sub-collector. The silicon area inside DT thus determines the CS junction area. During an ion strike, the CS junction either directly collects deposited charges through drift within the potential funnel or indirectly collects charges after they arrive at the junction after diffusion.

Given that carrier diffusion lengths are on the orders of tens of microns or more in the lightly doped substrate of a typical SiGe HBT, a dummy CS junction placed outside the DT along the device perimeter should be able to at least reduce the amount of diffusive charge collection by the HBT collector, for charge deposited both inside and outside the DT isolation. A cross section and schematic layout are shown in Fig. 2(a) and (b). This dummy junction can be obtained by pulling out the NS layer in the regular HBT so that the NS encloses the outer DT edge by an amount W_d. As we will show below, a 1 $\mu\mathrm{m}$ wide dummy NS junction provides sufficient hardening. The dummy NS outside the DT is contacted through the same N+ sinker used for contacting the transistor NS. Fabrication of the hardened HBT is thus done with only a few layout changes. For a stand-alone device, one may be concerned about the extra silicon area. In integrated circuits, however, the proposed hardening approach does not really suffer area penalty. Devices are placed apart by several microns due to design rules, density requirement and other practical reasons. The unused silicon between neighboring devices can be utilized to create the dummy collector needed for SEU hardening.

Hardened devices have been fabricated in IBM 5AM technology and tested. Measured device characteristics are the same for regular and hardened HBT, showing no degradation in electrical characteristics, as the dummy CS junction is isolated from the main transistor. The measured breakdown voltage of the dummy CS junction is 21 V, which is more than sufficient for the technology.

Next we present 3-D simulation of the proposed SEU hardening approach, first using stand-alone single device, and then using arrays of HBTs to mimic the more realistic situations in an integrated circuit with HBTs placed together. Both normal strikes and angle strikes are simulated, with representative striking locations.

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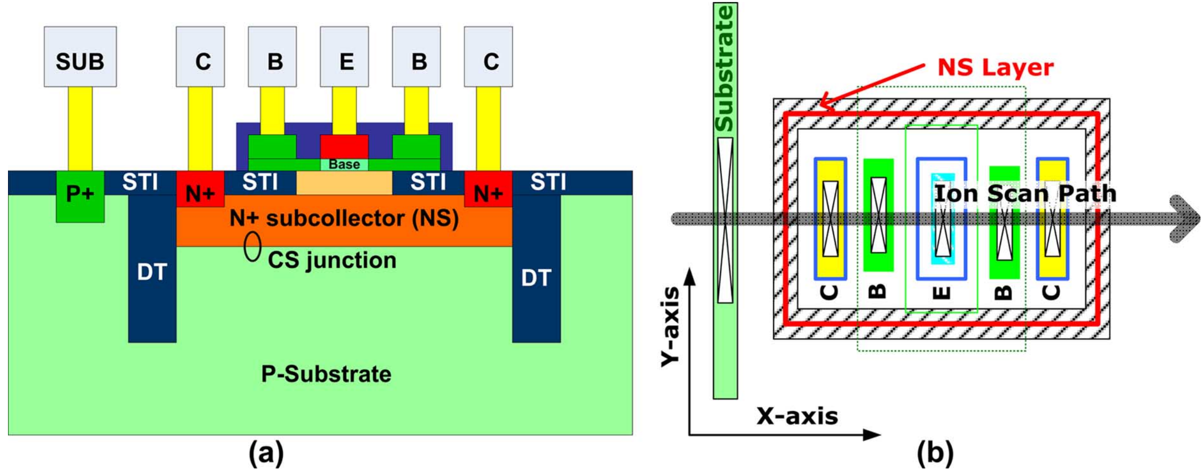

Fig. 1. (a) Schematic cross-section and (b) schematic of the layout of a SiGe HBT (not to scale). The ion travels in the XZ plane with a fixed y along the negative x direction. The simulated ion strikes will be located along the axis "ion scan path.".

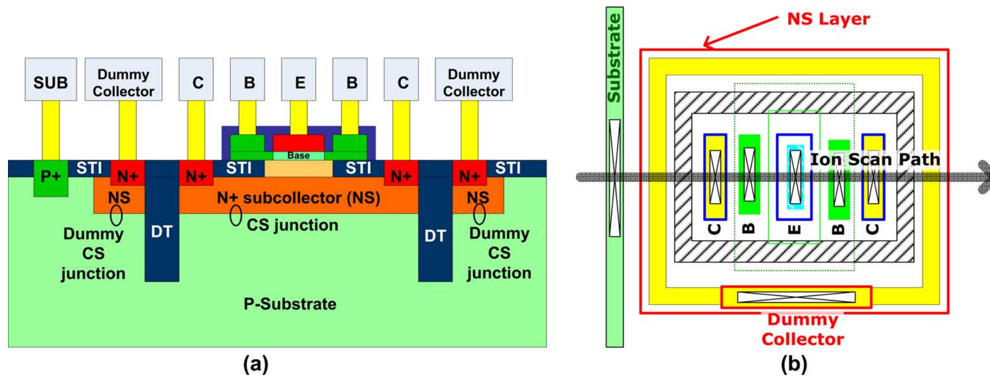

Fig. 2. (a) Schematic cross-section and (b) schematic of the layout of a hardened SiGe HBT (not to scale).

III. Stand-Alone Single Device

We first consider stand-alone single device, like those used in typical device characterization and microbeam testing. Devices are separated by 100 μm or more, and transistor active area is very small compared to the area needed for pads and interconnects leading to device terminals. Here we simulate a total silicon area of 35×35 μm^2, to mimic a stand-alone device.

The transistor is centered in the total silicon area. The 3D structure is 35 μm deep. The simulations were performed for various depths of the substrate for the same conditions. The charge collection was compared for the various depths and the minimum depth from which the charge collection remains constant was chosen as the depth of the substrate. This was done to ensure that the simulation results are not artificially dependent on the thickness of the substrate used in simulation, which is always much smaller than the actual substrate thickness to keep the number of grid points low.

Due to thick overlayers in modern silicon technologies, current heavy ions available for microbeam testing [5], [7], [8] cannot provide deep strike, particularly for angled incidence, therefore at present 3-D simulation is the only viable way of examining charge collection for deep strikes and large angled strikes. Here we use Sentaurus Device for 3-D simulation [9]. Charge track generation and physical models used are the same as in [3]. Deep strikes with an LET of 0.1 pC/μm (9.7 MeV-cm^2/mg) are simulated. The ion crosses the whole device. As the device size in the simulation is large, the amount of charge deposited in the simulated structure varies as the angle varies. However the amount of charge itself is not a meaningful parameter, as charge collection is not limited by the amount of charge deposited for these deep strikes.

We note that default SRH recombination model parameters are used, as opposed to those used in [5] for fitting microbeam data. The default parameters give longer lifetime, 9 μs for a substrate doping of 1×10^{15} cm^{-3}, and represent the worst case. Collector, emitter and base are grounded. $V_{substrate} = -4$ V. No difference is found for variation of V_{dummy} from 0 to 4 V. $V_{dummy} = 3$ V is used below.

As 3-D simulation is time consuming, we simulate only strikes along the x-axis, for a fixed y that is at the center of the device, as shown in Fig. 1(b). At each incident position, simulations are done for incident angles of $\theta = 0°$, 30°, 45° and 60°. The ion travels in the XZ plane with a fixed y along the negative x direction.

A. Regular HBTs

Fig. 3 shows collector charge versus ion incident position for various incident angles in the regular HBT. The worst charge collection occurs for normal strike, as expected. As the incident angle increases the area of large charge collection is reduced and

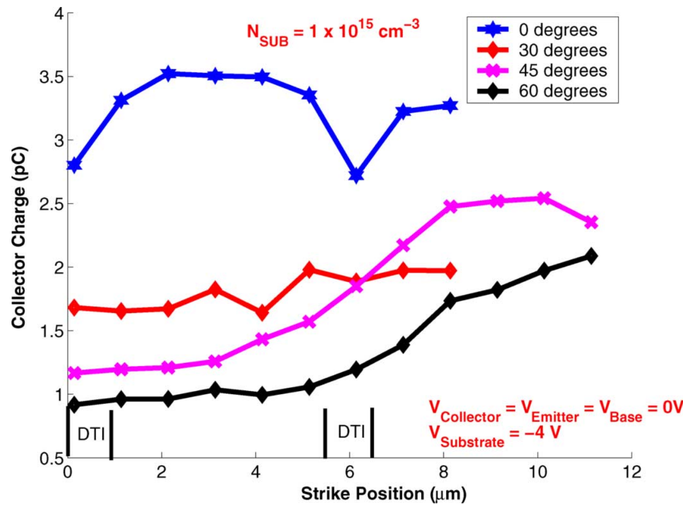

Fig. 3. Collector charge versus strike location for incident angles $\theta = 0°, 30°$, $45°$ and $60°$ in a regular HBT.

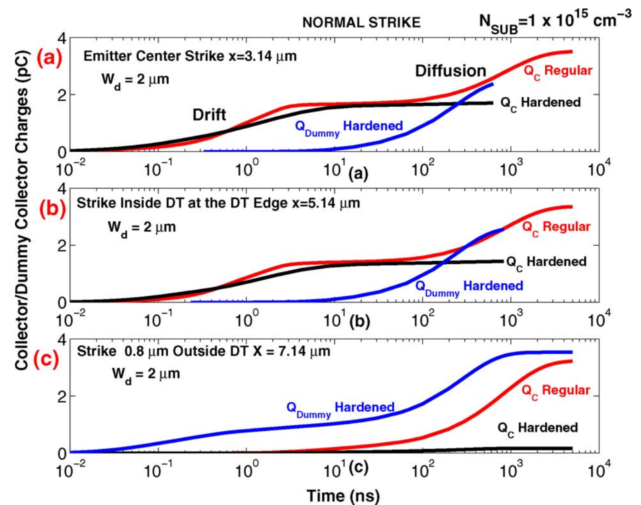

Fig. 5. Charge collection characteristics comparison for ion strike at (a) emitter center, (b) DT edge and (c) outside DT between the regular and hardened HBT.

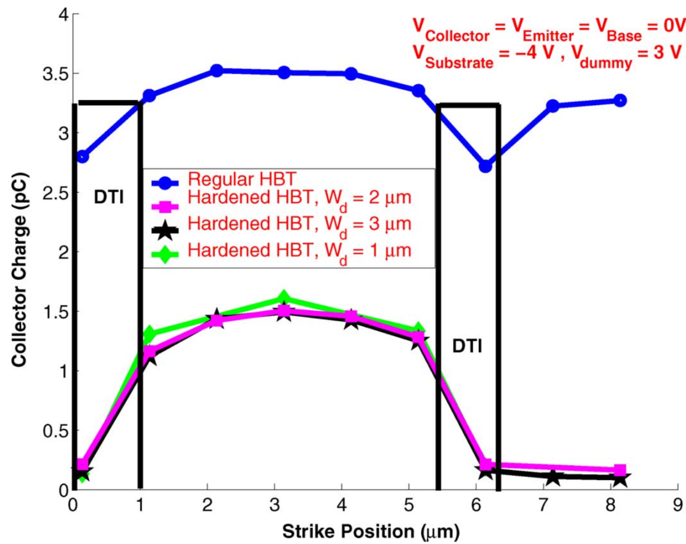

Fig. 4. Normal strike collector charge comparison between the regular HBT, and hardened HBT with $W_d = 1,\ 2$ and $3\ \mu\mathrm{m}$.

area of lower charge collection increases [8]. The collector collects a large amount of charge for even strikes occurring outside DT because of the long lifetimes and large diffusion lengths.

B. Hardened HBTs

1) Normal Strike: Fig. 4 shows the normal strike charge collection comparison between the regular and hardened HBTs. Simulations were performed for different dummy collector widths (W_d) [see Fig. 2(a)]. Charge collection is approximately the same for $W_d = 1 - 3\ \mu\mathrm{m}$, indicating that the typical 5 $\mu\mathrm{m}$ spacing between adjacent HBTs found in circuit design is more than sufficient for placing the dummy collector. This is good news, as no area penalty is involved. A width of 2 μm is used below. We note that the actual dummy CS junction area is larger than what W_d indicates, because of the existence of lateral junction between the N+ sub-collector and the surrounding p-substrate.

We emphasize that the dummy collector should be placed around the DT isolation of the device to achieve the most effective hardening. The N^+ is highly conductive and in general the metal contact to the dummy collector can be placed anywhere on top of the N^+ dummy collector.

The hardened device reduces collector charge collection significantly, not only for strikes outside DT, but also for strikes inside DT. To further understand these results, we plot charge collection vs time at representative locations in Fig. 5.

For emitter center strike, the charge collection curve for the regular HBT shows two distinct regions: drift and diffusion [Fig. 5(a)]. The charge collected by each terminal is obtained by the integration of current in the terminal. The final collector charge at 1000 ns is 3.5 pC and 1.71 pC for the regular and hardened HBTs. The diffusive charge collections by the dummy collector and the collector of the regular HBT have not completely saturated, and a slightly higher charge is expected if simulations were done for a longer time. This, however, does not affect our conclusion, as charge collection by the hardened HBT collector has completely saturated. A longer simulation would lead to slightly higher charge collection by the regular HBT collector, but the same charge collection by the hardened HBT collector. The final dummy collector charge is 2.1 pC. The total charge collected with hardening ($\mathrm{Q}_{dummy} + \mathrm{Q}_C$ hardened) is higher than the Q_C in the regular HBT. The drift portion of the curves are approximately the same in the regular and hardened HBTs. The charges left in the substrate after drift collection start to diffuse outward towards the extrinsic portion of the device. In the hardened HBT, the diffusive charge collection is dominated by the dummy CS junction, as evidenced by the saturation of Q_C hardened and the increase of Q_{dummy} in Fig. 5(a). This leads to less charge collection by the CS junction of the active device. Fig. 5(b) shows charge collection vs time curves for a strike at the NS edge, which are similar to those for the center strike. Again, the dummy CS junction dominates diffusion charge collection.

For strikes outside DT, charge collection in the regular HBT is only through diffusion of charges generated outside DT towards

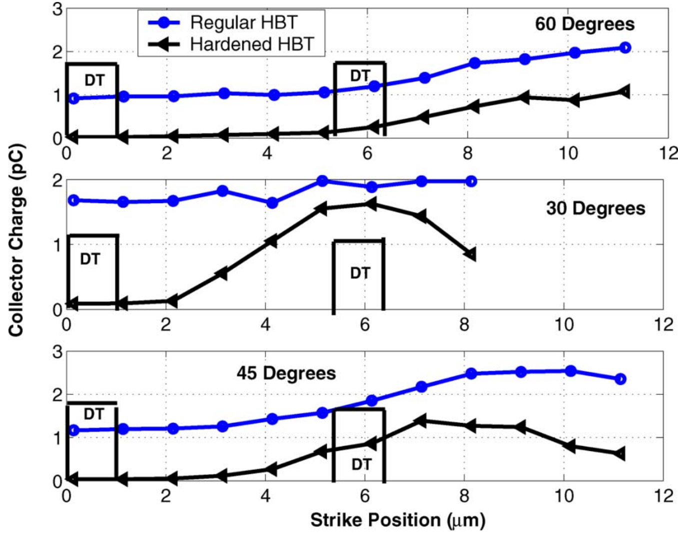

Fig. 6. Positional charge collection comparison between the regular and hardened HBT for angled strikes $\theta = 30°$, 45° and 60°.

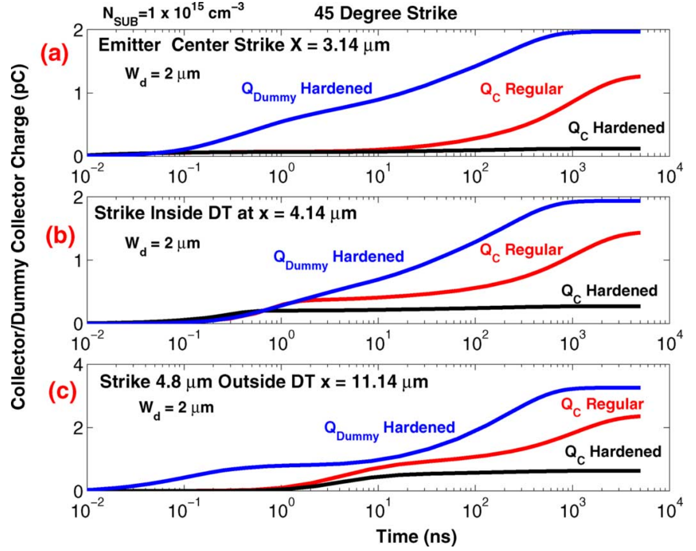

Fig. 7. Charge collection characteristics comparison for ion strike at (a) emitter center, (b) DT edge and (c) outside DT between the regular and hardened HBTs for $\theta = 45°$.

the CS junction inside the DT. Fig. 5(c) shows such a strike that is on the dummy collector. As expected, the dummy collector charge collection has a large drift component. The dummy collector collects 3.5 pC charge, and reduces collector charge from 3.2 pC in the regular HBT down to 0.17 pC in the hardened HBT. For strikes occurring W_d μm away from the outer DT edge, the lateral junction of the dummy CS junction will come into play.

To summarize, for all normal strikes, with hardening, the drift component of charge collection remains approximately the same, while the diffusion charge collection component is nearly completely suppressed.

2) Angled Strike: As large angles are of practical concern [10], [11] , we now examine the mechanisms of angled incidence charge collection.

Fig. 6 shows the angle strike comparison for $\theta = 30°$, 45° and 60°. The hardened HBT collects less charge than the regular HBT for all angles and all strike positions. The area of higher charge collection is reduced by a considerable amount in the hardened HBT. The improvement from hardening is overall more significant compared to normal incidence, and can be understood as follows. For normal incidence, the ion passes through either the transistor CS junction or the dummy CS junction. For large angle incidence, the ion either passes through one junction, or misses both CS junctions. Consequently, charge collection by the transistor CS junction is mainly through diffusion in most cases, and the dummy CS junction becomes more effective. This explanation is supported by simulated details of electron density n, hole density p, and potential ψ.

The charge collection vs time plots at representative strike points are shown in Fig. 7 for $\theta = 45°$. For the 3 locations, only the $x = 4.14$ μm [Fig. 7(b)] case shows a small amount of drift charge collection by the transistor collector, which is complete in 2 ns. For the outside DT strike at $x = 11.14$ μm, the ion passes through the dummy CS junction, causing a drift component in the dummy collector charge. Collector charge collec-

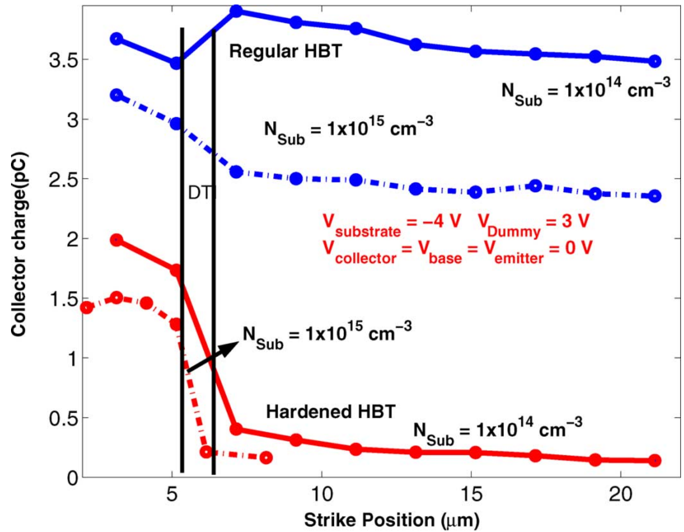

Fig. 8. Substrate doping comparison between 1×10^{15} cm^{-3} and 1×10^{14} cm^{-3}. Normal strike.

tion remains mainly by diffusion, and a significant reduction is achieved with hardening.

3) High Resistivity Substrate: Substrate doping influences the charge collection for strikes outside DT by modifying the lifetime of the diffusing charges [12], [13] . Fig. 8 shows charge collection comparison for substrates with $N_{Sub} = 1 \times 10^{14}$ cm^{-3} and $N_{Sub} = 1 \times 10^{15}$ cm^{-3} for regular and hardened HBTs. Charge collection for $N_{Sub} = 1 \times 10^{14}$ cm^{-3} is higher than for $N_{Sub} = 1 \times 10^{15}$ cm^{-3} doping mainly because of the slightly increased lifetime from 9 μs to 10 μs.

IV. Simultaneous Charge Collection Issues in Multiple Devices

Previous simulations are done for a stand-alone single HBT with a large simulation area of 35×35 $\mu\mathrm{m}^2$. This large area is necessary due to the large lifetime and large diffusion length in-

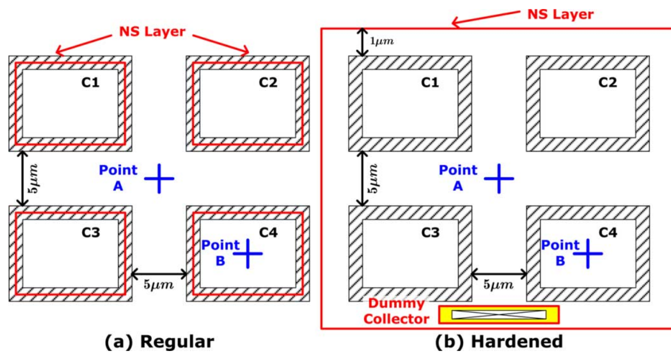

Fig. 9. (a) 2×2 regular HBT array and (b) 2×2 hardened HBT array.

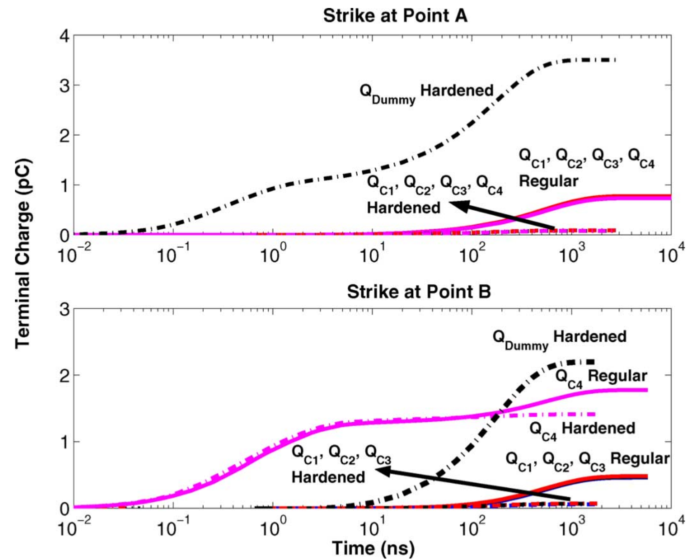

Fig. 10. Charge collection comparison between 2×2 regular and hardened HBT arrays for ion strikes at point A and B.

volved. In circuits, however, the spacing between transistors is only several microns, which is comparable to or even less than the diffusion lengths. A single ion strike can then cause simultaneous charge collection in multiple devices near the strike location [13]. Thus we need to examine charge collection using realistic layout including multiple devices. From a hardening standpoint, we do not need to pull out the individual NS layer for individual devices. Instead, a effective way is to replace the NS of several devices by a single NS enclosing several devices, as shown below. As the ion path of angled strikes intersects with more neighbouring devices in an array of HBTs, we expect the shared dummy collector to work effectively for angled strikes and reduce charge collection in all devices. Simulation results on 2×2, 3×3 and 4×4 HBT arrays are presented below.

A. 2×2 HBT Array

Fig. 9 illustrates the layout of a 2×2 array for regular and hardened HBTs simulated. C1, C2, C3 and C4 are the collectors of individual devices. A 5 μm spacing, typical of circuit layouts using SiGe HBT technology, is used. Normal ion strike simulations are performed at points A and B. Point A is at equal distance from all devices, and represents the outside DT strike location for maximum charge collection sharing. Point B is the center of C4, and represents inside DT strikes.

Fig. 10 gives the charge collection comparison between the regular and hardened HBT arrays for strikes at point A and B. For a strike at point A, C1, C2, C3 and C4 of the regular HBTs collect 0.7759, 0.7758, 0.735 and 0.743 pC charges, respectively. These charges are large enough to cause simultaneous upsets in all four transistors if the critical charge is less than 0.73 pC for all of the transistors in question. The value of critical charge depends on the details of specific circuits, and a few tenths of pC is significant to cause upsets in SiGe HBT logic circuits [14].

In the 2×2 hardened HBT array, the dummy collector collects 3.5 pC charge through drift and diffusion, thereby reducing the C1, C2, C3 and C4 charge collection to 0.0866, 0.0863, 0.0786 and 0.079 pC, respectively, and reducing event and/or error rate. Depending on propagation of transistor upset towards circuit output, the overall circuit upset rate should be much reduced with hardening, as all four transistors are now collecting negligible amount of charge. In addition to reduced total amount of charge collection, the duration of transients is significantly reduced, as shown earlier in the charge collection plots, because the slow diffusion charge collection by the HBT collector is suppressed. In particular, for analog and RF circuits, such as amplifiers and oscillators, we expect significant reduction of single-event transients in circuit output due to much shorter collector current transients. SEU testing of circuits with deep strikes will be needed to experimentally quantify the effectiveness of the proposed hardening approach.

For a strike at point B, the struck device C4 collects 1.7761 pC charge while C1, C2, C3 collect 0.46, 0.47 and 0.48 pC charges respectively in the regular HBT array. Even though the strike is in C4, other devices collect considerable charge through diffusion for the regular HBTs due to the long lifetimes. For a critical charge less than 0.45 pC, all of the four devices would be upset. Although the hardening approach does not significantly reduce charge collection in the struck device, it reduces the charge collection in the neighbouring devices C1, C2 and C3 down to 0.07, 0.069 and 0.058 pC, respectively, which is significant.

B. 3×3 HBT Array

We now examine a 3×3 array, with multiple incident angles. As illustrated in Fig. 11, as the angle of incidence increases, the ion path gets closer to the CS junction of adjacent devices in a regular HBT array, thereby causing more charge collection by adjacent devices. In the hardened HBT array, the ion path inevitably passes through or nearby the dummy CS junction that surrounds all of the HBTs. We therefore expect a significant reduction of charge collection overall in an array of HBTs for angle strikes as well.

Figs. 12 and 13 illustrate the layout of the 3×3 regular and hardened HBT arrays. Each HBT is identified with their row and column index (i, j), $i = 1 : 3$, and $j = 1 : 3$. For instance, A11 refers to the HBT at row 1 and column 1. Normal, 30°, and 45° ion strike simulations are performed at three representative points 1, 2 and 3. Point 1 is at the center of A32. Point 3 is at the center of A22, also the center of the HBT array. Point 2 is located outside the DT between A32 and A22.

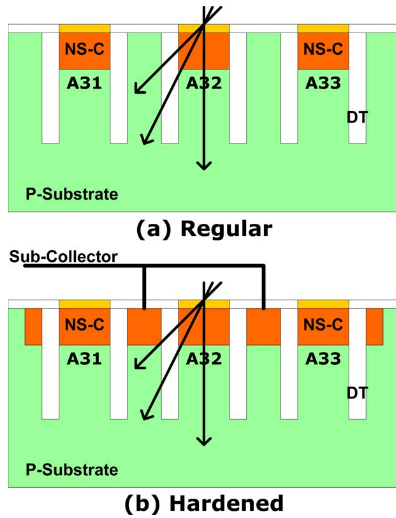

Fig. 11. A cartoon illustration of the cross-section of the regular and hardened HBT array showing the devices A31, A32 and A33 (not to scale). The ion path represents the normal and angled strikes.

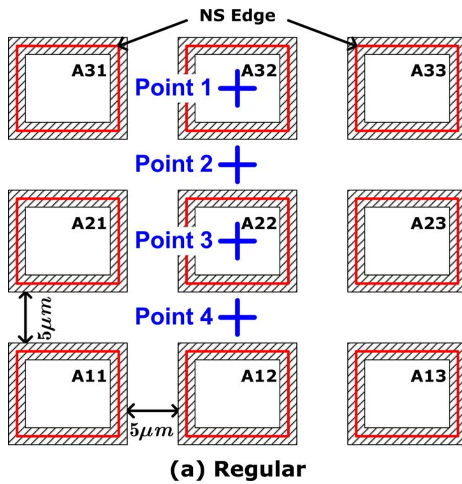

Fig. 12. 3×3 regular HBT array.

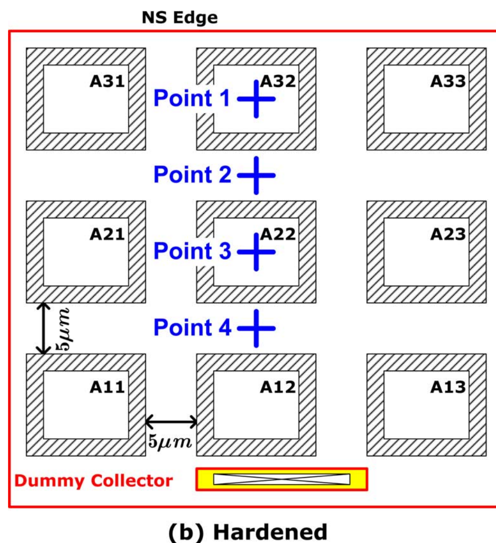

Fig. 13. 3×3 hardened HBT array.

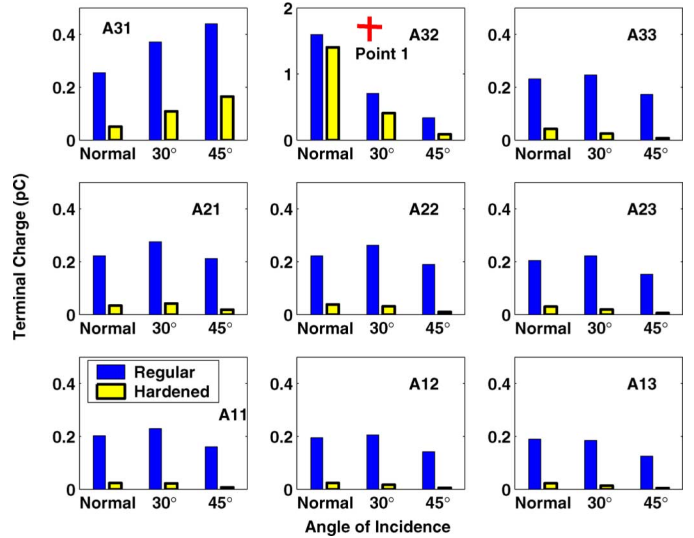

Fig. 14. Total charge comparison between 3×3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 1. The red cross indicates that the device A32 is hit by the ion.

Fig. 14 shows the total charge collected by all the devices of the regular and hardened HBT array for a strike at Point 1, that is, inside the DT of A32, indicated by a red cross. A32, the struck device in the 3×3 regular HBT array collects 1.59 pC, which is less than the 1.78 pC in the 2×2 regular HBT array and 3.5 pC in the stand-alone regular HBT. This clearly shows that without hardening the charge collected by the struck device decreases with increasing HBT array size, primarily because of charge sharing by adjacent HBTs. The total charge collected by all HBTs, on the other hand, *increases* with increasing HBT array size, as expected.

As in the 2×2 array, for normal and 30 degrees angle strikes, charge collection in the struck device is only slightly reduced by hardening. However, for every other device in the 3×3 array, a considerable reduction of charge collection has been achieved with hardening, as was in the 2×2 case, thanks to the presence of the dummy collector surrounding all of the HBTs. For 45 degree angle strike, a sizable reduction of charge collection in the struck device A32 is also observed and can be understood from examining how the ion path intersects different devices. Fig. 15 shows the total terminal charge comparison for a strike at point 3. The charge collection characteristic is similar to the charge collection at point 1.

Fig. 16 shows the 3×3 simulation results for a strike at Point 2, outside the DT, and in between devices A32 and A22. As charge collection is through diffusion in all of the devices in the regular HBT array, the dummy collector in the hardened HBT array yields a significant reduction in charge collection characteristic in all of the HBTs. We can therefore conclude that the shared dummy collector hardening approach works effectively for both inside and outside DT strikes, for both struck devices and neighboring devices,

C. 4×4 HBT Array

Fig. 17 shows the simulation results of a 4×4 HBT array, both regular and hardened. Only normal strikes are simulated.

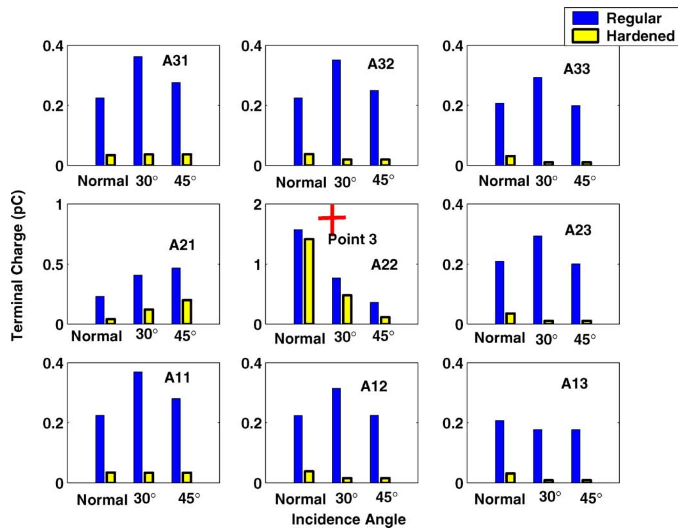

Fig. 15. Total charge comparison between 3×3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 3. The red cross indicates that the device A22 is hit by the ion.

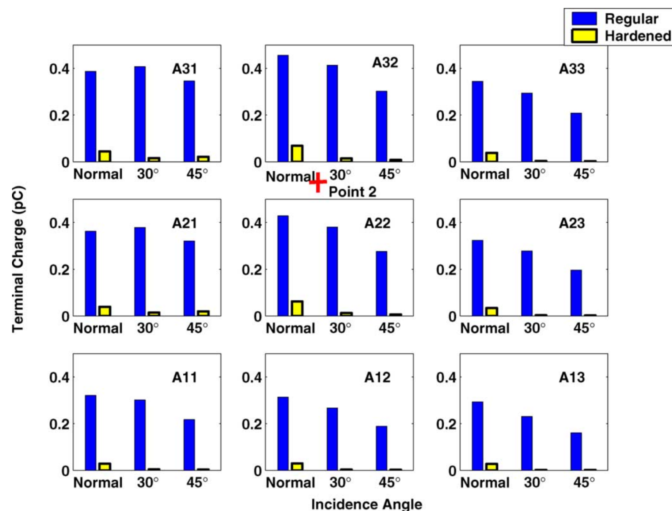

Fig. 16. Total charge comparison between 3×3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 2. The red cross indicates that the ion strike position is located between A32 and A22.

The 4 incident points are indicated by the "x"'s. P1 and P3 are inside DT. P2 and P4 are outside DT and in between devices. For the struck devices, A23 for P2 incidence, and A14 for P4 incidence, approximately 1.6 pC charge is collected without hardening. This number is about the same as the charge collected by struck devices in the 3×3 array, indicating that even though the amount of charge collected by a struck device decreases with increasing number of adjacent devices, due to charge collection sharing, the decrease becomes very gradual eventually.

Like in 2×2 and 3×3 arrays, even though hardening has only a small effect on the struck devices for inside DT incidence, it has a pronounced effect on other devices. For outside DT incidence (P1 and P3), hardening is effective in reducing charge collection by all devices.

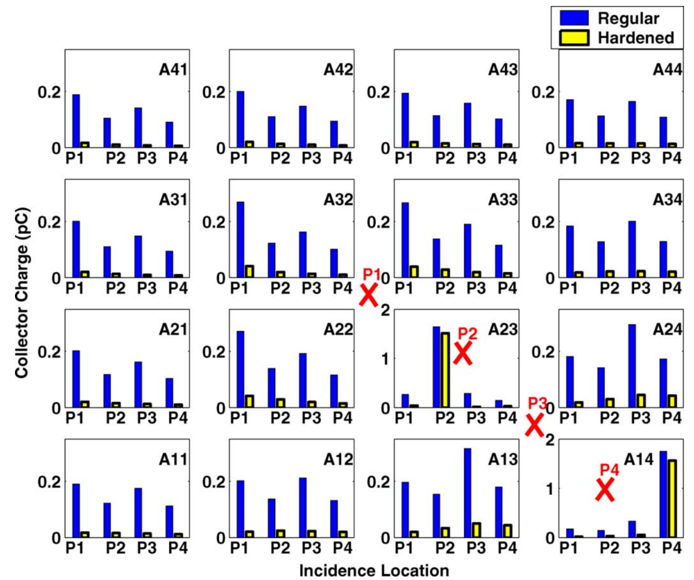

Fig. 17. Total charge comparison between 4×4 regular and hardened HBT arrays for 4 incident points.

V. Conclusions

We have proposed a SEU hardening approach that uses a dummy collector to reduce charge collection by the main transistor. The dummy collector can be obtained using existing silicon space between adjacent HBTs without process modification or area penalty, and can be shared by several adjacent devices. 3-D simulations of normal and angled incidence deep strikes are performed at representative strike locations to examine the effectiveness of the proposed approach. In all cases, the hardened devices show significant reduction of charge collection, primarily due to sharing of diffusive charge collection by the dummy collector. Impact of dummy collector width and substrate doping are examined as well. 2×2, 3×3 and 4×4 arrays of regular and hardened HBTs are simulated to examine simultaneous charge collection sharing between adjacent devices. With increasing HBT array size, the amount of charge collected by struck devices for inside DT incidence first decreases, and then stays at a significant value. Without hardening, significant charge collection sharing exists between adjacent devices, for both inside and outside DT strikes, leading to simultaneous upsets of multiple transistors. With hardening, significant simultaneous charge collection by multiple devices is suppressed considerably for normal and angled strikes, as the shared dummy collector collects a large amount of charges that would be shared by regular collectors.

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An Evaluation of Transistor-Layout RHBD Techniques for SEE Mitigation in SiGe HBTs

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***Abstract*—We investigate transistor-level layout-based techniques for SEE mitigation in advanced SiGe HBTs. The approach is based on the inclusion of an alternate reverse-biased *pn* junction (n-ring) designed to shunt electron charge away from the sub-collector to substrate junction. The inclusion of the n-ring affects neither the *dc* nor *ac* performance of the SiGe HBT and does not compromise its inherent multi-Mrad TID tolerance. The effects of ion strike location and angle of incidence, as well as n-ring placement, area, and bias on charge collection are investigated experimentally using a 36 MeV O_2 microbeam. The results indicate that charge shunting through the n-ring can result in up to a 90% reduction in collector collected charge for strikes outside the DT and a 18% reduction for strikes to the emitter center. 3-D transient strike simulations using NanoTCAD are used to verify the experimental observations, as well as shed insight into the underlying physical mechanisms. Circuit implications for this RHBD technique are discussed and recommendations made.**

***Index Terms*—Charge collection, deep trench (DT), ion beam induced charge collection (IBICC), NanoTCAD, radiation hardening by design (RHBD), silicon-germanium (SiGe), SiGe HBT, single event effects (SEE).**

I. Introduction

SiGe BiCMOS is rapidly evolving as a key technology enabler for extreme environment electronics, as a result of its built-in multi-Mrad (SiO_2) total ionizing dose (TID) tolerance, enhanced performance at cryogenic temperatures, high-level integration capability, and low cost [1]. Single event effects (SEE) mitigation continues to be a major research area in SiGe, with recent results demonstrating limiting cross-sections (SEU-free operation) at linear energy transfer (LET) values well above 50 MeV-cm^2/mg for 16-bit shift registers [2]. This milestone was achieved by first dual-interleaving the pass and storage cells of the latch, followed by the subsequent encapsulation of the register in triple modular redundancy (TMR) architecture with voting at end (VAE) decision blocks with the associated area and/or power consumption penalties [3]. In the present work, a radiation hardening by design (RHBD) technique implemented solely using transistor layout variations to the standard SiGe HBT is proposed. This transistor-level RHBD approach targets bulk SiGe HBTs without any intentional process-induced hardening.

Drift transport of excess carriers (generated in the aftermath of a heavy ion strike) via the strong electric field of a reverse biased *pn* junction has long been accepted as the primary mechanism for charge collection in semiconductor devices [4], [5]. In the SiGe HBT, the junction of interest is the substrate (p) to sub-collector (n) junction, which is universally reverse-biased in normal circuit operation. 3-D TCAD simulations of charge collection in SiGe HBTs have identified the collector and emitter terminals as the sink for electrons, and the base and substrate as the sink for holes, in the case of an *npn* SiGe HBT. The relative contributions from each terminal depend strongly on the loading characteristics (terminal impedances), bias, substrate doping, and ion strike depth [6], [7]. Perturbations in the collector node voltage resulting from electrons collected at the collector of the device and coupled into the loaded circuit have also been identified as the primary mechanism underlying the observed broad-beam heavy ion circuit sensitivity [8] first reported in [9].

The RHBD approach presented here features an alternative/additional route to SEE hardening in SiGe HBTs, by implementing a low impedance path within the transistor designed to shunt charge away from the collector terminal. This path is realized by including an additional reverse biased *pn* junction formed between the p-substrate and n^+ guard ring (n-ring) resulting in a secondary electric field. Special considerations in the implementation of this approach include: the location and area (A_{NR}) of the n-ring; n-ring bias (V_{NR}); enclosed trench area (A_{DT}); strike location, and incident angle (θ).

Manuscript received July 20, 2007; revised September 5, 2007. This work was supported in part by the Defense Threat Reduction Agency (DTRA) under the Radiation Hardened Microelectronics Program, in part by the NASA Goddard Space Flight Center (GSFC) under the NASA Electronic Parts and Packaging (NEPP) Program, in part by the NASA Exploration Technology Development Program (ETDP), in part by the AFOSR Multidisciplinary University Research Initiative (MURI) program, in part by Sandia National Laboratory, and in part by the Georgia Electronic Design Center (GEDC) at the Georgia Institute of Technology.

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Digital Object Identifier 10.1109/TNS.2007.908697

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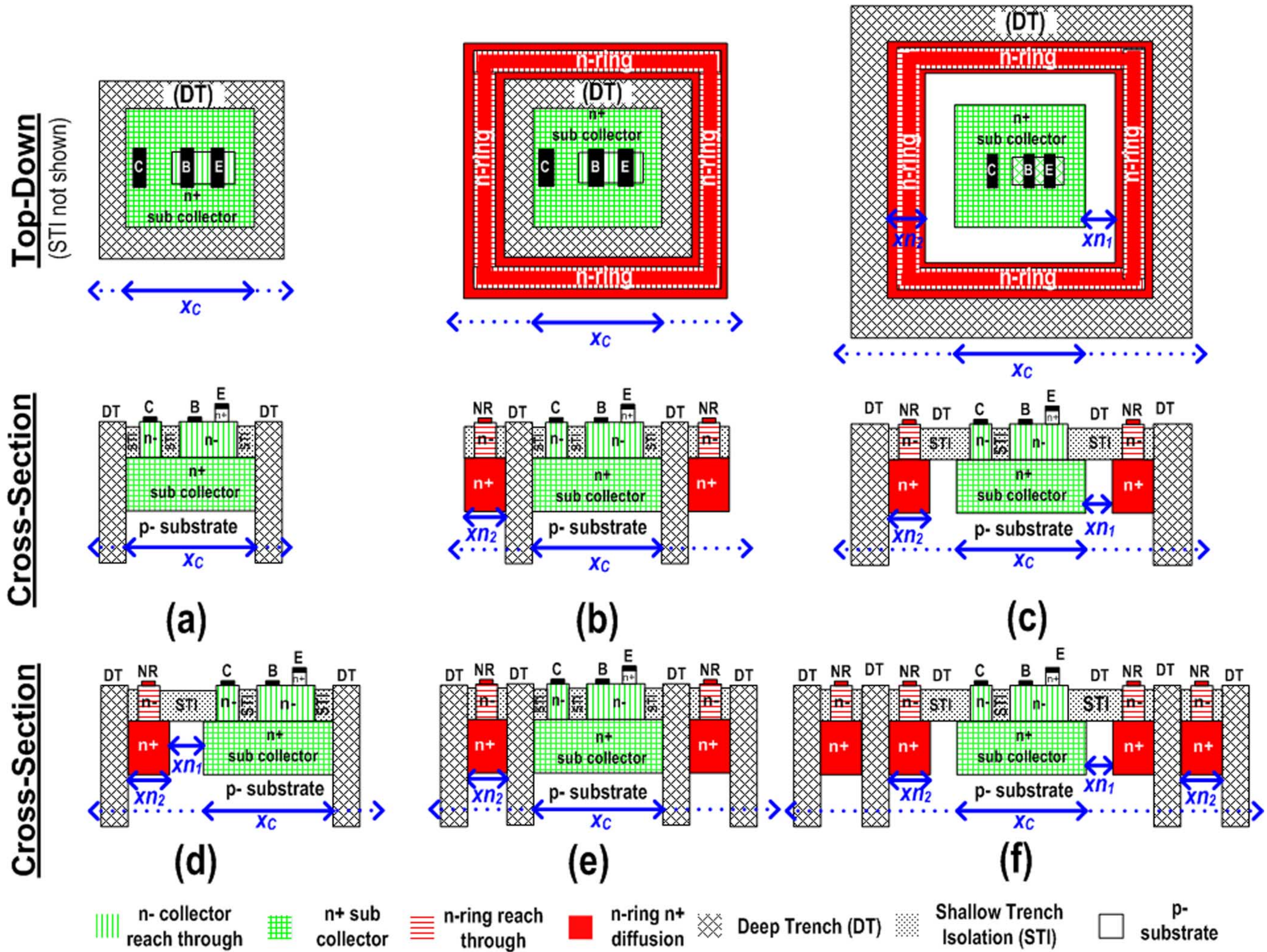

Fig. 1. Top down and cross-section views of the: (a) nominal-HBT (unhardened); (b) external R-HBT; (c) 3, 6, 8 μm R-HBT; and cross-section views of the (d) 1-sided 3 μm R-HBT, (d) 1NR, 2DT (3 μm R-HBT) (f) 2NR, 2DT (3 μm R-HBT). The key lateral dimensions x_C, xn_1 and xn_2 are shown.

II. Devices Under Test

A. RHBD Layout Variations

The SiGe HBT evaluated in this work features an $f_T/f_{\rm MAX}$ of 200/285 GHz, a $BV_{\rm CEO}$ of 1.7 V, and is offered alongside 130 nm CMOS in the commercially-available IBM 8 HP, seven metal layer (7 LM) SiGe BiCMOS process [10]. The device is fabricated on an 8–10 Ω-cm p-type substrate with an *in-situ* doped polysilicon emitter, raised extrinsic base, a conventional (5 to 7 μm) deep-trench (DT), and shallow-trench (ST) isolation. All devices are implemented in a single stripe CBE configuration, as opposed the larger double-collector, double-base stripe CBEBC configuration, featuring an emitter area (A_E) of 0.12×3.0 μm^2. The CBE configuration has a smaller internal trench area as discussed in [2]. The top down and cross section views of RHBD layout devices featuring a variety of n-ring placement and spacing are shown in Fig. 1(a)–(f). The lateral distance across the device is denoted as x_C, the width of the n-ring is denoted as xn_2, and the spacing between the internal n-ring and the device sub-collector is denoted as xn_1. The devices tested feature an n-ring width of 2 μm and a spacing varying from 3 to 8 μm. In the 8 HP process, a spacing less than 3 μm could result in an n-ring to sub-collector short as a result of dopant out-diffusion during device fabrication. A smaller n-ring spacing, allowing for a more compact and effective design, may be possible in other technology platforms with reduced doping levels. In this work we focus on the measured and simulation charge collection of the nominal-HBT, external R-HBT and the internal 3 μm R-HBT which have shown to be the most effective in SEE mitigation. Measured charge collection of alternate n-ring schemes such as the 1-sided 3 μm R-HBT (reduced $A_{\rm DT}$), 1 NR, 2 DT 3 μm R-HBT (external R-HBT + 2nd outside DT), and 2 NR, 2DT 3 μm R-HBT (internal + external R-HBT devices with a 2nd outside DT) are used to understand the charge collection dynamics.

The inclusion of the n-ring in the device layout affects neither the *dc* nor *ac* performance of the device (regardless of the applied V_{NR} or xn_1), as evidenced by the overlay of the forward-mode Gummel and f_T versus I_C characteristics shown in Fig. 2(a) and (b). In the case of the internal R-HBT devices, the maximum applicable V_{NR} (occurring when the substrate to n-ring depletion region contacts the device sub-collector) is proportional to xn_1, being reduced from 25 V at $xn_1 = 8$ μm to 9 V at $xn_1 = 3$ μm, for $V_C = V_B = V_E = 0$ V.

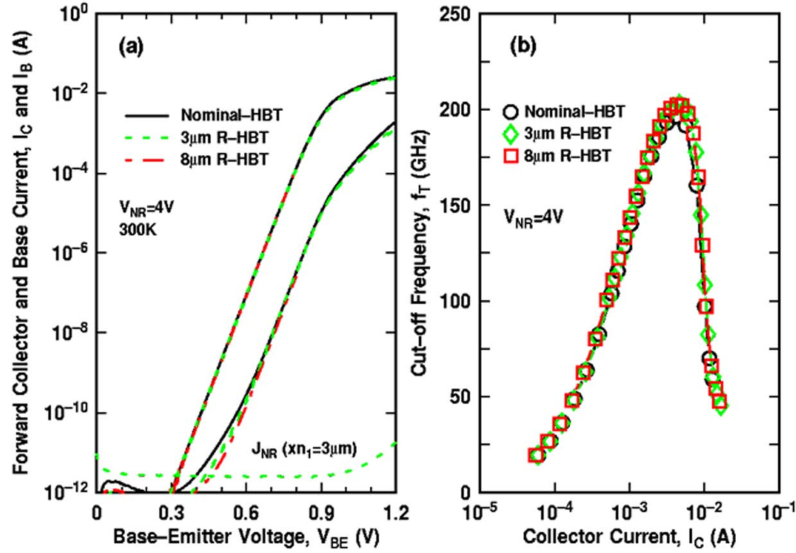

Fig. 2. RHBD impact on device performance: (a) Forward-mode Gummel comparison for the nominal-, 3 μm-and 8 μm R-HBT devices and, (b) f_T versus I_C characteristics of the nominal 3-and 8-μm R-HBT devices.

B. Experiment Details

Total ionizing dose (TID) tolerance of the 8 μm R-HBT device was evaluated via proton testing at the Crocker Nuclear Laboratory, the dosimetry system of which has been previously described in [11], [12]. Irradiations were performed to a cumulative dose of 3 Mrad (SiO_2) for $V_{NR} = \pm 3$ V with all device terminals grounded. The post-irradiation ΔJ_B for the 8 μm R-HBT is comparable to that of the nominal-HBT, indicating that TID tolerance has been maintained. This result follows from the fact that the inclusion of the n-ring does not alter the location of the emitter-base (EB) spacer and shallow trench isolation (STI) Si/SiO_2 interfaces, where radiation induced interface trap density (D_{it}) is expected to be highest [13].

Ion microbeam testing was performed at Sandia National Laboratory's ion beam induced charge collection (IBICC) facility [14]–[16]. 36 MeV ^{16}O ions, with a 1 μm spot size, a range of 25.5 μm in Si, surface LET of 5.2 MeV-cm^2/mg and a Bragg peak of 7.5 MeV-cm ^{2}/mg were stepped across a 100×100 μm^2 field encompassing the device active area. Charge collection on the 5 terminals (C, B, E, SX and NR) were monitored for $\theta = 0^\circ$ and 15° strikes. Prior to ion exposure, a non-destructive, fluorine-based reactive ion etch (RIE) was used to selectively remove several microns of inter-metal dielectric above the device, thereby increasing charge deposition in the substrate underlying the device active area. There was no measured degradation in the device performance characteristics.

III. Microbeam Results

The 3-D charge collection data was reduced by taking a 1 μm wide slice in the y-axis direction about the peak collector collected charge (Q_C) in the x-y plane and projecting it onto the x-axis (x_C in Fig. 1). A 1 μm slice was chosen to avoid sampling too many external DT events (slice widths >1 μm), and not capturing the charge collection profile (slice widths <1 μm). The peak Q_C and the path integral of Q_C along x_C ($Q_{C,\text{INT}}$) in (1) will be used as the key performance figure-of-merit for comparing the SEE mitigation capability of the various RHBD layout schemes. The peak Q_C is representative of collection resulting from an emitter center strike, whereas $Q_{C,\text{INT}}$ is representative of the sum of the collection resulting from strikes across the entire length (x_C) of the 1 μm slice

$$Q_{C,\text{INT}} = \int_a^b Q_C(x_C)dx_C. \tag{1}$$

Q_C is illustrated as a function of x_C, for the nominal-, 8 μm, 3 μm-, and external-HBT devices at $V_{NR} = 4$ V and $\theta = 0^\circ$ in Fig. 3. 36 MeV ^{16}O ions deposit 26 MeV of energy, generating 1.1 pC of charge in Si. Prior investigations (on IBM 7 HP), have determined a peak Q_C of approximately 1.0 pC, representing a 90% charge collection efficiency [17]. A normal incident emitter center strike will result in the largest amount of charge deposition, thereby corresponding to the observed peak Q_C. The nominal-HBT has a peak Q_C of 0.95 pC for strikes within the DT and over 0.1 pC of collector collection for external DT strikes. For the internal R-HBT device there was no observed reduction in the peak Q_C at 8 μm; however, as x_{n1} is scaled down to 3 μm, a slight reduction in peak Q_C is observed. The external R-HBT offers no immunity for strikes inside the DT but does an excellent job at reducing collection from external DT strikes.

A. N-Ring Bias

The value of V_{NR} for a given V_{SX} determines the reverse bias voltage of the substrate to n-ring junction and consequently the depletion width, electric field, electrostatic potential, and ultimately the drift-dominated charge collection volume. The path integrated collected charge for all device terminals as a function of V_{NR} is illustrated in Fig. 4(a) and (b) for the 3 μm R-HBT and external R-HBT, respectively. As expected from prior investigations [17] negligible charge collection is observed on the base and emitter. Charge collection on the remaining terminals is balanced ($Q_{C,\text{INT}} + Q_{NR,\text{INT}} = Q_{SX,\text{INT}}$). Increasing V_{NR} yields a noticeable increase in $Q_{NR,\text{INT}}$ and $Q_{SX,\text{INT}}$ together

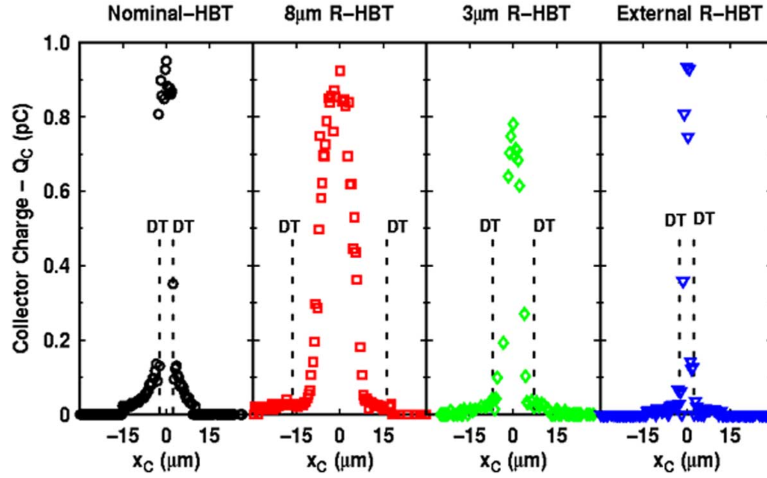

Fig. 3. Q_C as a function of x_C for the (a) nominal, (b) 8 μm, (c) 3 μm, and (d) external R-HBT. $V_{NR} = 4$ V for all R-HBT devices.

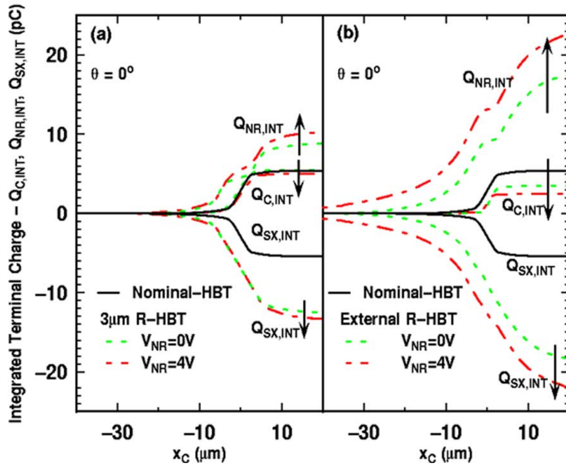

Fig. 4. Path integrated terminal charge ($Q_{C,\mathrm{INT}}$, $Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$) for the (a) 3 μm R-HBT and (b) external R-HBT for $V_{NR} = 0$ and 4V and $\theta = 0°$.

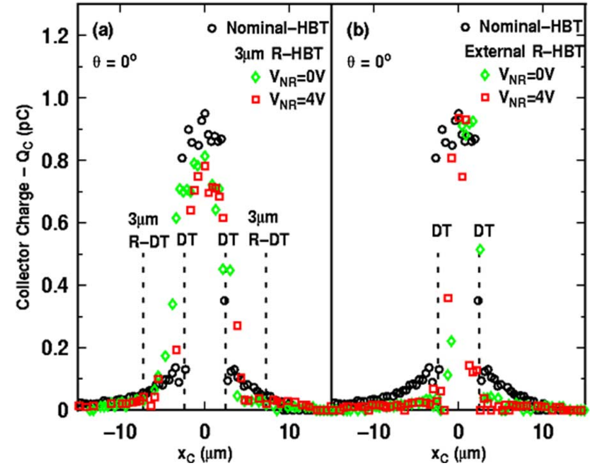

Fig. 5. Q_C as a function of x_C and V_{NR} for the (a) 3 μm R-HBT and (b) external R-HBT at $\theta = 90°$.

with a slight decrease in $Q_{C,\mathrm{INT}}$. The external n-ring collects approximately 2X more charge than the 3 μm internal ring, and demonstrates a larger percentage increase in $Q_{NR,\mathrm{INT}}$ as V_{NR} is increased. Q_C is depicted as a function of x_C at $V_{NR} = 0$ and 4 V for the 3 μm R-HBT and external R-HBT as shown in Fig. 5(a) and (b), respectively. Although the external n-ring collects 2X more charge than the 3 μm R-HBT, it offers no mitigation for emitter center strikes, while the 3 μm internal ring at $V_{NR} = 4$ V yields an 18% reduction in peak Q_C. Moreover, changes in V_{NR} have very little effect on the peak Q_C for both the internal and external ring devices.

B. Strike Location and Angle of Incidence

In addition to V_{NR}, the strike location (relative to the DT) and angle of incidence, θ, also impact the observed charge collection. Q_C is plotted on a logarithmic scale as a function of x_C for the nominal-, 3 μm R-HBT and external R-HBT devices at $V_{NR} = 4$ V for $\theta = 0°$ and 15° in Fig. 6(a) and (b), respectively. A strike through the center of the emitter presents the largest volume for charge deposition and un-recombined carriers are efficiently collected via drift and funneling [5]. Strike locations on the outside of the DT generate electron-hole pairs that must first diffuse under the DT before they can be collected via drift, resulting in a Q_C that is at least an order of magnitude smaller. The external n-ring provides up to 90% reduction in Q_C from strikes originating in this region, while the 3 μm ring device provides only a small reduction.

The nominal-HBT, external R-HBT, and 3 μm R-HBT all yield approximately 20% reduction in observed in peak Q_C for internal DT strikes and an increasingly asymmetric external DT collection component when θ is increased from 0° to 15°. External DT collection is also reduced, as evidenced by a rapidly decaying Q_C in the case of the nominal- and 3 μm R-HBT, and complete suppression for the external R-HBT as shown in Fig. 6(b). At $\theta = 15°$, $Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$ are also reduced (when compared to $\theta = 0°$), as illustrated in Fig. 7(a) and (b).

The effective LET, described by the inverse cosine law, $(\mathrm{LET_{eff}} = \mathrm{LET_0}/\cos\theta)$ has traditionally been used to model enhanced charge collection at large θ. There have been, however, several experimental results that contradict the validity of

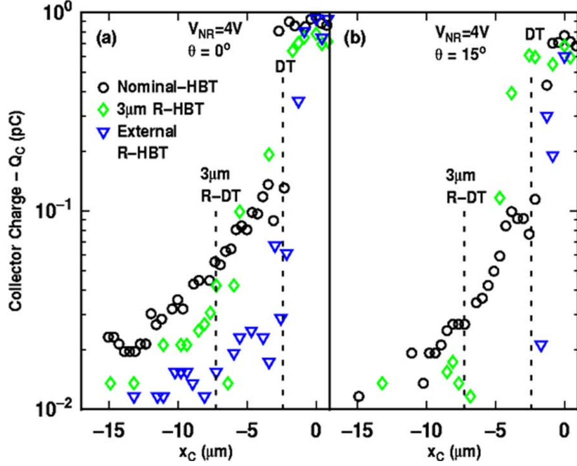

Fig. 6. External DT collection for the nominal-HBT, 3 μm R-HBT, and external R-HBT for $V_{NR} = 4$ V at (a)$\theta = 0°$ and (b) $\theta = 15°$.

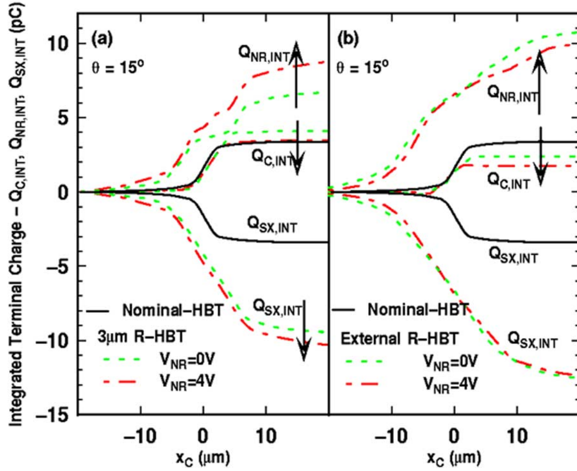

Fig. 7. Path integrated terminal charge ($Q_{C,\text{INT}}, Q_{NR,\text{INT}}$, and $Q_{SX,\text{INT}}$) for the (a) 3 μm R-HBT and (b) external R-HBT for $V_{NR} = 0$ and 4 V and $\theta = 15°$.

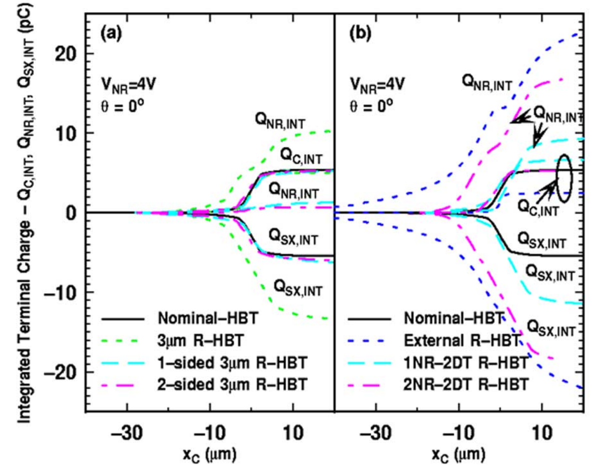

Fig. 8. Path integrated terminal charge ($Q_{C,\text{INT}}, Q_{NR,\text{INT}}$, and $Q_{SX,\text{INT}}$) for the (a) reduced A_{DT} devices: 1-, 2-sided 3 μm R-HBT compared to 3 μm R-HBT and (b) double DT devices: 1NR-2DT R-HBT and 2NR-2DT R-HBT compared to external R-HBT. All comparisons at $V_{NR} = 0$ and 4 V and $\theta = 0°$.

this model, as discussed in [18] for the case of CMOS SRAMs. In the case of the 7 LM 8 HP process used here, a larger θ translates into an increased path length in the over-layer material, resulting in reduced ion energy (and charge deposition) in the substrate. Additionally, perturbation of the ion track through the DT may contribute to reduced internal DT collection.

C. Alternate N-Ring Schemes

One of the major drawbacks of the internal ring structure is the increase in the enclosed trench area (A_{DT}), and resulting increase in the drift dominated charge collection volume. To further reduce A_{DT}, the ring may be converted into a single- or double-tap structure, as illustrated in Fig. 1(d). Although A_{DT} is now smaller, these structures suffer from a reduction in the total n-ring area, and the resultant $Q_{NR,\text{INT}}$ is reduced by almost 90% compared to the 3 μm R-HBT, as shown in Fig. 8(a). In this case the substrate to collector junction area is larger than the substrate to n-ring junction area, resulting in an increased $Q_{C,\text{INT}}$. Charge balance is still maintained $(Q_{C,\text{INT}} + Q_{NR,\text{INT}} = Q_{SX,\text{INT}})$

The external R-HBT has demonstrated the largest reduction in external DT collection, but little mitigation in the event of an emitter center strike. The substrate to n-ring junction for this device is not bounded by DT, thereby enabling both vertical and lateral collection. Encapsulation of this external ring [i.e., going from Fig. 1(b) to Fig.1(e)] by a 2nd DT results in over 50% reduction in $Q_{NR,\text{INT}}$, as shown in Fig. 8(b), as much of the lateral directed drift collection is now shut down. An obvious approach would be to combine external and internal rings in the same device. This is the case for the 2NR-2DT shown in Fig. 1(f). As shown in Fig. 8(b), $Q_{NR,\text{INT}}$ increases significantly for this device with a corresponding decrease in peak $Q_{C,}$ and $Q_{C,\text{INT}}$ approximately equal to that of the 3 μm R-HBT device, but at a 2X area penalty.

A summary of the observed charge collection is presented in Table I. In addition to peak Q_C and $Q_{C,\text{INT}}$, the charge collected for strikes approximately 1 μm outside of the DT (the bounding trench for that specific device) is also tabulated (Q_C (DT+1)). As shown previously, the inclusion of the external n-ring results in a 90% reduction in the collected charge from events outside of the trench. This is the driving force behind the 53% reduction in the overall $Q_{C,\text{INT}}$ for the external R-HBT (the best out of all devices tested). The addition of a 2nd DT on the outside of this structure [i.e., Fig. 1(e)] slightly reduces the advantage to 85% (although now events outside the trench are further away from the sub-collector).

IV. Charge Collection Simulations

3-D charge collection simulations were performed using the NanoTCAD simulation package [19], which has been previously been used to simulate radiation effects on a range of modern IC technologies [20]–[22]. Layout information, from substrate through to 1st level metal, was imported from Cadence, into a meshing utility, in GDS II format. Next, a solid geometry model of the transistor was constructed using a binary tree mesh represented as a $26 \times 26 \times 25$ μm^3 volume with local refinement of the mesh in the vicinity of

TABLE I
CHARGE COLLECTION FOR ALL DEVICES AT $\theta = 0°$ AND $15°$

Device	A_{DT} (μm²)	A_{NR} (μm²)	Q_C *(E)* (pC)	Q_C (DT+1) (pC)	$Q_{C,INT}$ (pC)
Nominal-HBT	11	NA	0.950	0.133	5.34
3 μm R-HBT	172	29	0.781	0.017	3.16
6 μm R-HBT	363	43	0.888	0.039	9.55
8 μm R-HBT	972	54	0.924	0.027	11.63
External R-HBT	11	59	0.935	0.012	2.48
1-sided R-HBT	24	1.2	0.878	0.115	5.36
2-sided R-HBT	37	2.4	0.845	0.102	5.36
1NR-2DT	69	16	0.978	0.021	6.68
2NR-2DT	326	68	0.749	0.020	5.33
at $\theta = 15°$					
Nominal-HBT	11	NA	0.766	0.051	3.38
3 μm R-HBT	172	29	0.679	0	3.46
External R-HBT	11	59	0.602	0	1.74

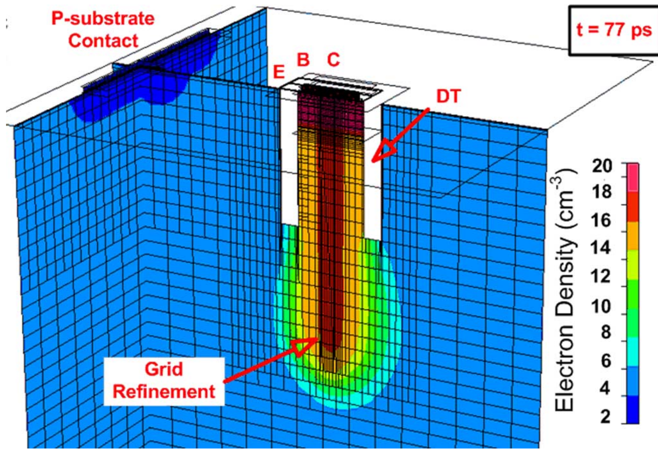

Fig. 9. X-cut through a 3-D solid geometry mesh of the nominal-HBT showing the electron density 77 ps following an emitter center strike.

the ion strike, as shown in Fig. 9. The EB spacer and DT oxide volumes were not meshed. In order to maintain such a relatively small volume (to be computationally efficient), and avoid reflective boundary conditions at the edges (which is non-physical), a "wrapping layer" with an artificially low lifetime ($\tau_{WR} = 50$ ns), encased the entire substrate volume. A standard substrate lifetime of 9 μs was used throughout the bulk region. Secondary ion mass spectroscopy (SIMS) data was used to reproduce the doping profiles, which are represented as a series of rectangular well regions with a constant dopant density enclosed by Gaussian distributed tails along the edges. Physical 3-D device models included doping-dependent carrier lifetimes, SRH and Auger recombination, and mobility models which accounted for doping, electric field and carrier-carrier scattering dependences.

Ion strike simulations were performed using a two step approach. First, steady-state conditions were established by the specification of initial boundary and volume conditions, and solution physics specific to the problem. Next, a transient ion strike simulation was performed using the steady-state solution as an initial condition. Normally incident ions were simulated at an LET of 0.07 pC/μm, a range of 13.72 μm (to account for 8 μm of dielectric), and Gaussian-distributed charge track peaking at 2 ps and with a *1/e* characteristic time scale of 0.25 ps and radius

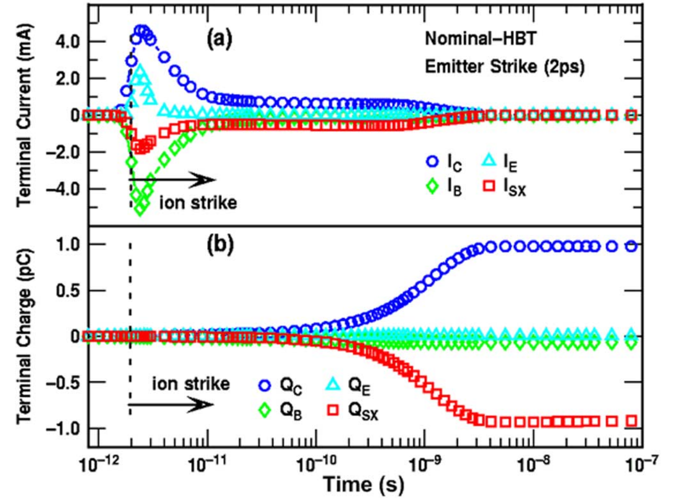

Fig. 10. Transient simulation results for an emitter centered ion strike to the nominal-HBT: (a) currents (I_C, I_B, I_E, I_{SX}), (b) charge (Q_C, Q_B, Q_E, Q_{SX}).

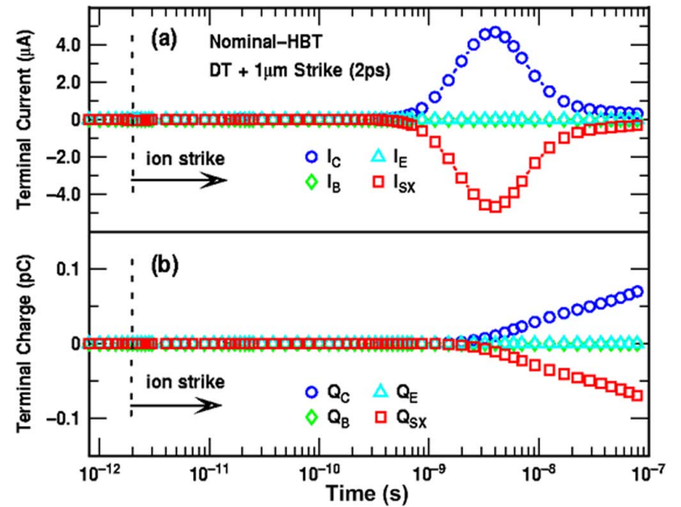

Fig. 11. Transient simulation results for an external DT ion strike to the nominal-HBT: (a) currents (I_C, I_B, I_E, I_{SX}), (b) charge (Q_C, Q_B, Q_E, Q_{SX}).

of 0.1 μm. To account for the potential impact of TID on charge collection, interface traps ($D_{\mathrm{IT}} = 5 \times 10^{11}$ cm^{-2}) were placed along all SiO_2 interfaces. Trap densities that were typical for studying TID effects in BJTs [23] were selected to match experimental charge collection data. Ion strikes on the external R-HBT and 3 μm R-HBT devices utilized similar model parameters as the nominal-HBT, with the exception that the lateral size of the 3-D model was extended to 40×40 μm^2. NanoTCAD was used to solve the fundamental carrier continuity and Poisson equations using the finite volume numerical method and post-processing performed using CFD-View. A typical ion strike simulation (to $10+$ μs) takes 3 hours on a 2.4 GHz Pentium PC.

Transient terminal current charge collection profiles from a normal-incident ion strike at 2 ps through the emitter center, and through the external DT, are shown in Figs. 10 and 11, respectively. The current waveforms are composed of a 5–10 ps long prompt component soon after the strike (drift dominated), followed by a time-delayed component (diffusion dominated)

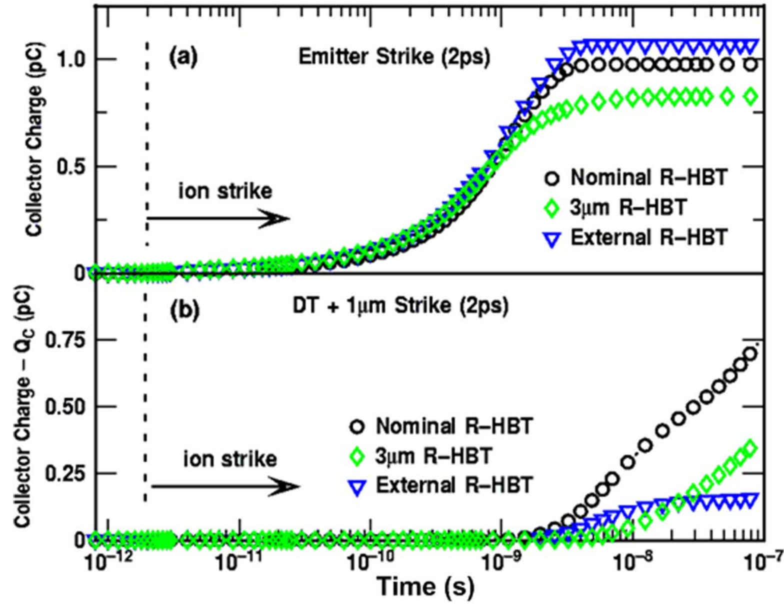

Fig. 12. Transient simulation results for nominal-, 3 μm R-, and external R-HBT showing Q_C (a) emitter centered (b) external DT strikes.

lasting up to 2 ns after the strike, as shown in Fig. 10(b). Prompt collection is observed on all terminals; however, delayed collection is only observed on the collector (electrons) and substrate (holes) terminals, which account for the majority of the collected charge, as shown in Fig. 10(b). These results are in reasonably good agreement with 3-D DESSIS ion strike simulations on 8 HP SiGe HBTs presented in [7] and [24]. In Fig. 11(a) an external DT strike result is shown to produce a delayed collection component observed only on the collector and substrate terminals. The peak of this delayed current component is observed 3–4 ns after the strike and is three orders of magnitude less than the prompt current component resulting in 0.07 pC collected after 100 ns (as opposed to 1 pC for the prompt current component), as shown in Fig. 11(b).

Transient Q_C for the nominal-HBT are compared with those of the 3 μm and external R-HBT devices, for an emitter center and external DT ion strike, as shown in Fig. 12(a) and (b). The inclusion of the substrate to n-ring junction results in the creation of a parasitic n(*collector*)-p(*substrate*)-n(*n-ring*) transistor. Under steady-state conditions ($V_{SX} = -4$ V, $V_{NR} = 0, 4$ V, $V_C = 0$ V), this device is in cut-off mode as both *pn* junctions are reverse-biased. In the aftermath of an ion strike, however, potential contours in the local vicinity of the strike are such that this parasitic BJT can be turned on (up to 0.5 ns after the strike) enabling a direct conduction path from the n-ring to the collector ($I_{NR} < 0$). In the case of the external DT strikes, the parasitic current flow is now from the collector to the n-ring ($I_{NR} > 0$) and also lasts up to 0.5 ns. A comparison of the measured and simulated Q_C is shown in Fig. 13(a) and (b), respectively. Each simulated Q_C represents a transient current integral over 14 μs. There is reasonably good agreement for drift-dominated strikes in the interior, while for strikes outside the DT there is some deviation between the simulated and measured results. Additional factors to consider include charge funneling collection and the impact of secondary particles generated from nuclear interactions within overlaying metallization.

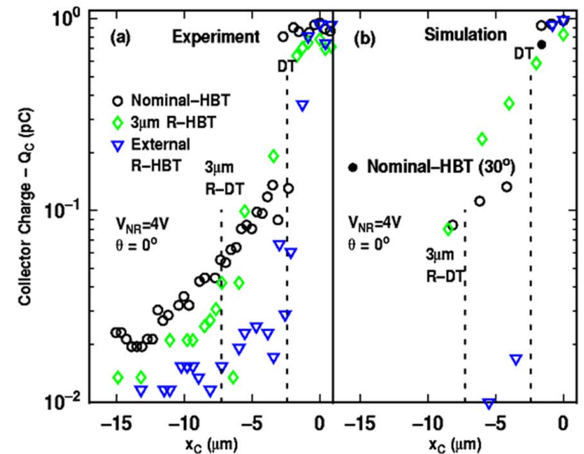

Fig. 13. Comparison of (a) experimental and (b) simulation results of Q_C as a function of x_C for the nominal-, 3 μm R-, and external R-HBT.

V. Discussion

An experimental evaluation of several layout-based RHBD techniques for SEU mitigation in SiGe HBTs has been presented and confirmed using 3-D transient ion strike simulations. In the best case scenario, reductions of 53% in $Q_{C,\mathrm{INT}}$ and 21% in peak Q_C have been demonstrated on two different R-HBT structures. These values compare well with the reductions achieved via employing varying epitaxial thicknesses [25], but are substantially lower than the reductions achieved via putting the SiGe HBTs on SOI [26], and ultimately still result in Q_C values much larger than the typical critical charge ($Q_{\mathrm{crit}} = 100$ fC) determined for SEU in high-speed SiGe BiCMOS circuits [9]. However, a strictly layout-based variation technique applied to

a bulk SiGe technology has the desirable advantage of being lower in cost compared to process changes (e.g., moving to SOI) for SEU robustness. Additionally, device layout approaches do not incur the increases in circuit area and power consumption common to many circuit hardening techniques. Similar layout-based approaches have been successful in SEU mitigation for CMOS, as demonstrated in [27] and such work for the SiGe HBT clearly warrants further investigation. Although the reductions in Q_C for emitter-center strike will not prevent an upset, the level of suppression of collection from external DT events is quite substantial. Assuming carrier diffusion lengths on the order of 100 μm or more (outside the DT), there is a considerable amount of charge that could potentially be diverted away from the transistor in a broad-beam environment, when there are a substantial number of strikes outside the DT.

Increasing the A_{NR}/A_{DT} ratio is critical in lowering Q_C, and to this end additional structures that increase n-ring width (thereby increasing A_{NR} within the same A_{DT}), while reducing xn_1 would be beneficial. We have demonstrated that in SiGe 8HP, an xn_1 of 2 μm results in an n-ring to collector short, quantifying the limitation of the technique as it applies to internal ring structures. This limitation may be overcome by reductions in the back end of the line (BEOL) thermal cycles and a reduction in the sub-collector doping levels. Another approach may be the combination of process driven hardening techniques (such as the epitaxial Si thickness [25] or SOI [26]), with the layout driven use of the n-ring. Alternatively a buried n-ring, analogous to the triple wells used in CMOS may be considered.

Ultimately, the success of any SiGe RHBD SEE mitigation technique will be determined by the cross-section (σ) versus LET response obtained via broad-beam heavy-ion analysis of actual circuits. The IBICC technique employed in this work gives a good indication, however, of the extent to which layout-based charge collection mitigation is effective, at least for shallow ion strikes. We believe that the ultimate SEU hardening success in SiGe will be achieved via a combination of layout-level RHBD and latch-level RHBD techniques implemented without excessive spatial or temporal redundancy techniques such as TMR. The external n-ring can extended to encompass several minimum spaced devices in a flip-flop or differential pair thereby minimizing the overall area penalty on the circuit level. Compared to TMR, this should yield a 60% reduction in circuit area. The circuit level power penalty will be minimal as the n-ring draws extremely low current (pA) when biased. The technique can also be adapted to mixed signal and analog applications by hardening, the input HBT pair in an operational amplifier for example. Pulsed laser analysis time resoled IBICC techniques could then be used to correlate RHBD charge collection mitigation on the single event transient characteristics.

VI. SUMMARY

Transistor-based layout techniques for mitigating heavy ion triggered charge collection in SiGe HBTs, through the addition of internal and external n-rings, has been presented and validated using ion beam induced charge collection techniques together with 3-D transient ion strike simulations. Up to 90% reduction in collected charge for events outside the DT, and 21% reduction in collected charge for events inside the DT have been demonstrated.

ACKNOWLEDGMENT

The authors would like to thank L. Cohn, K. LaBel, P. Dodd, J. Nance, J.P. Comeau, and the IBM SiGe team for their contributions to this work.

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Ion beam induced charge (IBIC) studies of silicon germanium heterojunction bipolar transistors (HBTs)

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Available online 14 February 2007

Abstract

SiGe HBTs are strong candidates for space communication applications because of their resistance to total dose effects and their overall high performance. However, they seem to be sensitive to single event upsets (SEUs). These devices were designed using deep trench isolation geometry to reduce charge collection due to ion hits outside the active area. Using four electrode (base, emitter, collector, and substrate) IBIC measurements at the Sandia Nuclear Microprobe Facility, we found that the largest fraction of the induced charge occurred on the collector and on the substrate; significantly less induced charge was found on the base electrode, and practically no induced charge was detected on the emitter. These devices showed a very well defined, high charge collection area enclosed by the deep trench. There was a sudden drop of induced charge at the trench but a long tail was present outside of the active area extending several tens of microns. The charge collection mechanisms inside and outside of the deep trench will be discussed and first results of Time Resolved IBIC in SiGe HBTs will be presented.
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PACS: 81.05.Hd; 61.80.−x; 81.40.Wx

Keywords: IBIC; TRIBIC; SiGe; Radiation effects; Single event upset

1. Introduction

Most of today's electronics is based on silicon. Silicon has many advantages over other semiconductors. It is available in large amounts and can be purified to very high grade (<10^{10} impurities/cm^3). It can be grown into large, defect-free single crystals and can be easily doped with either n-type or p-type impurities in a high dynamic range. One of the most important properties of silicon is that an extremely high quality dielectric (SiO_2) can be grown on it using simple methods. Silicon is a perfect material for system-on-chip (SOC) technology since several different kinds of devices can be built on the same chip. Analog (bipolar junction transistors (BJTs)) and digital (metal-oxide-semiconductor field emission transistors (MOS FETs)) devices can be manufactured and connected on the same wafer. Unfortunately, silicon has its limitations. The carrier mobility in silicon is relatively small; it saturates around 10^7 cm/s at high electric fields. Also, since silicon is an indirect bandgap semiconductor, it has very low light emission efficiency. The communication industry today requires higher speeds and high levels of integration for its integrated circuits (ICs) at low cost. In addition, the space industry wants to find an IC technology that is radiation hard for space application without additional radiation hardening which usually leads to increased cost, speed degradation, and area penalty. An alternative to

[1] Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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0168-583X/$ - see front matter © 2007 Published by Elsevier B.V.
doi:10.1016/j.nimb.2007.02.032

the silicon technology are devices based on the III–V semiconductors, such as GaAs. These devices have the carrier mobility required for high speed ICs, and due to the way they are fabricated, they allow bandwidth engineering which is beneficial for optical devices. But there are practical disadvantages as well of these materials. First of all there is no robust thermally grown oxide for these materials. The single crystal wafers are also generally smaller compared to the silicon ones, and they have much higher defect density and poorer thermal and mechanical properties. All these lead to lower yields and consequently to higher cost. The III–V semiconductor technology has its place in the world of electronics, but it will never become a mass production technology if silicon based technologies can achieve or even approach the performance levels that these other technologies offer.

A promising new technology that combines the high speed of the III–V semiconductors with the well established and easy manufacturing processes of silicon is based on SiGe. The SiGe alloy allows the bandgap engineering of silicon devices while keeping the same fabrication technology developed for silicon devices; therefore, the analog BJTs can be easily combined with digital CMOS devices on the same wafer. These new devices are very promising; a current, very detailed review of the technology and the characteristics can be found in [1]. The SiGe HBTs can perform comparably to the III–V devices, and an additional bonus is that they were shown to be extremely radiation hard considering total dose and displacement damage [1]. However, it was shown through experiments [2,3] and simulations [4] that these devices can be vulnerable to single event upsets (SEUs). SEUs are changes in the logical state of a circuit due to the current induced in the device by the movement of the carriers created by an incident heavy ion. In order to understand the mechanism of SEUs it is necessary to study and understand the ion beam induced charge induction in the device. This study can be done through simulation using various device codes or experimentally using the ion beam induced charge/current (IBIC) technique. The simulations are usually compared to the experiments to calibrate/validate the calculations. We used the Sandia National Laboratories (SNL) nuclear microprobe facility to perform IBIC experiments on various SiGe HBT structures. Simulations were carried out to model the spatial distribution of the IBIC signal (induced charge). Finally, we performed the first Time Resolved IBIC (TRIBIC) experiments on these structures. The TRIBIC results provide more information for the simulation validation/calibration since they measure the induced current/charge as a function of time instead of only the total induced charge as the IBIC experiments do.

2. Experimental

In these experiments we used SiGe HBTs from various vendors, but they basically had the same structure as shown in Fig. 1. All the devices underwent chemical vapor etching to remove all but about 7 μm of the dielectric and metallization stack. This process allowed the ions to penetrate deeper into the device. For these experiments a beam of 36 MeV oxygen ions was focused into a 1 μm^2 spot and scanned over generally a 50×50 μm^2 area. These oxygen ions have a range of 25.5 μm and deposit a total of ~1.7 pC of charge in silicon. All four electrodes (collector, base, emitter, and substrate) were connected to amplifier chains consisting of Ortec 142A charge sensitive preamplifiers and Ortec 671 spectroscopy amplifiers. In addition, the signals were fed into individual SCAs which were then connected to a four input OR logical unit. The output of the logical OR unit was connected to the gates of the ADCs for the *X*–*Y* scan generator's output that were operated in SVA mode. All the ADCs were connected to a FastCom MPAWIN multi-parameter system. This way a signal on any of the four channels triggered an event in the MPAWIN system. The data were recorded in a list file and processed off-line later. During the experiments all the

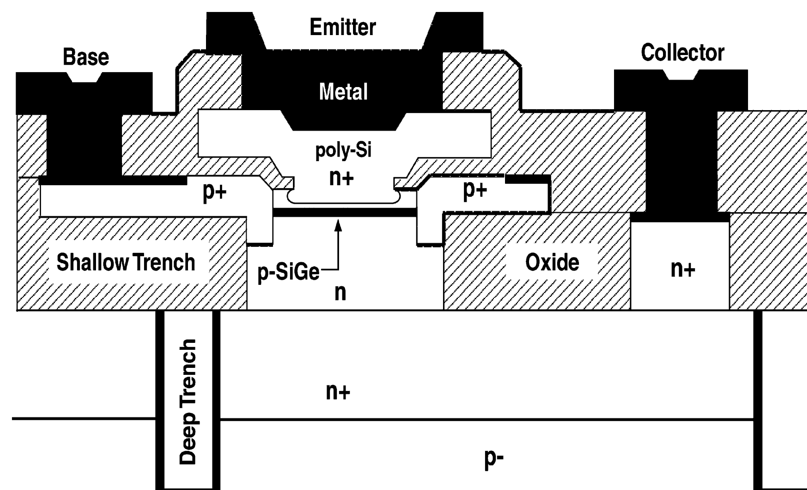

Fig. 1. Typical cross-section of a SiGe HBT after [1].

transistor electrodes were connected to ground except the substrate electrode, which was connected to negative bias to simulate a worst case scenario. The total induced charge was calibrated to the charge induced in a Hamatsu PIN diode.

3. Results and discussion

Fig. 2(a)–(c) show the 2D maps of the induced charge on the collector (a), base (b), and substrate (c) electrodes. There was no detectable signal of the emitter. Notice there is a different color scale for the induced charge for the base electrode. In case of this particular device the area enclosed by the deep trench isolation (see Fig. 1) was about 4 μm (width) × 10 μm (length). The figures demonstrate a very well defined rectangular high charge induction area (red)[2] that coincides with the location and size of the area enclosed by the deep trench isolation. Outside of this area there is a much lower charge induction region (blue) that has the shape and size of the deep trench. Further away from the center the amount of charge is higher again (green), and it takes the shape of an ellipsis. This charge gradually fades away, keeping the shape of the area the same. These features are more pronounced in Fig. 3 where we show a cut along the x-axis through the center of the red area averaging the signals over 4 μm. Fig. 2(c) shows the charge induction map for the base electrode. The area of the measured induced charge corresponds roughly (within the microbeam resolution) to the actual area of the base.

The first thing that we have to consider to interpret these results is the Gunn theorem [5] that states

$$I_i = -q\mathbf{v}\frac{\partial \mathbf{E}}{\partial V_i}, \tag{1.1}$$

i.e. the induced current in an electrode (I_i) is equal to the product of the charge of a carrier (q), its velocity ($\mathbf{v}$), and the differential of the electric field with respect to the voltage on the electrode while all the other voltages are kept constant. By applying this theorem to the structure of the device in Fig. 1, we can deduce why there is no signal from the emitter and why the base signal is so small and limited to a small area while there is a large signal from a large are on the collector and substrate electrodes. By changing the voltage on the emitter electrode, the only region where the electric field changes is in an extremely small area right below the emitter. Additionally, even a large change in the emitter voltage produces small field change. The base voltage has slightly more effect but is limited to the area of the base collector junction (p-type SiGe base and n-type collector). On the other hand, there is a large area, the p^-n^+ junction between the n^+ subcollector and the p-type substrate. Any change in the substrate or collector voltage (when this junction is in reverse biased mode) changes the properties of this depletion region; therefore, it changes the field in it. In addition, most of the charge is deposited in this region when an ion hits within the deep trench isolation area. This explains the small area and low charge induction in the base electrode and the very well defined high charge induction area for the collector and substrate electrodes. The sudden drop at the edge of this high charge induction area is due to the ions hitting the deep trench isolation. The elliptical lower charge collection area in the collector and substrate maps is due to ion hits outside of the deep trench. Since the deep trench itself is only 8–9 μm deep, the oxygen ions penetrate deeper in the substrate beyond the depletion layer. Carriers created in this region can move by ambipolar diffusion to the edge of the depletion layer where they will then drift through the fielded region inducing current in the collector and substrate electrodes. The elliptical shape of this region is a good proof of this diffusion-driven process in addition to the exponentially decreasing charge induction profile. Using a simple model of the diffusion of carriers into the depletion layer, a fit to the exponential profiles gives about 4 ± 0.1 μm for the diffusion length of the ambipolar diffusion in the p substrate. We have to mention that the Gunn theorem cannot account for the effect of funnel creation that is always present with high energy heavy ions. The electron–hole plasma created by these ions is so dense that it pushes out the electric field along the particle track in the device. In this case this funnel will increase the amount of the induced charge for ion hits within the trench with respect to the charge calculated from the Gunn theorem.

There are several mitigation techniques being developed to reduce this diffusion charge; one such technique involves using a charge-blocking buried layer. Simulation of this buried layer's effect on the induced charge is shown in Fig. 4 [6].

These IBIC measurements proved to be useful tools to calibrate device simulation codes. Fig. 5 shows the measured and simulated (after calibration to the measurement) charge induction profile for an IBM 5HP SiGe HBT. The details of how the microbeam IBIC measurements can be used to calibrate device simulation codes can be found in [6].

An interesting effect can be observed when the ion beam is incident on the device at an angle instead of normal to its surface. Figs. 6 and 7 show the 2D charge induction map of the collector electrode and the profiles along the x-axis across the center for a 36 MeV oxygen beam incident at ~20° to the normal of the surface (we omitted the 2D maps for the base and substrate to save space). There are several features that are worth noticing. The charge induction map and profile is not symmetric anymore; it is higher at the right trench and lower at the left trench. Another feature that is different from Figs. 2a and 3 is the lack of the drop in the charge induction when an ion hits the trench. These phenomena can be explained qualitatively as follows. When an ion hits the device close to the right edge of the device (the ions are coming from the right to the left) it will create more carriers in the depletion layer (crossing it diag-

[2] For interpretation of color in Fig. 2, the reader is referred to the web version of this article.

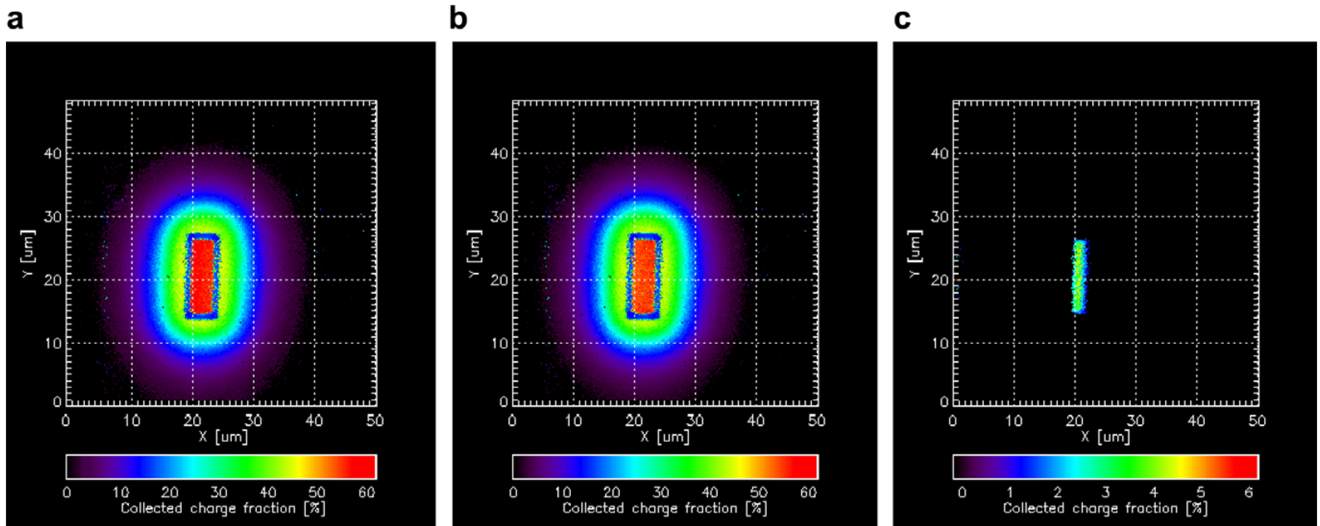

Fig. 2. 2D IBIC maps of induced charge on the collector (a), base (b), and substrate (c) electrode.

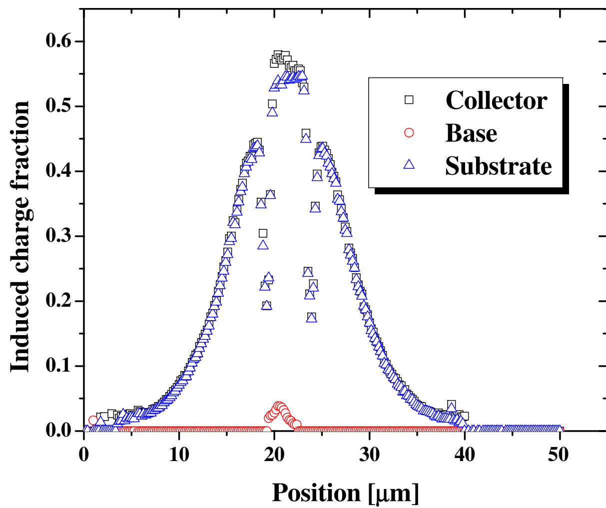

Fig. 3. Cut along the x-axis across the center of the 2D maps in Fig. 2(a)–(c). The curves are the averages over 4 μm in the y-direction.

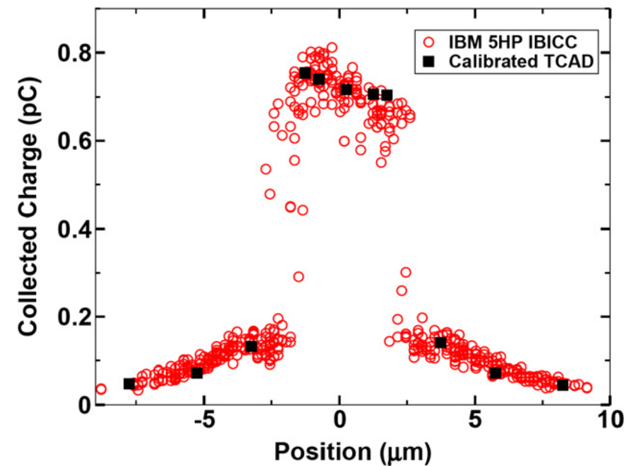

Fig. 5. Simulated and measured charge induction profile across an IBM 5HP SiGe HBT [6].

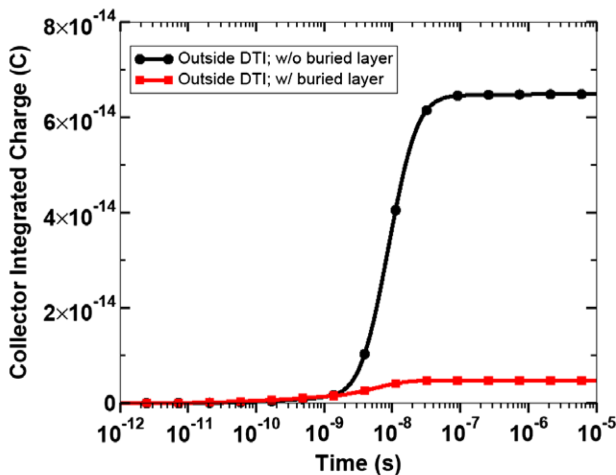

Fig. 4. Simulated charge induction curves for ion hits outside of the trench isolation area with and without a charge-blocking buried layer [6].

onally instead of perpendicularly) and its funnel extends further. When ions hit close to the left edge a significant part of their path goes through and outside of the trench. This also explains why the edges (where the charge induction dropped previously) are smeared out. A detailed discussion of both experiments and device simulations of angular strikes for these structures can be found in [7].

We performed both IBIC and TRIBIC measurements on one of the devices. This device's geometry was somewhat different from the ones shown above as can be seen from Fig. 8; it had more of a square collector area than the long rectangular area of the previous devices. It also showed a significantly smaller diffusion contribution to the induced charge as shown in Fig. 9. The collector signal was directly connected to the 50 Ω input of a TDS7404 oscilloscope with 4 GHz analog bandwidth and 20 Gsample/s sampling rate. In a $50 \times 50\ \mu m^2$ scan (identical to

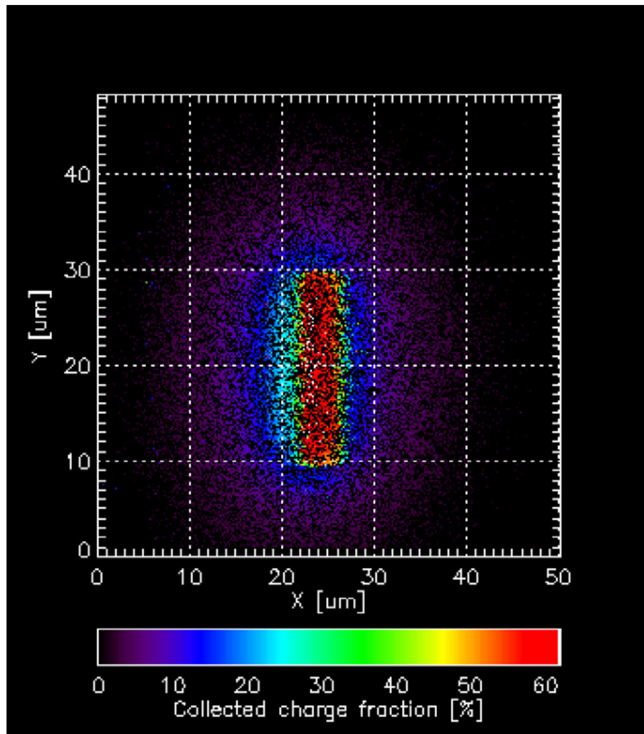

Fig. 6. 2D charge induction map on the collector electrode for oxygen ions incident at ~20° to the surface normal of the device.

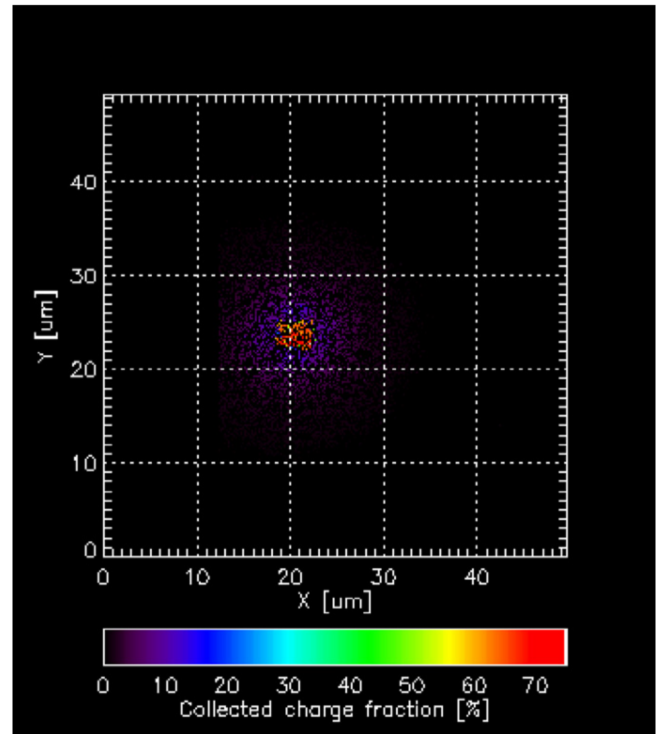

Fig. 8. 2D charge induction map of the collector of square shaped device.

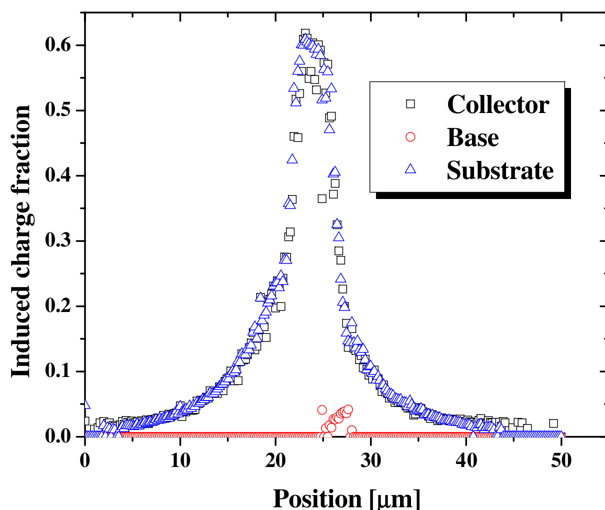

Fig. 7. Charge induction profile along the x-axis through the center of the charge induction map shown in Fig. 6.

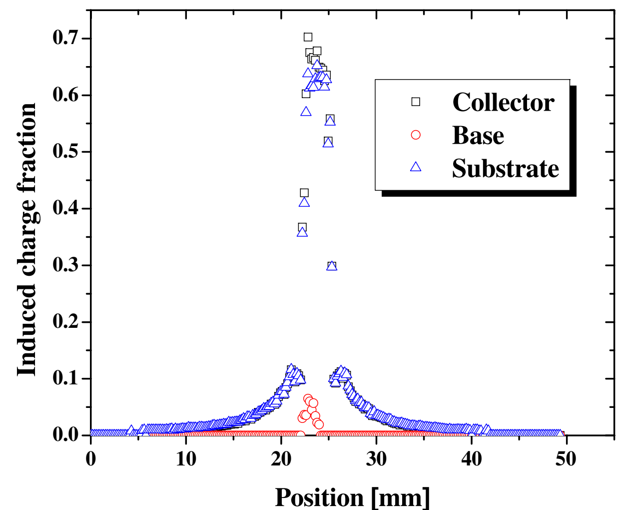

Fig. 9. Charge induction profile along the x-axis thorough the center of the charge induction map shown in Fig. 8.

the one in Fig. 9) we were able to detect only signals from hits from the area enclosed by the deep trench isolation area. This was more or less what we expected since the induced charge was about a factor of six smaller outside the trench than inside. Furthermore, since the charge induction due to hits outside of the trench is due to the diffusion of carriers to the depletion layer we can expect a much slower signal, which means currents more than an order less than in case of the drift signal. The magnitude of the current signal from outside of the trench was just too small to be able to trigger the oscilloscope. Fig. 10 shows a typical current signal. We suspect that the shape is somewhat determined by the hardware limits of our setup. Also, there is significant ringing that is due to the poor impedance matching of the transistor to the oscilloscope input impedance. The maximum currents and pulse widths varied very little, with averages of 650 ± 40 µA and 570 ± 40 ps.

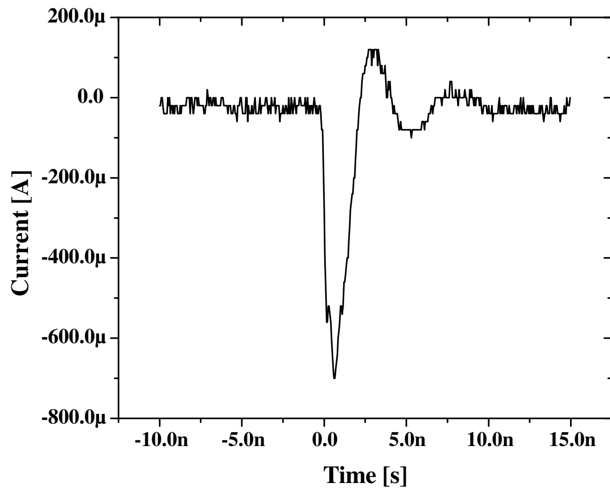

Fig. 10. Typical current transient recorded on the same spot as shown in Fig. 8.

4. Summary

We performed IBIC and TRIBIC experiments on SiGe HBTs manufactured using deep trench isolation technology. We showed that most of the charge collection (up to 80% of the total deposited charged) occurs within the deep trench enclosed region due to carrier drift. We also showed that significant charge induction occurs when ions hit outside the trench, due to carriers diffusing into the depletion layer formed between the subcollector and the substrate. The results of the initial TRIBIC measurements were presented. These measurements need more development to eliminate the ringing on the current signal and increase sensitivity level. An improved TRIBIC measurement would be invaluable for device code validation and calibration.

Acknowledgements

The authors would like to thank to Prof. John D. Cressler and his team students for the preparation and the electronic tests done on the sample.

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Applications of heavy ion microprobe for single event effects analysis

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Available online 20 April 2007

Abstract

The motion of ionizing-radiation-induced rogue charge carriers in a semiconductor can create unwanted voltage and current conditions within a microelectronic circuit. If sufficient unwanted charge or current occurs on a sensitive node, a variety of single event effects (SEEs) can occur with consequences ranging from trivial to catastrophic. This paper describes the application of heavy ion microprobes to assist with calibration and validation of SEE modeling approaches.
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PACS: 61.82.Fk

Keywords: Radiation effects in semiconductors; Focused ion beam

1. Introduction

Ionizing-radiation can have dramatic effects on microelectronic circuit operation [1]. A class of effects, called single event effects (SEEs), is initiated when a single ionizing particle moves through a microelectronic component. The result can be a loss of stored information, erroneous transients at the circuit output, or even catastrophic circuit failure.

The underlying mechanisms for most SEE responses are: (1) ionizing radiation-induced energy deposition within the device, (2) initial electron–hole pair generation, (3) thermalization of charge carriers, (4) transport of thermalized carriers within the semiconductor and (5) the response of the device and circuit to carrier movement and recombination processes. Heavy ion microprobes have been used to support analyses and modeling of some of these mechanisms [2].

Ionization (mechanism 1) can result either from the direct interaction of incident particles with the integrated circuit (called direct or primary ionization) or from ionization induced by scattered particles or reaction products (called indirect ionization). These interactions can be modeled using radiation transport tools like Geant4 (described in more detail later). Conversion of energy deposition into thermalized electron–hole (e–h) pairs (mechanisms 2 and 3) is modeled by assuming that the ion must lose, on average in silicon, 3.6 eV of its energy to generate one e–h pair. Transport of the charge carriers (mechanism 4) and the resulting response of the device and circuit (mechanism 5) is modeled using technology computer-aided design (TCAD) tools [3].

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0168-583X/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.nimb.2007.04.163

In this paper, we discuss some recent applications of the microprobe at Sandia National Laboratories to uncover important charge collection properties of an emitter coupled logic (ECL) circuit based on silicon germanium (SiGe) heterojunction bipolar transistors (HBTs), validation of TCAD simulation of single event upsets (SEUs) in a 0.25 μm CMOS SRAM and calibration of sensitive volume dimensions for analysis of multiple bit upset (MBU) in a 130 nm CMOS SRAM.

2. Charge collection properties of an ECL circuit fabricated using SiGe HBTs

SiGe based technology is widely recognized for its potential to impact the high speed microelectronic industry by monolithic incorporation of low power complementary logic with extremely high speed SiGe HBT logic. Accessibility to SiGe through an increasing number of manufacturers adds to the importance of understanding its intrinsic SEE characteristics. IBM is now manufacturing its third generation of their commercial SiGe HBT processes and access is currently available to the first, second and third generation HBT processes (known as 5HP, 7HP and 8HP) through the MOSIS shared mask services. The data presented in this paper were collected on a simple ECL circuit fabricated in the 7HP HBT process (0.20 μm emitter and an f_T of 120 GHz).

Fig. 1(a) shows a diagram of the physical layout of an IBM SiGe HBT and identifies the location of the base, emitter and collector contacts. The transistor is manufactured almost entirely from silicon; the only germanium used is a small fraction of the material confined in the base region. The transistor area is totally contained inside two insulating trenches – a shallow trench (STI) and a deep trench (DT).

Previous investigations have examined the SEE response of 5HP and 7HP HBT circuits through both circuit testing [4,5] and modeling [6]. Charge collection modeling and measurement [7] studies in the 5HP process have also been conducted. The basis for most of the modeling and analysis in all of these papers has been ion beam induced charge collection (IBICC) measurements with emitter, base and collector contacts grounded and the substrate biased between −3 and −5.2 V. To date, no measurements have been reported that show charge collection properties of a SiGe HBT biased and loaded, as it would be in an active circuit.

The text that follows is a description of our use of Sandia National Laboratories' IBICC facility to interrogate the amount of charge collected by each terminal of a single SiGe HBT transistor that was configured as the "off" leg of an ECL differential pair, as shown in Fig. 1(b).

The target transistor was a $0.20 \times 1.14\ \mu m^2$ HBT. The surface area of the silicon volume contained within the DT is $2.12 \times 2.88\ \mu m^2$, called the active area. A physical analysis of the overburden was done using SEM images taken after irradiation. There was approximately 13 μm of dielectric and metallization (nearly 12 μm of this was dielectric) and 4 μm of polyimide.

A four probe IBICC measurement was used to simultaneously measure the charge induced on the collector, emitter, base and substrate terminals due to ion strikes occurring in and around the transistor area. The flux was set sufficiently low to ensure that no more than one ion was incident on the die at each step. The IBICC measurements were made using 36 MeV ^{16}O ions that have a range of 25.5 μm in silicon. For all tests, the ion beam "spot" size was approximately $1.6 \times 1\ \mu m^2$. This spot was stepped through a 1600 μm^2 area that contained the transistor with a step size of about 0.1 μm. The data cube is built up by thousands of scans and consists of the location (x, y coordinate) of the ion "spot" and the charge collected by each probe for each ion strike.

The data plotted in Fig. 2 show a 1 μm slice through the data cube in the y-direction. It shows the charge collected on the collector and the base as a function of position. The data are collapsed on a y-plane and were selected to contain events inside the DT. These data were also selected to be representative of events that traverse a cross-section through the device like that shown in Fig. 1(a).

Fig. 1. (a) Cross-section of SiGe HBT. (b) ECL circuit used for microbeam irradiation of target HBT.

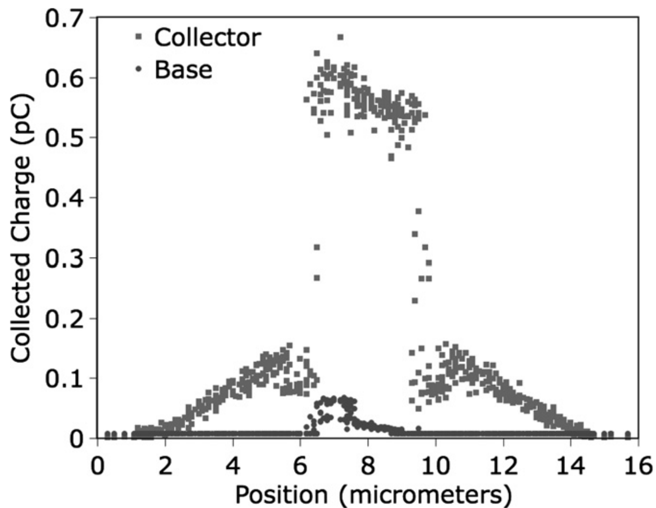

Fig. 2. Charge collection by the collector and base of the target HBT for various microbeam spot locations.

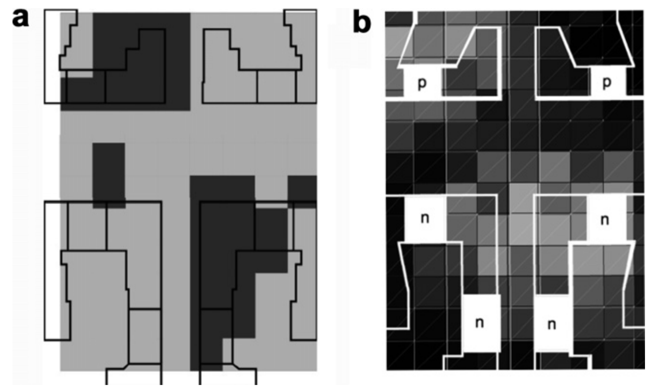

Fig. 3. (a) TCAD simulation results showing the areas (in dark gray) that produce an SEU for ion LET = 6 MeV cm^2/mg. (b) Measured average SEU results from microbeam testing showing the areas (in light gray) that produce an SEU for 36 MeV oxygen ion.

The charge collection on the collector is significantly higher than that on the base and the physical area for collector charge collection is much large than that for the base. Given the overburden describe above, approximately 12 MeV will be deposited in the silicon, or 0.53 pC of charge will be liberated. Note that this is near the maximum value collected by the collector. These data are very similar to those published on single HBTs with fixed bias on each contact and represent a validation of the analysis and modeling in several papers [4–7, and references within].

3. Validation of TCAD simulations of single event upsets (SEUs) in 0.25 μm CMOS

Detailed 3D mixed-level TCAD simulations were performed on one cell of a commercial 4 Mbit SRAM. Most of the memory cell transistors were modeled in a single TCAD description, i.e. a large fraction of the active semiconductor was built in TCAD. The TCAD model was developed via calibration of electrical characteristics of 2D and 3D discrete transistor models to known device characteristics, e.g. I_d–V_g data. To ease the burden of device simulation, the local interconnects and large portions of polysilicon were replaced with SPICE components. Device cross-section and doping profile information were provided by the vendor and SEM analysis.

Over 176 TCAD simulations were performed. The purpose of the TCAD simulations was to understand the topology of the SRAM cell's SEU sensitive area to 36 MeV ^{16}O ions normally-incident to the cell surface. The SEU simulations were performed by rastering a particle strike over the entire surface of the cell. The steps were 0.25 μm in both the *x* and *y* dimensions. For each *x*–*y* pair, a TCAD simulation was done to determine if the ionizing-radiation-induced a SEU. Fig. 3(a) shows SEU results for a stopping power of 6 MeV-cm^2/mg (the radiation effects on microelectronics community typically refers to stopping power as linear energy transfer or LET). The dark gray areas define the *x*–*y* position for events that caused errors, while events in the light gray areas did not cause a SEU. The lower right region shows the drain and gate of the off NMOS device to be a portion of the sensitive area, while the top left region gives the contribution to the sensitive area of the drain and gate of the off PMOS device. These results are consistent with the classical understanding of SEUs in this type of SRAM.

Heavy ion induced SEU data were taken at SNLs microprobe facility. The probe was focused to be incident within a 1.6×1 μm^2 area. The accelerator was tuned to deliver 36 MeV ^{16}O ions on the target. The incident LET was approximately 5.2 MeV-cm^2/mg in silicon. We approximate the LET at the sensitive regions to be 6 MeV-cm^2/mg. The data are presented in Fig. 3(b). Also shown are the n- and p-regions of the cell. Note that the data show similar characteristics to those given by the TCAD simulations. This comparison provides experimental verification of the TCAD simulations, allowing for higher confidence in simulations done with other ion species.

4. Calibration of SEU sensitive volume dimensions for analysis of MBUs in a 130 nm CMOS SRAM

SNL's IBICC facility was used to help define the geometric volume used as input to a Monte Carlo radiation transport code that predicts energy deposition in multiple volumes due to an ensemble of single radiation events (more on the code later). A single transistor from IBM's 8RF 130 nm process was irradiated using the 36 MeV ^{16}O focused ion beam much like that described in the Section 2. The gate length was 1.6 μm and the gate width was 10 μm. The structures had less than 1 μm of overburden above the active region.

Fig. 4 gives the induced charge collection at the drain terminal for normally-incident ^{16}O ions for various ion spot locations. As before, a 1 μm slice of the data was

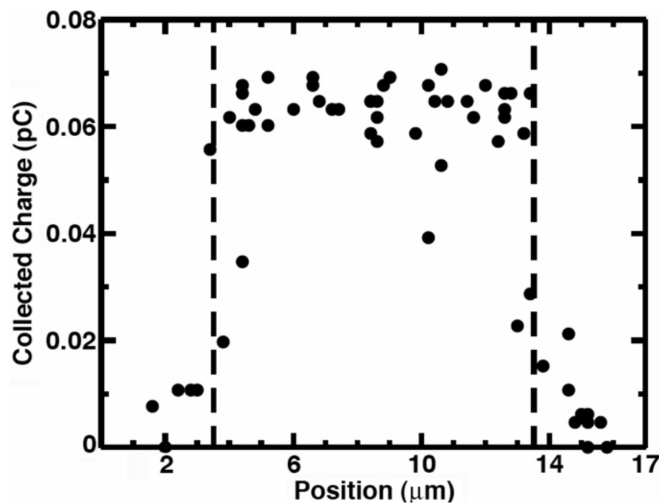

Fig. 4. Charge collected by drain of the target NFET for various microbeam spot locations.

collapsed on this plane. The data were selected to represent a cut line through the drain region parallel to the gate width. The dotted lines enclose the drain diffusion region of the device. Charge collection in this region peaks near 0.065 pC and quickly falls to zero outside the drain diffusion. The linear energy transfer (LET) of 36 MeV ^{16}O ion is near 5.2 MeV-cm^2/mg in silicon. Using the density of silicon and the fact that one e–h pair will be created when the ion loses 3.6 eV to ionization allows for conversion of this LET to a charge generation per micrometer rate, i.e. 0.052 pC/μm. From the maximum collected charge and the charge generation rate, we can determine the thickness of the collection volume region by determining the ion path length required to deposit an amount of energy equivalent to a charge generation of 0.065 pC, e.g. 0.065 pC/0.052 pC/μm = 1.2 μm. Of course this method assumes that the ion stopping power is constant over a range longer than the path length of interest, which is true for a 36 MeV ^{16}O ions moving through 1.2 μm of silicon. This result is consistent with TCAD device simulations given in [8].

Given this collection volume depth and the physical area of the drain diffusion, we defined a set of sensitive volumes that represent an array of memory cells in an SRAM [9]. The details of the cell size and layout were developed from proprietary information provided by IBM. We used this as input to our virtual irradiator call MRED (Monte Carlo radiative energy deposition, developed by researchers at Vanderbilt University). MRED is a Geant4 application. Geant4 is a library of c++ routines assembled by an international collaboration for describing radiation interactions with matter. MRED was structured so that all physics relevant for this radiation effects application was available at run time. In [9], we used MRED to determine the probability of proton-induced MBUs in an SRAM designed in the 130 nm IBM 8RF process. The simulations predict a single event response that has a strong dependence on the angle of proton incidence.

5. Conclusion

We demonstrate several uses for SNL's microprobe facility to support modeling efforts to assess SEEs in modern technologies. The ion microprobe has been shown to be a valuable tool for model calibration and validation. As microelectronic technologies advance, the current microprobe facilities must change to allow for these types of assessments to continue. One major limitation is the ion energy that is available at current facilities. Microelectronic fabrication processes are moving towards much thicker overburdens, e.g. nine metal layers that are over 16 μm thick. Overlying metallization and dielectric stacks of this thickness severely limit the penetration range of ions into the active silicon, reducing the signal induced on the circuit nodes in question, making accurate measurements difficult or impossible.

Acknowledgement

Sandia is a multi-program Laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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Substrate Engineering Concepts to Mitigate Charge Collection in Deep Trench Isolation Technologies

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***Abstract*—Delayed charge collection from ionizing events outside the deep trench can increase the SEU cross section in deep trench isolation technologies. Microbeam test data and device simulations demonstrate how this adverse effect can be mitigated through substrate engineering techniques. The addition of a heavily doped p-type charge-blocking buried layer in the substrate can reduce the delayed charge collection from events that occur outside the deep trench isolation by almost an order of magnitude, implying an approximately comparable reduction in the SEU cross section.**

***Index Terms*—Deep trench isolation, Ion Beam Induced Charge Collection (IBICC), silicon germanium, Single Event Upset (SEU), substrate engineering.**

I. Introduction

A. Overview

SOME device technologies that typically make use of Deep Trench Isolation (DTI), such as Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs), have Single Event Upset (SEU) cross sections exceeding the active area of the device. Recent work [1] reveals that shift registers composed of a particular type of SiGe HBT have an SEU cross section approximately ten times the active area of the device, which is defined by the area enclosed by the DTI. This work shows that the SEU cross section enhancement at highly ionizing energies is the result of delayed (long time) charge collection from regions of charge generation many micrometers away from the DTI. The range and magnitude of charge collection is primarily governed by the doping concentration and physical structure of the substrate.

Heavy ion microbeam irradiation reveals the effects of substrate engineering in SiGe HBTs, specifically how it affects delayed charge collection. Based on the microbeam charge collection data, a substrate engineering concept in the form of a p-type charge-blocking buried layer at the bottom of the DTI is proposed. Three dimensional Technology Computer-Aided Design (TCAD) simulations reveal that the buried layer concept reduces charge collection by more than 70% for lightly ionizing events that occur outside the DTI and by more than a factor of ten for highly ionizing events.

B. Driving Factors

There have been in excess of thirty publications since 2000 covering radiation effects in SiGe devices and circuits—most of them appearing in *IEEE Transactions on Nuclear Science*. SiGe HBTs have been shown to be robust to Total Ionizing Dose (TID) effects at absorbed doses well above 6 Mrad(Si) [2]. This TID tolerance has made SiGe HBT technology an attractive tool for space applications envisioned by agencies such as NASA. SiGe HBTs have been incorporated in some missions that are already flying.

Despite their favorable TID response, SiGe HBTs have an extremely low threshold and high saturated cross section for SEU in most circuit topologies due to the way that they collect charge from the substrate. Linear Energy Transfer (LET) thresholds for SEU less than or equal to 1.2 MeV$\cdot$ cm^2/mg have been reported [3]. Furthermore, the SEU cross section can increase by more than an order of magnitude when operating at high data rates (e.g., greater than 6 Gbits/s).

The experimental work of Reed and Marshall [1], [3]–[5] over the past six years has sought to uncover the mechanisms responsible for the poor SEU tolerance of these devices so that

Manuscript received July 14, 2006. This work was supported by the NASA Electronic Parts and Packaging Program and the Defense Threat Reduction Agency Radiation Hardened Microelectronics Program under IACRO06-4012I to NASA, the NASA SiGe ETDP project, BAE Systems, Sandia National Laboratories, and the Georgia Electronic Design Center at at The Georgia Institute of Technology. Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration, under Contract DE-AC04-94AL85000.

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Digital Object Identifier 10.1109/TNS.2006.885798

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actions can be taken at the device and circuit levels to correct single-event effects.

C. Historical Context

Using substrate engineering, such as buried layers of increased doping concentration, in heterostructure semiconductor devices, like SiGe HBTs, to control radiation-induced charge collection has been proposed for other device technologies. For example, Umemoto proposed using p-type buried layers to reduce charge collection in Gallium-Arsenide (GaAs) devices [6], [7].

One of the most successful implementations of substrate engineering to radiation-harden a semiconductor device was developed jointly by Marshall, McMorrow, and Weatherford. They employed a buffer layer of Low-Temperature grown GaAs (LT GaAs) in a GaAs Heterostructure Insulated Gate Field Effect Transistor (HIGFET) [8], [9]. The buffer layer provided a region of very high recombination, thus shortening the minority carrier lifetime and eliminating ion-induced charge collection. This is a very different charge collection suppression mechanism than that produced by the buried p-type layer, which slows charge transport with an electric field as opposed to eliminating charge through recombination processes.

Substrate engineering for radiation-induced charge suppression, of the kind described in this work, has not yet been physically implemented in SiGe HBTs. However, Niu *et al.* [10] designed and simulated an effective charge collection suppression technique by incorporating an n^+ back junction at the level of the bottom of the deep trench in a third-generation, 200 GHz SiGe HBT. The buried p-type layer described in this work can be created by standard ion-implantation and epitaxial growth techniques before device fabrication.

As a point of comparison, the proposed buried p-type layer is analogous to well engineering in present commercial CMOS processes, with the exception that the retrograde well is approximately 5 μm below the active device. Buried layers in current CMOS processes usually abut the active device well, making them 1 to 3 μm below the surface of the device, whereas the proposed buried layer in SiGe HBTs is approximately 8 μm below the device surface. This results in minimal interference with device operation while still providing radiation-induced charge suppression.

II. Ion Microprobe Testing of SiGe HBTs

A. Experimental Setup and Methods

All of the devices in this study were tested at Sandia National Laboratories' (SNL) Ion Beam Induced Charge Collection (IBICC) facility [3], [11]. The test methodology and data reduction follow the procedures described in [3]. All of the SiGe HBTs underwent four-probe IBICC so that charge collection on all the terminals (emitter, base, collector, and substrate) could be monitored simultaneously. The emitter, base, and collector were held at 0 V while the substrate was biased to -5 V via the charge collection amplifier biasing. These charge collection bias conditions were intended to replicate the "off-state" of the device-under-test (DUT), shown to be the most sensitive state in previous work [12], [13]. This charge collection setup had fidelity to those conditions.

All four electrodes were connected to amplifier chains composed of Ortec 142A charge sensitive preamplifiers and Ortec 671 spectroscopy amplifiers. Additionally, the signals were fed into individual single channel analyzers and then connected to a four-input OR logic unit. The output of the OR logic unit was connected to the gates of the analog-to-digital converters for the X-Y scan generator's output. A signal on any one of the four channels can trigger an event, which causes the position of the ion and charge collected on each device terminal to be recorded. Further information on radiation effects microscopy, including ion beam induced charge methods can be found in [11], [14]–[16] and references therein.

As in [3], experiments were conducted using normally-incident 36 MeV ^{16}O ions with approximately a 1 μm spot size. Due to the finite spot size and low beam current, approximately 600 ions/s, there is a positional uncertainty of $\pm$ 1μm in the x-and y-directions. The ions have a range of 25.5 μm in silicon, a surface incident LET of 5.2 MeV$\cdot$ cm^2/mg, and a Bragg peak of approximately 7.5 MeV$\cdot$ cm^2/mg. The penetration depth and LET were determined using **M**onte Carlo **R**adiative Energy **D**eposition (MRED) [17]–[20] calculations.

Due to the fact that SNL's tandem Van de Graaff can only provide heavy ions with kinetic energies less than 50 MeV, all six SiGe HBTs in the study underwent chemical etching to remove a significant portion of the overlying passivation and metallization layers so that the ions could penetrate into the active silicon in excess of 12 μm. This is an adequate depth to study all relevant charge collection mechanisms and effects. This differs from the physical situation in which very penetrating cosmic rays would deposit energy much more uniformly and deep into the substrate. However, the modeling activities to ascertain the dominant mechanism and device effects were chosen to simulate the test conditions.

IBICC data is reported for six devices from three different vendors: IBM Corporation [21], [22], Jazz Semiconductor [23], and National Semiconductor [24], with relevant parameters detailed in Table I. The abbreviations used in Table I will be used throughout the rest of the manuscript. All devices were subjected to the same ionizing radiation under identical bias conditions. The Jazz HRS and SOI SiGe HBT devices, as well as the NSC epi SiGe HBT device, supplied by BAE Systems, were from experimental hardware lots and are not standard commercial product offerings. All devices are $npnn^+$ with p-type substrates. The DTI in all six devices is approximately the same, being 1 μm wide, 8–9 μm deep, with 4–5 μm between the trench walls, as shown in Fig. 1. The data for the IBM 5HP devices were taken before the others, so the DUTs were not etched with the other technology lots. Consequently, they had almost two additional micrometers of overlying material, which cut down on the amount of charge that was generated in the substrate by about 15%. This was confirmed with SEM images of post-etched device cross sections.

B. IBICC Results

The data sets shown in Fig. 2(a)–(c) displays integrated charge collection on the collector terminal, since ion-induced

TABLE I
SiGe HBT Device List for IBICC Testing

Device Name (Abbreviation)	**Emitter Area** A_E (μm)	**Substrate Resistivity** ($\Omega \cdot$ cm)
IBM 5HP (IBM 5HP)	0.5 × 10.0	8-10
Jazz SiGe-120 Bulk (Jazz bulk)	0.2 × 10.16	8-10
Jazz SiGe-120 SOI† (Jazz SOI)	0.2 × 10.16	8-10
Jazz SiGe-120 High Resistivity Substrate† (Jazz HRS)	0.2 × 10.16	1500
National SiGe-8iED Bulk (NSC bulk)	0.4 × 20.0	8-10
National SiGe-8iED epi† (NSC epi)	0.4 × 20.0	0.009

† Not standard commercial product offerings. Experimental hardware lots.

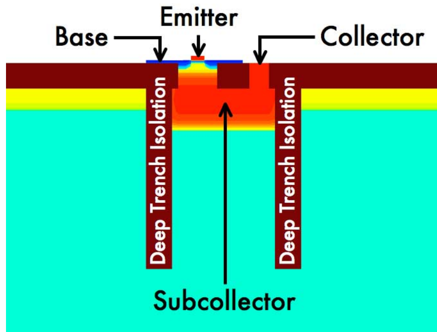


Fig. 1. TCAD cross section of the IBM 5HP SiGe HBT device. The two most important features pertaining to charge collection, the deep trench isolation and the n+ subcollector, are shown. The standard SiGe HBT device terminals are also labeled. For minimum geometry devices, the area enclosed by the deep trench is nearly rectangular and is approximately equal to 10 μm^2. However, for devices with a large emitter length—like some of the test structures listed in Table I, the area enclosed by the deep trench can approach 50 μm^2. The area of the subcollector junction is equal to the area enclosed by the DTI.

collector current is the major cause of SEU in most standard SiGe HBT circuits [3]. All subsequent plots of charge collection will be for the collector terminal. While the data plots here focus on the collector terminal, the majority of the current sensed on the collector terminal also appears on the substrate terminal. The currents have opposite polarities since one current is traveling into the device and one is traveling out of the device.

The plots in the aforementioned figures, Fig. 2(a)–(c), are "slices" through what is actually three dimensional data, though the third dimension has been collapsed against the xy-plane. The data clearly show the structure of the devices. The peak charge collection occurs for strikes within the DTI and the tails represent charge collection from events occurring outside the DTI. These two regions of data reveal separate charge collection characteristics, which are position dependent. Within the DTI, drift transport dominates due to the extension of the potential into the substrate from the bottom of the subcollector (collector-substrate) depletion region [25] (the subcollector is shown in Fig. 1). Normally-incident 36 MeV oxygen ions deposit about 26 MeV in the substrate of a typical etched device, which generates roughly 1.1 pC of charge. The noted exception in Section II-A for the IBM 5HP devices applies here, since the presence of the thick overlayers decreased the range of the ion in the substrate and thus the total charge generated.

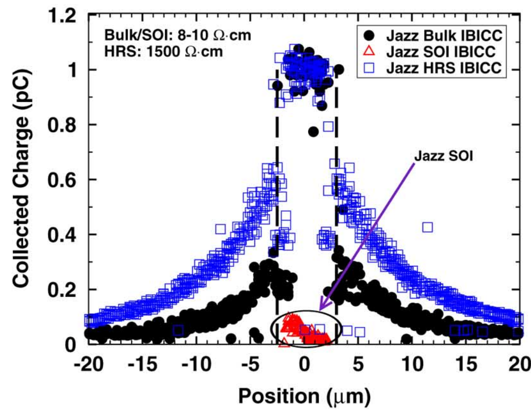
The peak charge collection in Fig. 2(a)–(c) occurs within the DTI for ions that cross the reverse-biased subcollector junction. The microbeam data show this peak to be about 1 pC, a charge collection efficiency of approximately 90%. Outside the DTI, there is no pre-existing electric field to move the charges once they separate from the ion track, so the charge collection is slower and less efficient since the electrons must diffuse to the subcollector junction to induce current on the collector terminal. The tails to either side of the DTI seen in all the figures are representative of this collection mechanism. They peak at about 200 fC and fall off to less than 50 fC in most cases. This amount of charge is sufficient to cause upset in typical unhardened SiGe HBT circuits.

The charge collection results described above are further confirmed by the cross-vendor comparison shown in Fig. 3. The only characteristic these three devices have in common is deep trench isolation and substrate resistivity; their operational requirements and performance characteristics are quite different. Nevertheless, all of them exhibit the same charge collection profiles, taking into account the considerations for the IBM 5HP devices. This suggests that the physics of charge collection for the three device types is the same.

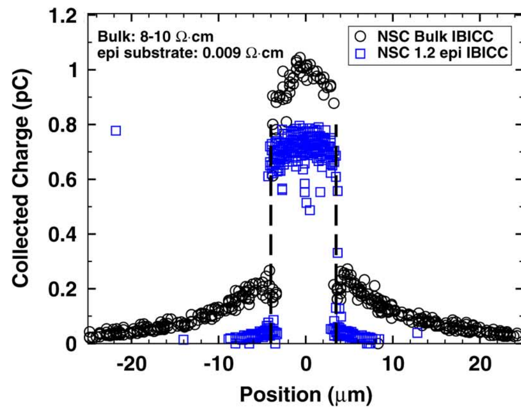
III. Charge Collection Modeling and Mitigation Strategies

A. TCAD Device Calibration

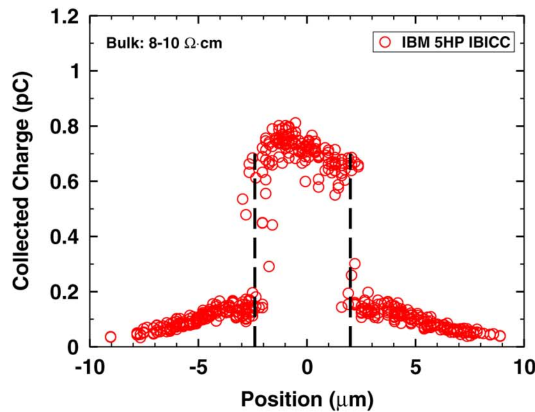
The IBM 5HP device was chosen for modeling since it represents a broad selection of SiGe HBT technologies and because of access to calibrated TCAD models. The device model used in this work is based on the structure described in [26]. All of the TCAD simulations were three dimensional and executed with DESSIS v10.0.6 [27]. IBICC microbeam data, shown in Fig. 2(c), was used in order to both extend the work presented in [26] and to calibrate charge collection simulations for normally-incident 36 MeV ^{16}O ions, identical to the ones used in the microbeam experiments. The LET profile for the simulated oxygen ions was generated using MRED, which is similar to the profile used in [26]. Using an iterative process, the silicon model parameters for bulk electron lifetime were modified until reasonable agreement with experimental data was achieved. The calibrated charge collection simulation points are shown in Fig. 4 as "Calibrated TCAD" points.



(a)



(b)



(c)

Fig. 2. IBICC data for the six SiGe HBT DUTs. The data sets shown display charge collection on the collector terminal. *The Jazz HRS, Jazz SOI, and NSC epi SiGe HBT devices are experimental hardware lots and are not standard commercial product offerings*. In the above three figures, the deep trench isolation boundary is indicated approximately by vertical dashed lines. The substrate resistivities are listed on the individual charts. The absence of a symbol occurring outside the DTI indicates no events were triggered there.

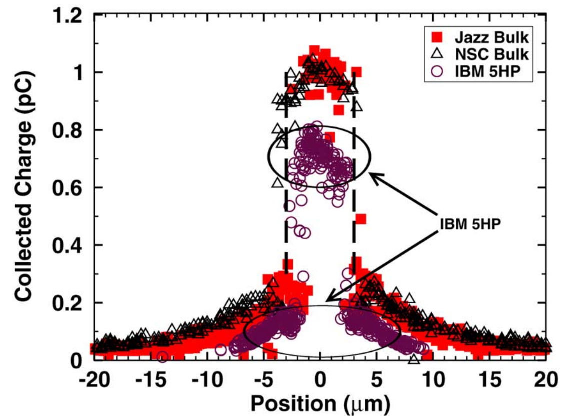


Fig. 3. IBICC data cross-vendor comparison of SiGe HBT devices with similar substrate constructions and doping levels. All devices shown—Jazz, NSC and IBM—have substrate resistivities between 8 and 10 Ω·cm.

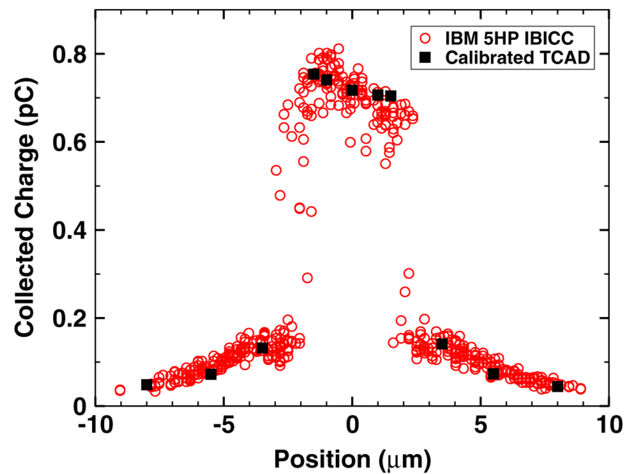


Fig. 4. Calibrated TCAD charge collection simulation points for the IBM 5HP device. The calibration was achieved by iteratively adjusting the electron lifetime in the bulk silicon. The simulation results are overlaid on the IBM 5HP IBICC data shown in Fig. 2(c).

B. Charge Collection Mitigation

Circuits fabricated using SiGe HBTs, while robust against total ionizing dose [2], [24], [28] usually suffer from low SEU thresholds and large saturated cross [1], [3], [5]. A pseudo-random number sequence generator fabricated in the IBM 7HP SiGe HBT process, described in [3], has a $Q_{\rm crit}$ of approximately 100 fC, which was derived from Fig. 3 in [3], assuming a maximum collection depth of 15 μm. Broadbeam heavy ion data [1] for the IBM 5AM SiGe HBT suggest that the sensitive area for a single sensitive transistor is almost an order of magnitude larger than the active region of the device. Very often, the upset cross section for highly ionizing incident particles does not saturate, which is indicative of delayed charge collection from charge generated outside of the DTI. This class of charge collection is also responsible for the burst error modes reported in [1] and [5].

Present simulation and experimental results suggest that delayed charge collection from ionizing events outside the DTI can be mitigated—if not eliminated—by introducing a charge-blocking buried layer of heavily doped p-type silicon at the level of the bottom of the DTI. A cross section of the IBM 5HP device with the addition of the buried layer is shown in Fig. 5. The p-type layer shown at the level of the bottom of the DTI is approximately 2 μm thick and has a peak boron concentration of 1×10^{17} cm^{-3}.

First generation SiGe HBT devices with this buried layer could be manufactured with little to no degradation in device performance since the retrograde well is more than 4 μm below

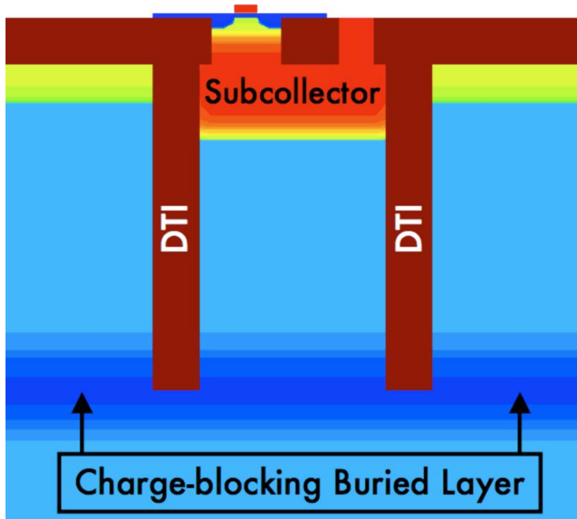


Fig. 5. Cross section of the buried layer concept for the IBM 5HP device. The buried layer is located at the level of the bottom of the deep trench isolation. It is 2 μm thick, p-type and peaks at 1×10^{17} cm^{-3}.

the subcollector junction. Under those circumstances, the collector capacitance is not modified. Compatibility with the companion CMOS device in the technology was not considered explicitly.

To evaluate the effectiveness of the proposed buried layer, another series of DESSIS simulations was conducted using the same oxygen LET profile and ion strike location as the original charge collection calibration simulations discussed in Section III-A. Though a buried p-type layer with a doping concentration of 1×10^{17} cm^{-3} is highlighted, two other sets of simulations were conducted—one with a buried layer doping concentration of 1×10^{16} cm^{-3} and one with 1×10^{18} cm^{-3}. A concentration of 1×10^{17} cm^{-3} yielded the most efficient reduction in charge collection based on the concentration of dopant in the buried layer.

As evidenced by the simulation points shown in Fig. 6(a), the buried layer reduces charge collection from events outside the DTI to the level measured in a SiGe HBT with a much higher substrate doping concentration, *viz.*, the NSC epi, which has a p-type substrate resistivity of approximately 0.009 $\Omega\cdot$ cm. The data for the NSC epi device are shown in Fig. 2(b). Charge integration curves for two sets of strikes in the IBM 5HP device with the 1×10^{17} cm^{-3} p-type buried layer are shown in Fig. 6(b).

The buried layer does not affect the charge collection magnitude for ionizing events that occur within the active region between the DTI walls, but it does result in a factor of two decrease in the time to saturation. Planned future work involving Time-Resolved Ion Beam Induced Charge Collection (TRIBICC) [29], [30] will provide more information about charge collection times and current pulse shapes for events both inside and outside the DTI.

The electric field that results from the buried layer is approximately 0.8 kV$\cdot$ cm^{-1}, which is not high; however, it is strong enough to influence the transport of the electrons. The level of charge collection for events that occur outside the DTI of the device with the buried layer is less than 50 fC, which is less than the inferred Q_{crit} of 100 fC based on data in [3]. This means that

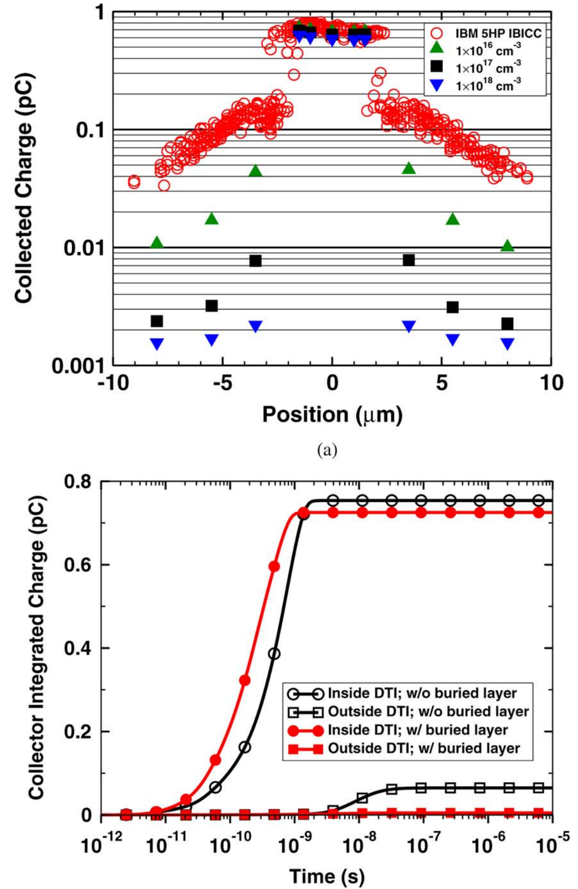


Fig. 6. Fig. 6(a) shows DESSIS charge collection simulations of the IBM 5HP device with three different versions of the p-type charge-blocking buried layer: 1×10^{16} cm^{-3}, 1×10^{17} cm^{-3} and 1×10^{18} cm^{-3}. The simulations were conducted with the same ion LET profiles used in Fig. 4 and are overlaid on the IBM 5HP IBICC data displayed in Fig. 2(c). Fig. 6(b) shows current integration over time (charge) for the collector terminal in the 5HP with and without a 1×10^{17} cm^{-3} p-type buried layer. The data markers shown are sparse (every 15 points) to aid visualization.

the SEU sensitivity of the IBM 5HP device could be reduced to a cross section roughly the size of the active device enclosed within the DTI, which would reduce the SEU cross section for highly ionizing particles impinging on the device, almost independently of any hardness-by-design techniques invoked in the circuit layout [4], [13].

It is important to note that while the proposed charge-blocking buried layer reduces the SEU cross section, it does not increase the upset threshold of the device. The threshold remains unchanged because the device will still collect a large portion of charge from the substrate if substrate potential modification is activated by an appropriate ion strike. This topic is covered in Section IV-A.

C. Simulated Heavy Ion Strike

Two additional heavy ion simulations were executed with a constant LET of 53 MeV$\cdot$ cm^2/mg, which is equivalent to a 1934 MeV ^{129}Xe ion, the most highly ionizing beam used for testing in [1]. One simulation was executed without the 1×10^{17} cm^{-3} buried layer and one was executed with the buried

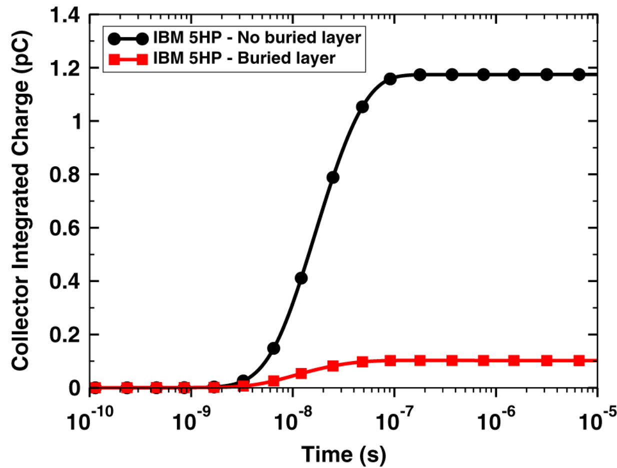


Fig. 7. Simulated current integration over time for a ^{129}Xe event 4 μm outside of the DTI in the IBM 5HP device. Results from two simulations are shown—one with the 1×10^{17} cm^{-3} charge-blocking buried layer and one without. The presence of the buried layer reduces charge collection by approximately 91%. The data markers shown are sparse (every 10 points) to aid visualization.

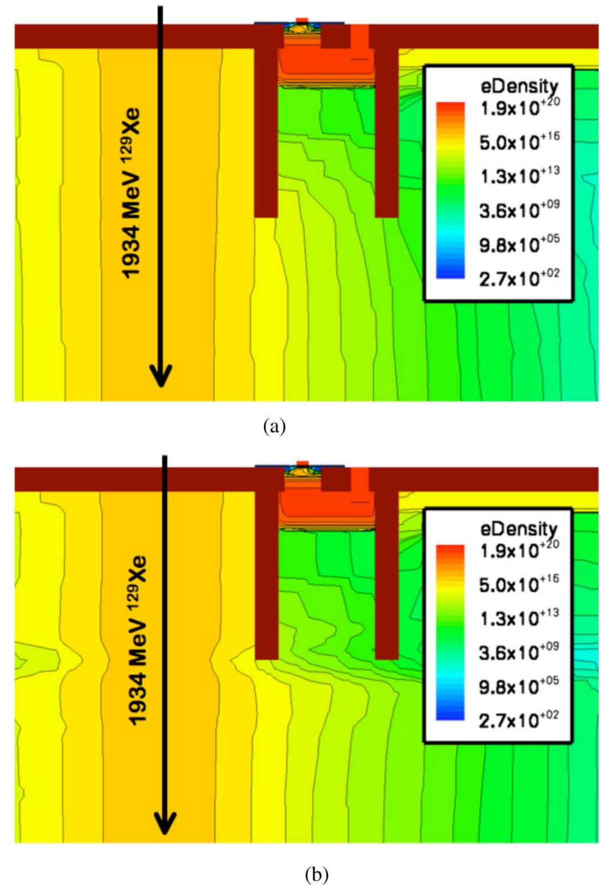


Fig. 8. Electron density contour cross sections for the 1934 MeV ^{129}Xe strikes in the IBM 5HP three dimensional TCAD description—with and without the 1×10^{17} cm^{-3} buried layer. The charge-blocking buried layer impedes electron transport into the DTI and towards the subcollector junction, which prevents the integration of current on the collector terminal. These time snapshots were taken at 5 ns. The ion event occurred at 1×10^{-11} s.

layer. These simulations were designed to provide clear evidence of the effectiveness of the charge-blocking buried layer under conditions of an impinging cosmic ray with a large linear energy transfer depositing energy deep in the substrate of the device.

The simulations were carried out in the calibrated IBM 5HP three dimensional TCAD description described earlier. The strike originated 4 μm outside the DTI and penetrated the entire device, generating 15.9 pC of charge. Fig. 7 shows the time profiles for current integration in both devices—with and without the charge-blocking buried layer. The charge-blocking buried layer reduces the integrated charge on the collector terminal by a factor of 11.5, or approximately 91%. This large reduction in charge collection is due to the electric field created by the buried layer impeding the transport of electrons to the subcollector junction.

Fig. 8(a) and (b) shows the electron density contours in the ^{129}Xe ion simulations. The buried layer reduces the electron density inside the DTI by several orders of magnitude since electron transport into the deep trench is limited by the electric field created at the edges of the p^+ buried layer.

IV. Discussion

A. *Charge Collection in Sige Hbts*

Based on analyses of the microbeam data and three dimensional TCAD device simulations of relevant ion events, the subcollector junction determines the charge collection properties of the device. The depletion region of this junction can be more than 2 μm wide and can drop a potential of 5 V in the case of current-mode logic circuits [1]. In BiCMOS applications, the substrate contact sits at V_{ss}, so the reverse bias of the subcollector junction is not as large, but it still has a significant depletion region. In the case of an ion strike, minority carriers compensate for the ionized acceptors in the subcollector space-charge-region and cause the subcollector equipotential surfaces to push out into the substrate to maintain the potential drop. This process is not unlike the Kirk effect that occurs in the collector region of bipolar transistors under conditions of high-level injection [31]. Hsieh *et al.* [32] and Hu *et al.* [33] laid out the framework for substrate potential modulation in the early 1980s. This phenomenon can result in a higher charge collection efficiency than purely diffusive processes.

Most SiGe HBT devices exhibit highly efficient charge collection because they are constructed on lightly doped substrates with an unobstructed deep trench. Electron transport in a 1×10^{15} cm^{-3} p-type substrate has a diffusion length greater than or equal to 100 μm [34]. This long diffusion length, and accompanying high mobility, permit the electrons produced by ionizing particle interactions to travel long distances, increasing the charge collection efficiency of most SiGe HBTs to levels that dramatically affect the SEU response of the circuits containing them.

While curtailing electron transport has been the major focus of this work, holes also contribute to SEU in SiGe HBTs. If an ion strikes the active region of the device, the area enclosed by the DTI, then charge can be induced on the base terminal,

possibly leading to upset. However, the base-collector junction is very thin and small compared with the subcollector junction—approximately 0.5 μm^2 versus 10 μm^2—which are minimum geometries for a typical first generation SiGe HBT device. Therefore, transients that appear on the base terminal are generally smaller and of shorter duration than events that appear on the collector terminal. Ions that hit outside the DTI will produce a negligible amount of current on the base terminal since the base-collector junction is protected from the substrate by the subcollector junction.

The microbeam data demonstrate that devices that employ measures to impede or stop electron transport to the subcollector junction have much lower charge collection efficiencies. For ion events that occur outside the DTI, the Jazz SOI and NSC epi devices, shown in Fig. 2(a) and (b), collect little or none of the approximately 1.1 pC that was generated in the substrate of the device. Conversely, devices that have lightly doped substrates and nothing to stop the electrons from reaching the subcollector junction can have charge collection efficiencies exceeding 60% for events outside the DTI, as in the case of the Jazz HRS device, shown in Fig. 2(a).

The charge-blocking buried layer was studied using lightly ionizing ^{16}O ions and highly ionizing ^{129}Xe ions. In both cases, the buried layer reduced simulated charge collection on the collector terminal by more than 70%, which suggests the possibility of reducing the SEU cross section for particles with a high linear energy transfer by a significant amount. These characteristics also bode well for mitigating charge collection due to indirect ionization from proton reactions occurring in the substrate.

V. Conclusion

Substrate engineering is a valuable tool for controlling delayed charge collection from events that occur outside the deep trench in DTI technologies, like SiGe HBTs. Moderate-to-low substrate doping concentrations permit large numbers of electrons to diffuse hundreds of micrometers, thereby increasing the charge collection efficiency of devices fabricated on these substrates. This effect increases the SEU cross section for highly ionizing particles, perhaps an order of magnitude or more beyond the active region of the device. The devices that showed the least efficient charge collection had the most heavily doped substrate or employed some other means of sheltering the subcollector junction—as in the case of a heavily doped substrate or buried oxide layer.

Based on present simulation results and experimental conclusions from the NSC epi and Jazz SOI experimental IBICC data, a device hardened with the proposed charge-blocking buried layer would be relatively insensitive to heavy ion and proton events that occur in the substrate outside the DTI, without suffering the speed or complexity penalties of other hardening approaches.

Acknowledgment

The authors would like to thank K. LaBel, L. Cohn, R. Van Art, M. El-Diwany, C. Mitchell, R. Lawrence, N. Haddad, M. Watson, D. Frazier, the NASA SiGe ETDP team, BAE Systems, Sandia National Labs, and the SiGe teams at IBM, Jazz, BAE Systems and National Semiconductor for their contributions. The computational portion of this work was performed with the resources of Vanderbilt University's Advanced Computing Center for Research and Education (ACCRE).

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SEU Error Signature Analysis of Gbit/s SiGe Logic Circuits Using a Pulsed Laser Microprobe

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***Abstract*—We present, for the first time, an analysis of the error signatures captured during pulsed laser microprobe testing of high-speed digital SiGe logic circuits. 127-bit shift registers, configured using various circuit level latch hardening schemes and incorporated into the circuit for radiation effects self test serve as the primary test vehicle. Our results indicate significant variations in the observed upset rate as a function of strike location and latch architecture. Error information gathered on the sensitive transistor nodes within the latches and characteristic upset durations agree well with recently reported heavy-ion microprobe data. These results support the growing credibility in using pulsed laser testing as a lower-cost alternative to heavy-ion microprobe analysis of sensitive device and circuit nodes, as well as demonstrate the efficiency of the autonomous detection and error approach for high speed bit-error rate testing. Implications for SEU hardening in SiGe are addressed and circuit-level and device-level Radiation Hardening By Design recommendations are made.**

***Index Terms*—Built-in self-test, circuit level hardening, high-speed bit-error rate testing, pulsed laser testing, silicon-germanium (SiGe), single-event effects (SEU).**

I. Introduction

SILICON-GERMANIUM HBT technology continues to make in-roads into the extreme environment electronics market. Recently reported results on the most aggressively scaled SiGe technologies include excellent low temperature performance [1] and inherent tolerance to multi-Mrad (SiO_2) levels of ionizing dose [2]. These attributes, coupled with its seamless integration with best-of-breed CMOS to form SiGe BiCMOS combine to make SiGe technology a contender for many extreme environment applications [3]. However, despite these attractive attributes, high speed, bulk SiGe digital circuits have traditionally demonstrated significant vulnerability to single-event effects (SEE), as evidenced from recent heavy-ion broad-beam and microprobe experimental results [4]–[7]. Radiation hardening by design (RHBD) is being employed to address SEE in this technology and includes layout variation at the device level [8] as well as novel circuit architectures [9].

In this work, the results of bit-error rate (BER) testing of high-speed SiGe logic circuits using a pulsed laser microprobe technique [10] are presented for the first time. Analysis of the bit error signatures is used to determine the relative sensitivity of circuit building blocks with respect to transistor location, circuit architecture, bias current, equivalent LET, and data rate. The results are shown to be in good agreement with recently reported heavy-ion microprobe testing on similar circuit architectures.

II. Experimental Details

A. Test Vehicle

The circuit for radiation effects self test (CREST) is a novel test platform to conduct high-speed BER testing and efficiently manage error detection and capture [11]. CREST is capable of operation either in standalone mode, or under FPGA assembly control; the latter of which facilitates the initialization, monitoring and resetting of the chip under irradiation. More importantly, the FPGA controlled version of CREST reduces the number of high speed off chip connections required to only one—a single ended clock drive. A more detailed discussion of the experimental setup for FPGA CREST control is given in [11] and for brevity is not repeated here.

CREST was fabricated through the MOSIS foundry service in an IBM 1st-generation (IBM 5 AM) SiGe technology ($f_T = 46$ GHz, $f_{\max} = 65$ GHz) [12]. The design includes 5 shift-registers employing different latch configurations, an on-board pseudo-random number (PRN) generator, clock generation and error reporting circuitry. Each circuit is powered individually and implemented using a current mode logic (CML) circuit topology.

B. Circuit Hardening Techniques

The five latch architectures that are used in the 127-bit SiGe shift registers addressed in this investigation are listed below, along with the relevant transistor size and bias (I_{TAIL}) currents.

Manuscript received August 25, 2006. This work was supported by the Defense Threat Reduction Agency (DTRA) under the Radiation Hardened Microelectronics Program, NASA Goddard Space Flight Center (GSFC) under the NASA Electronic Parts and Packaging (NEPP) Program, the NASA SiGe ETDP project, and the Georgia Electronic Design Center (GEDC) at Georgia Tech.

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Digital Object Identifier 10.1109/TNS.2006.886232

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TABLE I
PULSED LASER MICROPROBE PARAMETERS

Pulse Width	1ps
Wavelength	590nm (2.1eV)
Repetition Rate	1kHz, 10Hz
Spot Size	1µm
1/e Penetration Depth	1.8µm
Data Rate	50 Mbit/s – 6.5 Gbit/s
Laser Pulse Energy (PE)	0 pJ– 10 pJ

i) LP-M/S: low power master/slave (0.5 μm^2, 0.6 mA).
ii) HP-M/S: high-power master/slave (0.62 μm^2, 1.5 mA).
iii) DI: dual interleaved (0.62 μm^2, 3 mA) [9].
iv) NAND: cross-coupled NAND (0.25 μm^2, 0.6 mA).
v) CSH: current shared hardening (0.25 μm^2, 1.5 mA) [13].

A full description of the latch architectures and their circuit-level SEU tolerance was presented in [14], along with quasi-3D MEDICI device simulation and Spectre-based circuit level simulation that predicted a more robust SEU tolerance for the NAND architecture when compared to LP-M/S and CSH. The increased vulnerability in the latter two was attributed to transistor level cross-coupling. An improved SEU response was also predicted for the DI architecture, (over that of LP-M/S and CSH) with a much lower power penalty than the NAND architecture, and was again attributed to limited decoupling between the pass and storage cells.

The first heavy-ion experimental results comparing the CSH and LP-M/S in the IBM 5 AM SiGe technology showed no significant reduction in SEE sensitivity [4]. More recently however, a study also reported in this issue has yielded a much improved response for the DI architecture, implemented in a 3rd-generation technology (IBM 8HP) [15] utilizing triple mode redundancy (TMR) and voting-at-end (VAE) schemes.

C. Pulsed Laser Testing

The details of the NRL pulsed laser testing facility has been previously described in the literature [10], [16], and are summarized in Table I. A top-side illumination technique is employed, with the laser spot positioned in the x-y plane with 0.1 μm resolution. In order to access the sensitive device regions within key circuit blocks, the 1 μm laser spot must target openings in the top metal layers of the circuits.

A comparison between pulsed laser and heavy-ion microprobe data ideally requires the definition of an equivalent laser LET. A theoretical expression for the equivalent laser LET, based on the closed integral of the spatially and temporally distributed laser generation rate across a classical RPP volume [17], has been introduced [18], and an empirical relationship between the incident laser pulse energy (PE) and the heavy-ion LET that has proven valid for many circuit types has been established [10], [19]. Although it is acknowledged that metallization layers, and variations in carrier distributions, complicate the calculation of an effective LET [19], an increasing number of authors have reported good empirical correlations between the heavy-ion and pulsed-laser thresholds as reported in [10] and references therein.

In this work, the energy deposition in the material is presented in terms of the incident laser PE, which is corrected for reflection from the silicon surface [10]. This quantity can be expressed in terms of an effective LET value using the empirical correlation factor (1 pJ corresponds to an effective LET of 3 MeV·cm^2/mg) deduced previously [10], [19]. This correlation has been established for a range of technologies, but is not universally applicable. However, it should be noted that the laser-induced SEU threshold determined in the present study (0.7 pJ $\equiv$ 2.1 MeV·cm^2/mg) is in excellent agreement with the heavy-ion SEU threshold of 3 MeV·cm^2/mg reported in [11].

Once a sensitive region is determined in the x-y plane, the laser PE is minimized to determine the upset threshold (defined as the lowest laser PE at which single-bit errors are detected). This process usually involves iterative fine adjustments of the x-y position and the laser PE. The laser PE is then increased, by up to a factor of 3 to represent events with a larger energy deposition (LET).

III. CAPTURE AND ANALYSIS OF ERROR SIGNATURES

Signal generation was provided via an on-board PRN which generated a unique $2^7 - 1$ bit pattern. A commercial 12.5 Gbit/s Anritsu MP1764A BERT analyzer was used for data capture. Additional equipment supplied and monitored device power dissipation, provided diagnostics (via an oscilloscope), conditioned the signals (amplifier, balun, 4 dB splitters, delay line, bias-Ts, etc.) and provided the clock signal.

The on-chip PRN generator is the input to a 127-bit long shift register, the output of which is always synchronized with the input during error free operation. The input and output bit streams are XOR compared, and any differences result in the capture of the entire bit stream as an error event. Correct bits are represented as a "1" or "0." Bit errors are represented as a "+" ($0 \rightarrow 1$ transition), or a "$-$" ($1 \rightarrow 0$ transition). Each error event was logged in a data file along with the corresponding laser repetition rate, laser power and data rate.

Each data file was post-processed using a C++ application to generate histograms of the number of bits-in-error (BIE), error

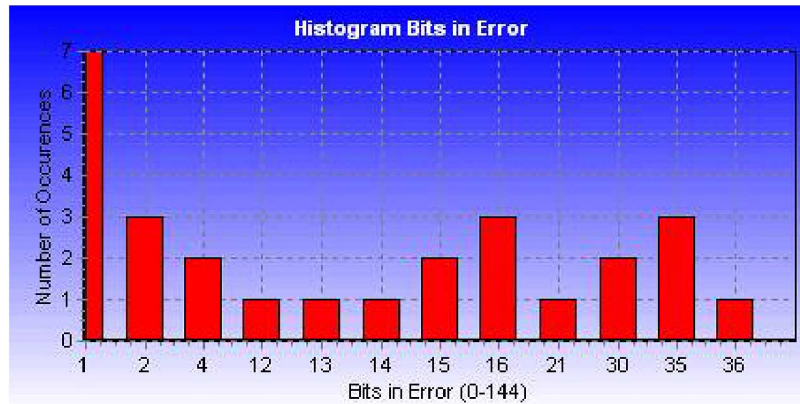

Fig. 1. BIE histogram of a CLKX32 strike in the LP-M/S architecture at 4.5 pJ pulse energy and 3 Gbit/s.

TABLE II
SEU ERROR CAPTURE CATEGORIES AND THEIR DESCRIPTIONS

Error Type	Description
Misfire	BIE=0 (a hit on error flag and/or clock circuitry)
D0	BIE=2 and EL=128 (2 single bit flips separated by 127-bits)
Single-Bit	BIE=1
XOR	A subset of Single-Bit
Flatten to 0	Multiple bit errors (all errored bits '-' , all correct bits 0)
Flatten to 1	Multiple bit errors (all errored bits '+' , all correct bits 1)
LTOT	>=10% to <25% of bits are in error vs. expected 50%
MBD0	Multiple bit D0, similar to D0 except it is repeated
Single-Shift	Pattern changes and never changes back. PRN hit.
Multi-Shift	Best attempt to describe the error as multiple shifts
Double-Shift	Pattern changes, then changes back. (deleted clock pulse)
Mangle	Totally scrambled un intelligible errors.

length (EL), $1 \rightarrow 0$ transitions, and $0 \rightarrow 1$ transitions as shown in Fig. 1. BIE is simply the sum of all "+" and "−" error events, excluding correct bits interleaved within the error. EL is defined as the index of the last BIE minus the index of the first BIE. These definitions are used to categorize errors into one of 13 error categories summarized in Table II.

It should be noted that each data file contains a randomly distributed, finite number of error events (owing to the variation in times for each experimental run). On average, there are 20 to 60 error events logged per run. Therefore, to accurately compare the recorded events, BIE, EL, OTZ and ZTO must all be normalized by the number of recorded error events for each log file. The average BIE, single-bit error percentage, and the percentage of $1 \rightarrow 0$ transitions are used as the primary figures-of-merit in comparing the relative sensitivities of different register architectures, strike locations and bias configurations. Wherever possible, error bars indicate one standard deviation bound on the data.

IV. RESULTS

A representative block diagram of a typical segment of a shift register is depicted in Fig. 2. The circuit blocks that have been targeted for laser strikes are highlighted. Key components of interest include clock buffers, and the last flip flop (DFFLast). Data is collected for a variety of bias conditions, circuit architectures, data rates and deposited charge (laser PE).

A. Clock Buffer Sensitivity

Clock buffers supporting different numbers of flip-flops were targeted for laser strikes. The clock buffer is a simple ECL gate

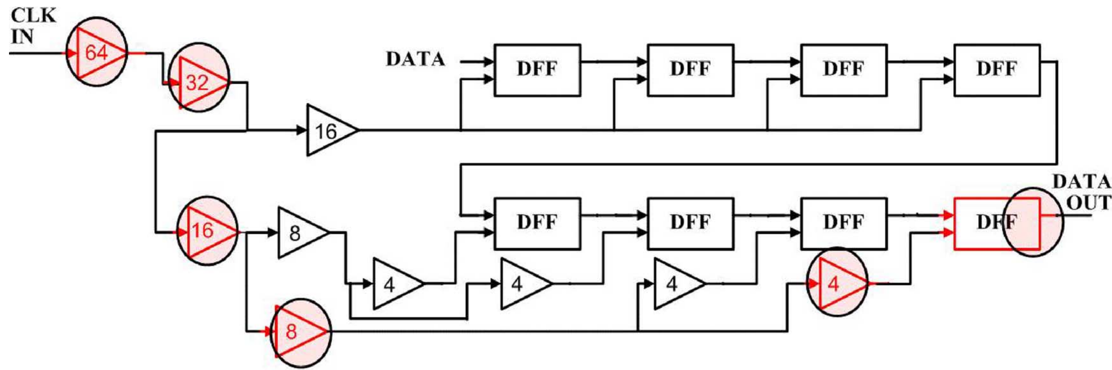

Fig. 2. Block diagram of a segment of a typical register depicting the target circuit blocks.

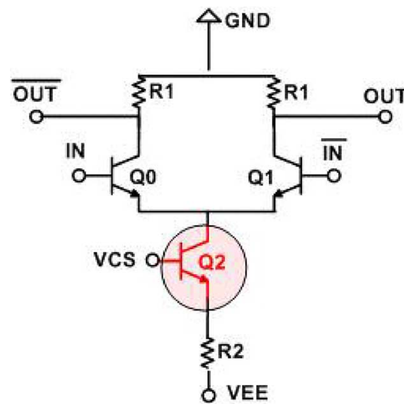

Fig. 3. Typical clock buffer with the control transistor (Q2) targeted for laser strikes.

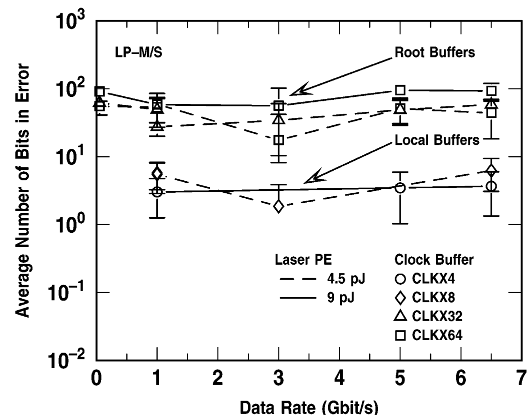

Fig. 5. Average BIE plotted as a function of data rate for local- and root-buffers in the LP-M/S architecture.

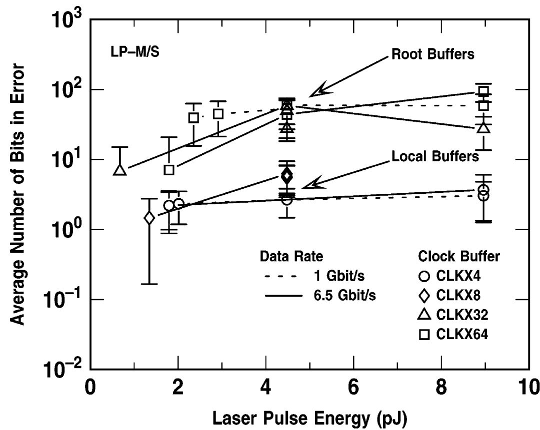

Fig. 4. Average BIE plotted as a function of laser PE for local- and root-buffers in the LP-M/S architecture.

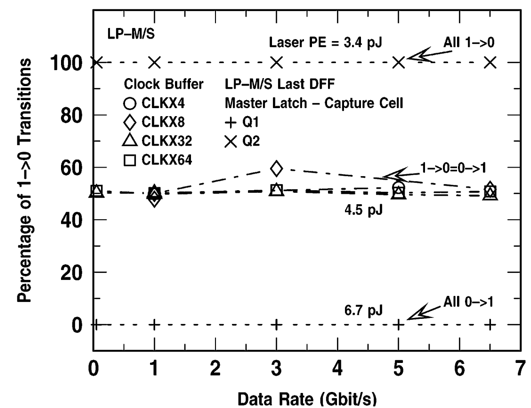

Fig. 6. Percentage of $1 \rightarrow 0$ transitions plotted as a function of data rate for local and root buffers in the LP-M/S architecture. Results are also shown for transistors Q1 and Q2 in the capture cell of the master latch of the last flip flop.

(shown in Fig. 3) used to maintain the voltage levels in the clock tree. We define local-buffers as those supporting 4 or 8 flip-flops, and root-buffers as those supporting 16 to 64 flip-flops. All of the clock-buffer results presented in this section pertain to strikes on the LP-M/S architecture.

The average BIE for strikes on clock buffers is plotted as a function of laser PE in Fig. 4, at data rates of 1 Gbit/s and 6.5 Gbit/s for the LP-M/S architecture. On average, a strike on a local-buffer produces very few BIE, even at high data rates and PE. In contrast, strikes on root-buffers result in an average BIE over an order of magnitude higher. This trend can be very easily explained using the fact that an upset current originating from the OUT terminals in Fig. 3 are propagated through many more flip-flop elements for a root-buffer, than a local buffer. However, it should be noted that the typical register will contain many more local-buffers than root buffers, thereby increasing the contribution of local-buffer strikes to the overall upset rate in a broad-beam test, for example.

Fig. 5 shows the average BIE as a function of data rate at PEs of 4.5, and 9 pJ. The increased average BIE observed for root-buffers compared to local-buffers is observed across all data rates.

Strikes to both the local and root clock buffers result in an equivalent number of $1 \rightarrow 0$, and $0 \rightarrow 1$ transitions as depicted in Fig. 6. The reader is reminded that transistor Q2, in Fig. 2,

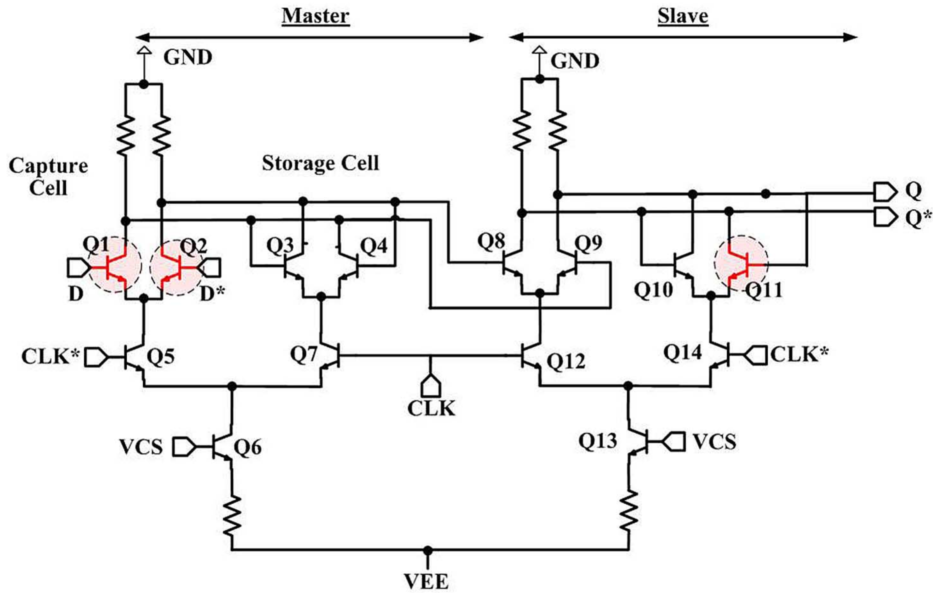

Fig. 7. Targeted transistors (Q1, Q2, and Q11) in the last D flip-flop of the LP-M/S latch.

is located one level below the differential pairs that switch the clock. The equivalent circuit model used to simulate a heavy-ion strike has been used to model the circuit level upset as a current spike in the collector node of the affected transistor along with a coincident drop in the collector voltage at that node [19], upsetting both Q0 and Q1. Furthermore, these upsets are fed into the last flip-flop at a level below the differential pairs that switch the data (Q5, Q7, Q12, and Q14) equally upsetting both pass and storage cells on both clock cycles. This can be contrasted with strikes to any differential pair in the data-path as will be discussed in the next section.

B. Data-Path Sensitivity and Bias Dependence

The last flip flop (as indicated in Fig. 2) was used to investigate the data path sensitivity. Specifically, transistors (Q1 and Q2) in the capture cell of the master latch, and the last transistor in the storage cell of the slave latch (Q11) were targeted for laser strikes as shown in Fig. 7.

The percentage of $1 \rightarrow 0$ transitions for Q1 and Q2 are illustrated in Fig. 6. At a laser PE of 6.7 pJ, for all data rates, strikes to Q1 yielded all 1s (corresponding to the Flatten to 1 error in Table II) and strikes to the complementary transistor, Q2 (at a laser PE of 3.4 pJ), yielded all 0s (corresponding to the Flatten to 0 error). As with strikes on Q2 in the clock buffer, a strike on Q1, Q2 or Q11 in Fig. 7 results in a drop in the voltage at the collector node. Assuming a low (0) on the input (D), a strike on Q1 brings the collector node of Q1 low (it would normally be high). This upset propagates through the circuit and results in a high (1) on the output (Q): (it would normally be a low), a $0 \rightarrow 1$ transition. Conversely, if the input (D) is already high (1), a strike on Q2, the complementary transistor, will bring its collector node voltage low. This propagates through the circuit as a high (1) on the output (Q*), or a low (0) on the output (Q): a $1 \rightarrow 0$ transition. The reader is reminded that the above analysis assumes that only the last flip-flop is examined, that no other transistors in the latch architecture are hit, and additionally, that

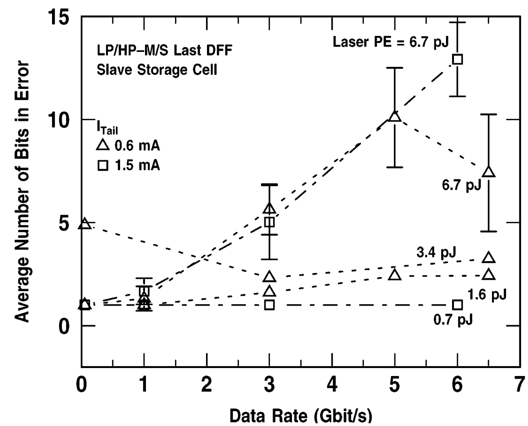

Fig. 8. Average BIE plotted as a function of data rate for a strike on Q11 in the storage cell in the slave latch of the LP/HP-M/S architectures.

the laser stimulus is applied to the target transistor for a sufficiently long duration. This complementary flattening behavior was also observed for strikes to the last flip-flop in other architectures.

The average BIE is plotted as a function of data rate for strikes to Q11 in the slave storage cell in Fig. 8. Results are shown for I_{TAIL} of 0.6 and 1.5 mA at laser PE values of 0.7, 1.6, 3.4 and 6.7 pJ. As expected, the data-path is found to exhibit a greater sensitivity to strikes than the clock tree (last flip-flop compared to local clock buffer). The average BIE for strikes to Q11 in Fig. 7 yielded values between 10 to 15 bits for the highest data rates and PE as depicted in Fig. 8, the corresponding values for strikes to Q2 of the clock buffer shown in Fig. 3, are on the order of 2 to 3 bits as evidenced in Fig. 5. Additionally, at laser PE values of 6.7 pJ (above threshold), the average BIE for strikes to Q11 increases steadily as a function of data rate, characteristic of a particularly short upset duration.

The bias dependence of laser induced upsets is also shown in Fig. 8. In the case of the last flip-flop, there was no observed

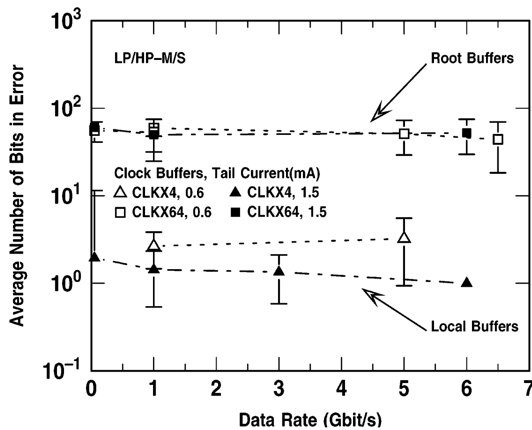

Fig. 9. Average BIE plotted as a function of data rate for local and root clock buffers in LP and HP M/S architectures for two different tail currents.

improvement in the average BIE at the higher value of I_{TAIL}. Similarly, the clock buffers also demonstrated a very small reduction in average BIE as a function of I_{TAIL} particularly for the local-buffers as shown in Fig. 9.

Heavy-ion strike simulations, performed in [9] previously indicated that an increased I_{TAIL} should improve SEU immunity. An increased I_{TAIL} requires a smaller load resistor R_C to maintain the same voltage swing. The ion-induced upset current remains the same, and must now flow through a smaller load resistor resulting in a reduced upset voltage. The experimental results however indicate no significant difference in the upset rate. One possible explanation is that the simulation assumed that the upset current would remain the same for the high-power architecture. In reality however, the HP-M/S architecture uses a larger transistor, thereby the sensitive volume available for charge collection (bounded by the DT) is larger leading to a potentially larger upset current resulting from increased collector collected charge [5], thereby compensating for the effect of the reduced load resistor.

C. Architecture Dependence

Circuit level simulation to address the relative SEU immunity of the latch architectures described above has been extensively discussed in the literature [4], [9]. The NAND gate architecture has been previously found to demonstrate a lower upset rate; however its large power consumption and circuit area are highly undesirable. The failure to eliminate transistor level cross-coupling in the CSH architecture [19] was found to compromise any gains in SEU immunity made using multiple active circuit paths.

In this work, the single-bit error percentage (SB%) will be used as a figure of merit to compare the relative immunity of various architectures. A larger SB % necessarily translates into a smaller average error length and average BIE, which, at the system level would mean reduced upset rates. The strong variation in average BIE as a function of data rate for laser PE values above 4.5 pJ can be understood by looking closely at the error signatures.

In Fig. 10, a histogram of errors, categorized according to their error length (single-bit, 2 to 8, 9 to 64, and 65 to 144), is plotted as a function of data rate for strikes (at laser PE of 6.7 and 3.4 pJ) to transistors Q1 and Q2 respectively in Fig. 7. At low data rates such as 50 Mbit/s and 1 Gbit/s, single-bit errors dominate the response, however, as the data rate is increased, the longer complex burst error modes begin to dominate. Therefore, by looking at the SB % of the different architectures further insight into the gains made via circuit level hardening techniques can be identified. We note that the results for both devices are presented for different laser PEs, however we emphasize that the trends in the recorded error length as a function of data rate remain the same.

The average BIE in the CLK32 buffers for the LP-M/S, NAND, CSH and DI architectures are plotted in Fig. 11. There is no significant difference in the saturation levels of BIE; however, for all the hardening techniques investigated, there is some measure of increased threshold laser PE. At the lowest data rate (50 Mbit/s) the DI architecture produced considerably fewer errors than the LP-M/S both in the "sub-threshold" and "saturation" regimes, while the NAND architecture did not show significant improvement in either region. Strikes to the CLKX24 CSH clock also resulted in increased PE thresholds at 3 Gbit/s, though they were significantly more sensitive at lower data rates.

The greatest evidence for SEU mitigation using these circuit level hardening techniques is illustrated in Fig. 12. In this figure, the SB % of the LP-M/S and HP-M/S, DI and CSH architectures are plotted as a function of data rate at laser PE values above threshold. The SB % for both the LP-M/S and HP-M/S falls to below 10% at 3 Gbit/s, as opposed to 70% for CSH, and 90% for the DI architecture at the same data rate. These gains are very impressive and point to both the promise of circuit level HBD for SEU mitigation in SiGe BiCMOS technology, as well as the viability of pulsed laser testing as a tool for evaluating HBD concepts.

V. Implications for SEU Hardening

A comparative study of SEU sensitivity in these 5 AM SiGe shift registers has been reported, based on detailed multi-Gbit/s bit error analysis. Design techniques formulated to realize improved SEU sensitivity were investigated including multiple circuit architectures, bias dependence, data path and clock buffer sensitivity. Careful classification of the captured error signatures into the error categories enables one to make key comparisons of the relative sensitivities among several available hardening approaches, investigated across a range of laser PE and data rates. A comprehensive solution to the SEU vulnerability of SiGe logic circuits (and other technologies) will be realized only though careful understanding of pulsed laser testing, broad-beam heavy-ion testing, ion micro-beam experiments, and TCAD modeling for accurate charge collection dynamics [20], and robust circuit simulation, to realize architectures tailored to suppress potential bit upsets.

The variation in the SB % for the various architectures can be coupled to the characteristic upset duration. For the LP-M/S latch operating at high data rates and PEs, a characteristic upset duration on the order of 2 to 2.3 ns (for the master capture cell) and 1.13 ns (for the slave storage cell) was observed. These values compare well with the values obtained in [6]. The corresponding value for the last transistor (slave storage cell) in the

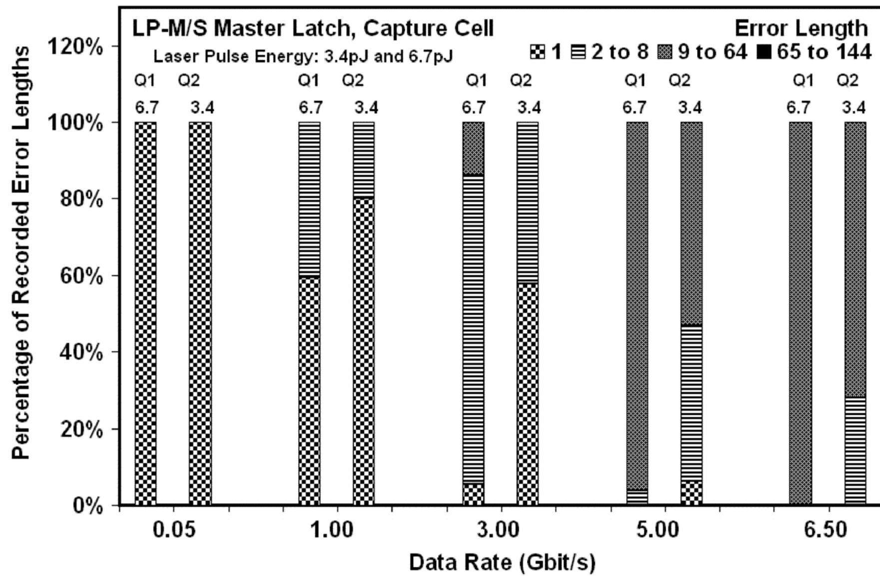

Fig. 10. Stacked histogram of the relative contribution to the total BIE from errors of various lengths to the capture transistors of the LP-M/S architecture. Results are shown for different laser PE values for Q1 (6.7 pJ) and Q2 (3.4 pJ) at data rates from 50 Mbit/s to 6.5 Gbit/s.

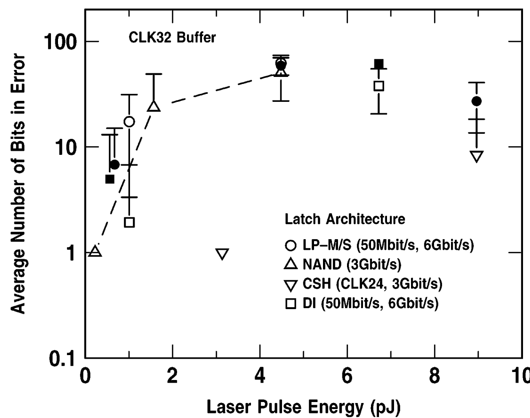

Fig. 11. Average BIE plotted as a function of laser PE for the CLKX32 buffer in different architectures. The closed and open symbols represent the high and low data rates respectively (as indicated in the legend).

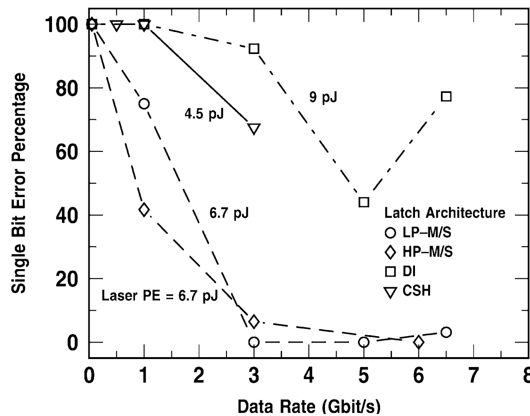

Fig. 12. SB% plotted as a function of data rate for strikes (at different laser PE) to the storage cell of the slave stage in the last flip-flop in shift registers configured using different latch architectures.

DI architecture is on the order of 0.2 ns, which explains the increased single-bit error percentage at higher data rates.

A recent ion-microprobe analysis of SiGe shift registers produced results that are very relevant to this study [21]. As with the pulsed laser test, the ion microprobe is able to explore sensitive transistor nodes within the circuit. A complementary behavior in the response of transistors within the differential pair of a latch was also observed, and a smaller sensitivity was shown in the bias transistors. Additionally, in the ion microprobe study, it was found that upset durations in the slave cell were shorter than in the master cell, and was accounted for based on a variation of the transistor size and switching current. A similar result is observed here, although both master and slave latches employ the same current and transistor size. Finally, the ion microprobe tool is able to give a direct correlation between measured upsets and the corresponding LET. As has been discussed in the text and cited in literature, such a relationship is not as straightforward in the case of pulsed laser testing.

The CREST design and testing methodology is a viable evaluation technique for radiation-hardening-by-design (RHBD) approaches for SEU mitigation, through a precise correlation of the error signatures with physical locations in the circuit layout and incident particle parameters, thereby facilitating better understanding of the most sensitive areas in a given circuit. A combination of device level and circuit-level RHBD techniques should focus on sensitive nodes within the data path and root buffers. Moreover, cadence design tools can be applied to simulate upsets in these regions and evaluate the efficacy of various transistor and circuit level techniques to reduce these upsets. Such simulation data can then be directly compared to the recorded error events resulting in more robust error prediction capability.

VI. Summary

The results from pulsed laser testing indicate that sensitive nodes are distributed throughout the register. Clearly, a strike on a root buffer results in up to 10 times more BIE than local buffers, however, above the threshold laser PE, no significant

increase in errors are recorded. Increases in I_{TAIL}, previously found to improve SEU immunity, had no significant effect on the average number of recorded BIE. Upsets emanating from a strike on a clock buffer are evenly distributed between $1 \rightarrow 0$ and $0 \rightarrow 1$ transitions. In contrast, strikes on transistors within the differential pair of a master slave latch in the last flip-flop result in an asymmetric distribution of errors, flattening to a "0" or "1" depending on which node is hit. Additionally, above threshold laser power, strikes on these nodes result in a BIE that increases steadily with data rate. Some improvement in the SEU response, measured using the percentage of single bit errors as a figure-of-merit, is observed for CSH and DI circuit hardening techniques compared to the LP-M/S architecture. These improvements are seen in the last flip-flop only, and not in the clock distribution network.

Acknowledgment

The authors would like to thank L. Cohn, K. LaBel, and the IBM SiGe team for their contributions to this work.

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Application of RHBD Techniques to SEU Hardening of Third-Generation SiGe HBT Logic Circuits

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***Abstract*—Shift registers featuring radiation-hardening-by-design (RHBD) techniques are realized in IBM 8HP SiGe BiCMOS technology. Both circuit and device-level RHBD techniques are employed to improve the overall SEU immunity of the shift registers. Circuit-level RHBD techniques include dual-interleaving and gated-feedback that achieve SEU mitigation through local latch-level redundancy and correction. In addition, register-level RHBD based on triple-module redundancy (TMR) versions of dual-interleaved and gated-feedback cell shift registers is also realized to gauge the performance improvement offered by TMR. At the device-level, RHBD C-B-E SiGe HBTs with single collector and base contacts and significantly smaller deep trench-enclosed area than standard C-B-E-B-C devices with dual collector and base contacts are used to reduce the upset sensitive area. The SEU performance of these shift registers was then tested using heavy ions and standard bit-error testing methods. The results obtained are compared to the unhardened standard shift register designed with CBEBC SiGe HBTs. The RHBD-enhanced shift registers perform significantly better than the unhardened circuit, with the TMR technique proving very effective in achieving significant SEU immunity.**

***Index Terms*—Current mode logic (CML), heavy ion, heterojunction bipolar transistor (HBT), radiation hardening by design (RHBD), shift register, silicon-germanium (SiGe), single-event upset (SEU), triple-module redundancy (TMR).**

I. Introduction

SILICON-GERMANIUM (SiGe) heterojunction bipolar transistor (HBT) technology has generated considerable interest in the space community due to its robustness to total ionizing dose (TID) radiation, without any additional hardening [1]. This TID tolerance does not, unfortunately, translate into improved single event upset (SEU) response for SiGe HBT logic. Digital circuits designed in first-generation (50 GHz) and second-generation (120 GHz) SiGe technology have been shown to be very sensitive to SEU [2]–[5], and circuit-level hardening using the current-shared hardening (CSH) [6] technique proved ineffective in mitigating single event upsets in these circuits.

Radiation-hardening-by-design (RHBD) employs layout and circuit architecture changes for the radiation hardening of space electronic systems using commercial foundry processes, with no modifications to the existing process or violation of design rules. In this work, we have applied RHBD techniques to improve the SEU immunity of SiGe HBT high-speed logic circuits.

II. SiGe HBT BiCMOS Technology

Shift registers featuring these RHBD techniques were realized for the first time in the commercially-available IBM SiGe 8HP BiCMOS technology platform. This process incorporates a 130 nm "raised extrinsic base" SiGe HBT structure with an *in-situ* doped polysilicon emitter, deep and shallow-trench isolation. The SiGe HBT has a peak unity-gain cut-off frequency (f_T) of 200 GHz [7]. The technology also integrates 130 nm CMOS devices as well as a wide array of passive elements and seven layers of metalization.

III. SiGe RHBD Techniques

A. Circuit-Level Techniques

Three different types of 16-bit shift registers in the current mode logic (CML) family were investigated in this work. The clock "tree" architecture in these shift registers was identical to the one used in shift registers reported in [3], with a master clock buffer driving four intermediate clock buffers, each in turn providing clock inputs to a set of 4-D flip flops (Fig. 1). Thus, as was noted in [3], an upset occurring in the clock tree has the potential to cause multiple bit upsets. Therefore, to improve their SEU immunity, the clock buffers in the present designs featured circuit-level hardening based on the gated-feedback cell (GFC) RHBD technique [8]. Two RHBD local circuit-redundancy based circuit-level hardening techniques were employed in the design of the constituent D-flip flops in two of the three shift registers, while the remaining shift register, referred to as "standard MS SR" ("std. SR"), featured unhardened conventional CML master-slave (MS) D-flip flops (Fig. 2), and was

Manuscript received July 14, 2006; revised August 21, 2006. This work was supported by the DARPA RHBD Program, DTRA under the Radiation Hardened Microelectronics Program, NASA-GSFC under the NASA Electronic Parts and Packaging (NEPP) Program, Mayo Foundation, Boeing, NASA ETDP, and the Georgia Electronic Design Center at Georgia Tech.

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Digital Object Identifier 10.1109/TNS.2006.885379

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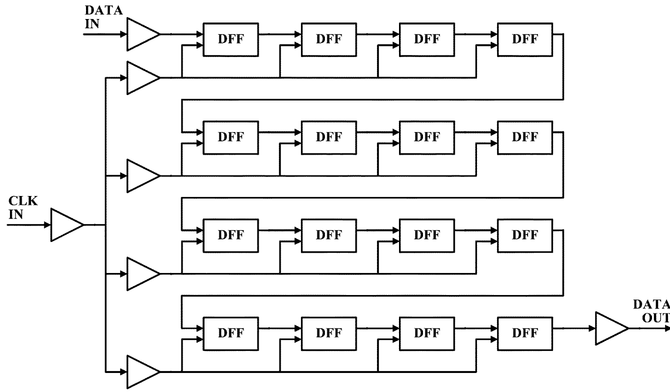


Fig. 1. Block diagram of the 16-bit shift registers.

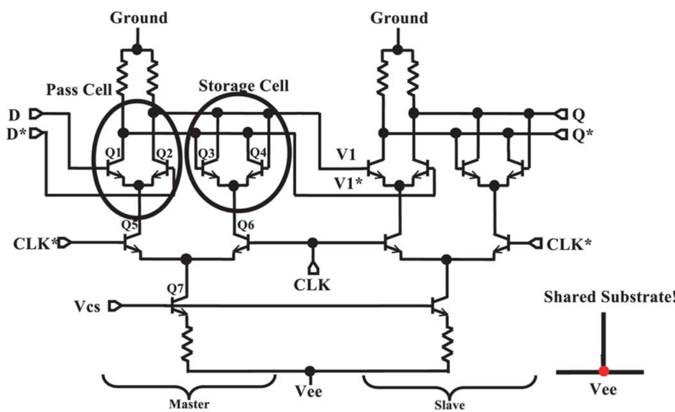


Fig. 2. Schematic of standard CML master-slave D-flip flop.

used as the baseline circuit (control) to enable meaningful comparisons. To study the effects of reduced bias current on the SEU characteristics of the shift registers, low-power ($I_{\rm tail} = 0.5$ mA) and high-power ($I_{\rm tail} = 1.0$ mA) versions were implemented. $I_{\rm tail}$ is the tail current of any differential pair in the D-flip flops. Upon complete switching the current flowing through the load resistor connected to the ON transistor is very close to $I_{\rm tail}$.

1) Dual-Interleaving-Based RHBD: One of the RHBD shift registers incorporated D-flip flops based on a newly proposed circuit implementation [10], referred to here as "dual-interleaved SR" or "DI SR" (Fig. 3). A previous study [11] on the dependence of SEU response on circuit architecture in the CML logic family indicated that cross-coupling at the transistor-level, required for the storage cell functionality in the standard master-slave D-flip flop (Fig. 2), increases the vulnerability of this circuit to SEU. Thus, local redundancy was built into the standard master-slave D-flip flop, which consumes the least power and occupies the smallest area, to incorporate limited transistor-level decoupling in the storage cell, thereby mitigating its SEU sensitivity with only a moderate increase in power consumption and circuit complexity.

Unlike the standard MS SR, the base and the collector of the transistors in the storage cell of the DI SR are not connected to the same differential pair in the pass cell, thus achieving effective decoupling of the base and collector terminals of the transistors in the storage cell. For instance, the base of Q5 in DI SR storage cell is connected to the collector of Q1 in the pass cell, whereas the collector of Q5 is connected to the collector of Q3 of the alternate differential pair in the pass cell. However, to maintain the storage cell functionality, the base and collector of each transistor in the storage cell are connected to complementary outputs from the pass cell. Thus, an SEU transient current flowing through the collector of the transistor Q5 does not affect the base directly. The voltage drop due to this transient flow, however, does affect the base of Q7, which might indirectly affect the base of Q5, potentially leading to upset [10].

2) Gated-Feedback Cell-Based RHBD: The other RHBD shift register featured a slightly modified gated-feedback cell (GFC) based master-slave D-flip flop [8], referred to here as "GFC SR" (Fig. 4). The OR-gates available in the GFC architecture perform a logical OR operation on identical logic outputs from the pass cell pair and feed the result back to the appropriate inputs of the duplicate storage cell pair. The OR operation, enabled by a pair of emitter followers, helps transmission of the correct logic to the storage cell inputs even when one of the OR gate inputs is in error via an ion strike.

The output of a two-input OR gate changes state only when both the inputs change state from high to low or low to high. A ion-strike on an npn transistor, in general, causes ion-induced current to flow into the collector, thereby pulling the collector potential low. Therefore, an ion strike on a storage cell transistor such as Q5 causes its collector and in turn the input to transistor Q9 to go low. This spurious transition, however, does not affect the output of the OR as the other input to Q10 is unaffected. In addition, the inputs to Q11 and Q12 (transistors in the alternate OR gate) are also unaffected, thereby ensuring the correct logic at the input (or base) of Q5. Thus, the OR-gate-based feedback to the storage cell inputs, in addition to local redundancy, is in principle expected to offer SEU immunity that is higher than that provided by dual-interleaving. In addition, there are diode voltage clamps positioned across the load resistors to increase the current onto an upset collector node, thus reducing the upset duration [8], [9].

3) Register-Level RHBD: Additional register-level RHBD based on triple-module redundancy (TMR) was applied to the low-power versions of DI SR and GFC SRs (referred to as DI TMR and GFC TMR, respectively), to gauge the performance improvement achieved from this additional level of RHBD. The output was selected based on majority voting between three redundant shift registers using GFC-hardened and unhardened voters working in parallel. Separate select lines (S1-S3) were provided for enabling or disabling individual shift registers in the circuit to test their functionality (Fig. 5).

B. Device-Level RHBD Techniques in SiGe HBTS

A previous microbeam study on second-generation SiGe HBTs concluded that the active region defined by the deep-trench (DT) boundary is only a portion of the upset sensitive volume and that the remaining sensitive volume encompasses the region of substrate several micrometers away from the trench [4]. Despite this observation, reduction in area enclosed by DT is expected to significantly improve the net upset cross-section of the transistor by reducing the effective

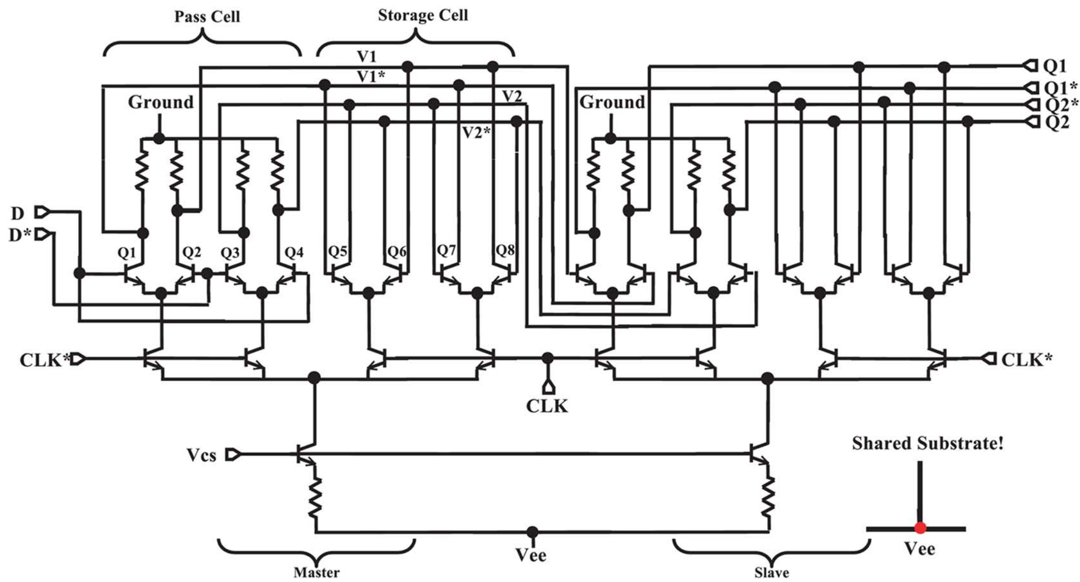


Fig. 3. Schematic of the new RHBD dual-interleaved D-flip flop circuit with minimal cross coupling in the storage cell.

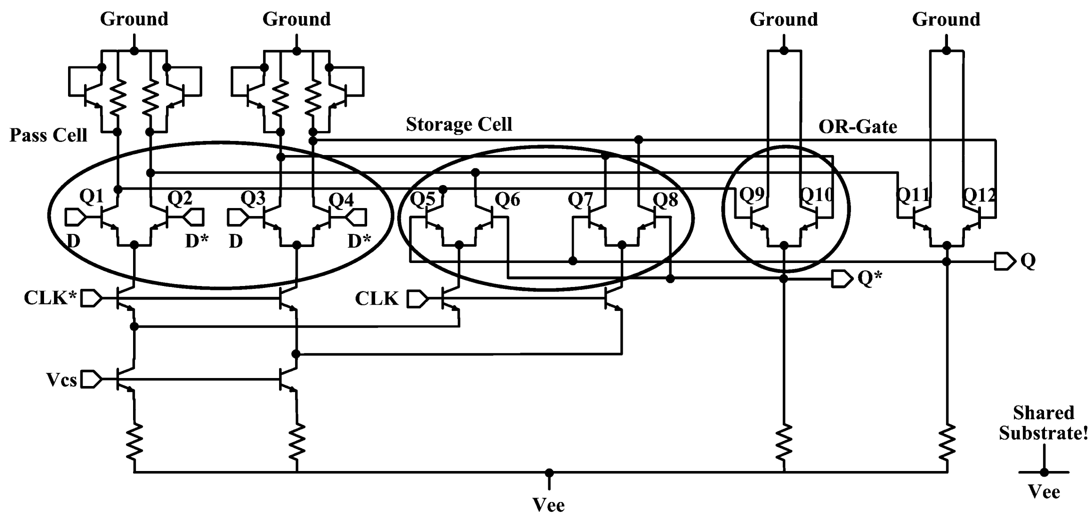


Fig. 4. Schematic of master stage of the GFC D-flip flop.

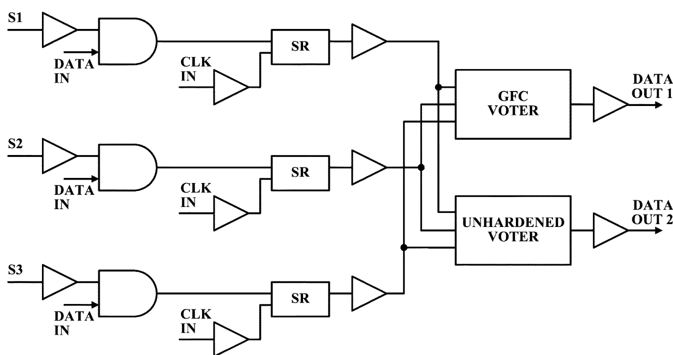


Fig. 5. Block diagram of the triple module redundancy (TMR) implementation.

sensitive area [12]. Thus, a transistor with minimum feature size, and with only a single collector, base, and emitter contacts (C-B-E), as opposed to the standard device with double collector and base contacts (C-B-E-B-C), was selected as the workhorse RHBD device to minimize local ion-induced upset cross-section within the RHBD latches. While the C-B-E-B-C device with an emitter area (A_E) of 0.12×2.50 μm^2 was used in the baseline standard MS SR, the RHBD (C-B-E) device with A_E of 0.12×0.52 μm^2 was employed in all other shift registers. Only a slight ac device performance penalty resulted. The internal trench area for the C-B-E-B-C was 15.10 μm^2 while that for the RHBD C-B-E devices was 4.08 μm^2. Thus, the net reduction in trench enclosed area for the RHBD SiGe HBT was about 73%. A bigger C-B-E-B-C device was intentionally used in the baseline circuit to demonstrate the degradation in upset cross-section associated with larger trench volume [Fig. 6(a) and (b)].

The various hardening techniques investigated are summarized in Table I. In addition, the total power consumption of the various shift registers, the contribution of individual D-flip flop to the total power consumption, the D-flip flop area, and the

TABLE I
COMPARISON OF HARDENING TECHNIQUES

Topology	Circuit Technique	Device Technique	
		Type	Emitter Area (μm^2)
Std SR	unhardened	C-B-E-B-C	0.12×2.50
DI SR	latch-level redundancy + limited decoupling	C-B-E	0.12×0.52
DI SR Low-P	latch-level redundancy + limited decoupling	C-B-E	0.12×0.52
DI TMR	three DI SR + voting at end	C-B-E	0.12×0.52
GFC SR	latch-level redundancy + OR-gate feedback + load diode clamps	C-B-E	0.12×0.52
GFC TMR	three GFC SR + voting at end	C-B-E	0.12×0.52

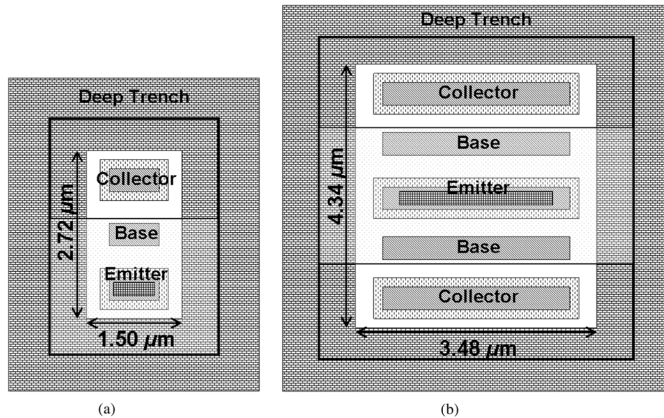


Fig. 6. (a) RHBD C-B-E transistor and (b) C-B-E-B-C transistor used in the baseline Std. SR.

maximum post-layout simulated speed are tabulated in Table II. Clearly, the operating speed of low power DI SR and the power consumption of its constituent D-flip flops are comparable with those of the standard SR with only a slight area penalty overhead and with minimal increase in layout complexity, suggesting that dual-interleaving can potentially be applied to other technology nodes. RHBD shift registers with much higher operating speeds than those presented here are clearly possible in this technology [13]. The primary reason for the more modest operating speeds for the present shift registers lies in the (intentional) overdesign of the latch output buffers, which caused significant internal capacitive loading. This can easily be altered as needed for specific speed requirements without compromising SEU performance. For instance, simulations using more standard buffers for the DI SR can be clocked to well above 20 GHz speeds. The die photomicrographs of a 16-bit shift register and its TMR implementation are shown in Fig. 7(a) and (b). The die area of 16-bit shift registers is 2.356×1.586 mm^2 and the die area of the TMR version is 2.636×2.686 mm^2, and dictated by the high-speed packaging fixture used.

IV. Test Setup

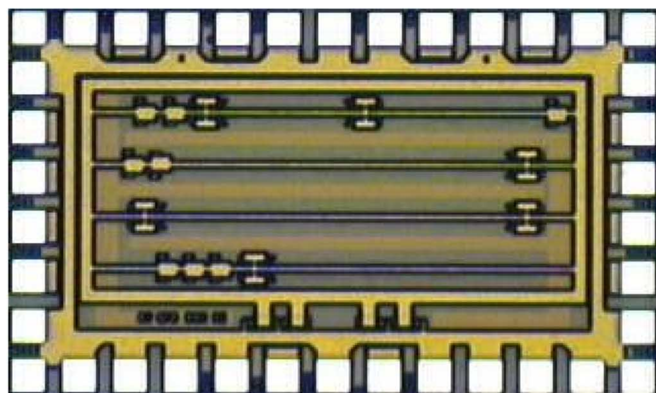
The shift registers (devices under test—DUT) were designed at Georgia Tech, and packaged at the Mayo Foundation. Two sets of heavy ion tests were performed at the Texas A &M Cyclotron Institute. In the first iteration the DUTs were subjected to Ne, Ar, and Xe ions at 15 MeV/amu. This was followed up with a second iteration where the DUTs were subjected to 15 MeV/amu Kr ion to obtain SEU response at the intermediate LET values. The angle of incidence of ion-beam was increased from normal incidence (0°) to 45° and 60° to vary the effective LET for a given ion. The DUTs, being serial shift registers, are ideal for standard Bit Error Rate Test (BERT) methods. The test set consisted of, fundamentally, a data source and an analyzer to examine the output of the DUT. The data source was a custom-built, Pseudo-Random Number (PRN) generator, which generated 2^7-1 long bit patterns. An Anritsu MP1764A, a 12.5 Gbit/s BERT analyzer, which can count bit errors and save the transmitted data stream in the vicinity of errors, was used. The data rates were continuously variable from 50 Mbit/s up to the maximum frequency of operation of a given DUT, and we typically acquired error information at several data rates of interest. A computer running Labview under Windows XP controlled the equipment, gathered the data, and provided some real-time data analysis. Further, the clock and data inputs were driven differentially with voltage swings compatible to CML voltage levels. Additional equipments such as a balun, 6 dB splitters, delay-lines, and bias-Ts were used to derive differential clock and data signals from a single RF source (Fig. 8).

V. Heavy Ion Data and Analysis

Figs. 9–11 show the heavy ion induced event cross-section (σ) as a function of effective LET for all circuits tested in this work, at various data rates. Event cross-section is chosen for representation of upsets in order to decouple the effect of varying error durations and to present only the physical ion-circuit interactions. As expected, the baseline standard MS SR displays the highest saturated device cross-section ($\sigma_{\rm sat}$) across all data rates (Figs. 9–11). The downward pointing arrows at LETs of 2.8, 5.8, and 12 MeV-cm^2/mg in Fig. 9 correspond to limiting cross-sections (i.e., no upset bits) associated with the RHBD DI TMR, GFC SR, and DI SR, respectively. Interestingly, the low-power version of the DI SR, despite having the same $I_{\rm tail}$ as the standard MS SR, but with twice as many sensitive nodes, shows $>$ $2.5\times$ lower σ or equivalently 60% reduction in σ (Figs. 9–11) at almost all data rates. This improvement in σ is, however, higher than the estimated $1.85\times$ improvement or equivalently 46% net reduction in σ. The $1.85\times$ improvement in σ was estimated by combining the 73% "reduction" in transistor upset cross-section associated with using RHBD CBE SiGe HBTs in DI SR and the expected $2\times$ degradation in σ attributable to the $2\times$ more sensitive nodes in the DI SR compared to standard MS SR. The potential reason for higher achieved improvement could be due to the "immunity" provided by the circuit hardening technique. Note that this simplified analysis does not account for charge collection from outside the deep-trench, which was concluded to

TABLE II
COMPARISON OF POWER CONSUMPTION, AREA, AND SPEED

Topology	D-flipflop I_{tail} (mA)	Power (mW) Total	Power (mW) Flipflop	D-flip flop Area ($\times 10^3$ μm^2)	Max. Sim. Speed (Gbit/s)
Std SR	0.5	257	11	10	6
DI SR	1.0	506	19	16	8
DI SR Low-Power	0.5	399	12	16	7
DI TMR	0.5	1136	19	16	5
GFC SR	1.0	729	40	25	8
GFC TMR	0.5	1945	33	25	5


(a)

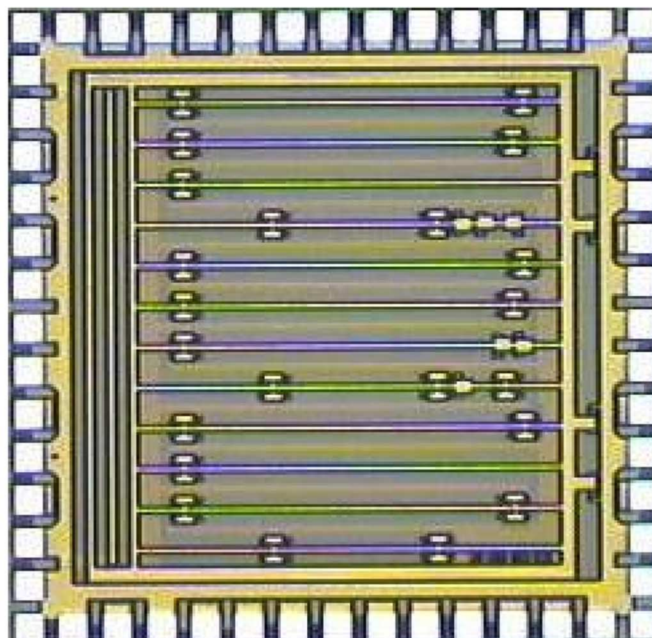

(b)

Fig. 7. Die micrograph of a 16-bit shift register (a) and its TMR implementation (b).

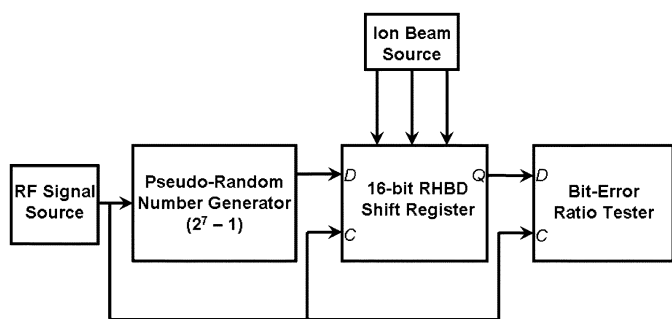


Fig. 8. Block diagram of the heavy-ion test-setup for SEU characterization of 16-bit RHBD shift registers.

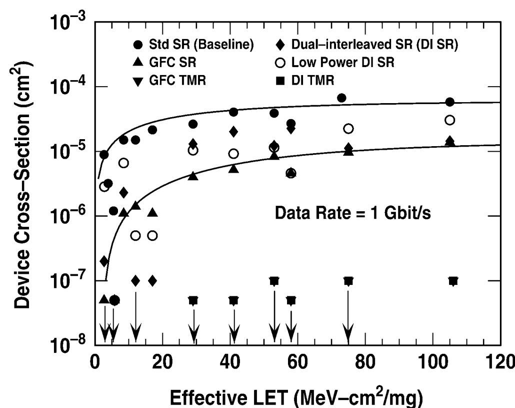


Fig. 9. Device cross-section (σ) as a function of effective LET for data rate = 1.0 Gbit/s.

be significant in second-generation SiGe HBTs [4]. This simplification further disregards the "function-related" sensitivity of individual transistors in the circuit observed in a previous work, which, however, also concluded that larger transistors present larger sensitive area [12]. The high-power version of the DI SR, as expected [14], showed significantly better performance over the low-power DI SR version at lower data rates, to a lesser extent at higher data rates, across all ion LETs. The high-power GFC SR showed the better σ_{sat} performance over DI SR at low data rates and progressively degraded as the frequency increases, but always remained better than or comparable to that of the DI SR.

The heavy ion test data showed limiting cross-sections in both "double RHBD" DI TMR and GFC TMR at 1 Gbit/s (and at higher data rates) up to an LET of 75 MeV-cm^2/mg (Fig. 9). However, at data rates below 100 Mb/s in GFC TMR and below

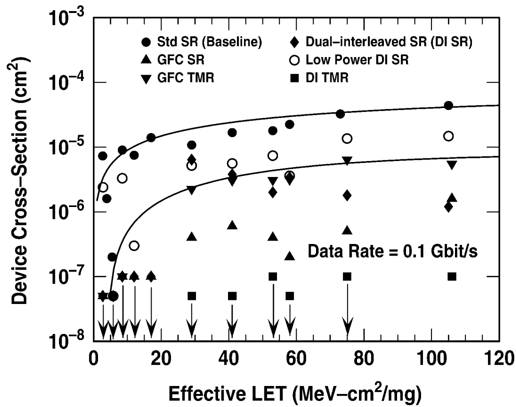


Fig. 10. Device cross-section (σ) as a function of effective LET for data rate = 0.1 Gbit/s.

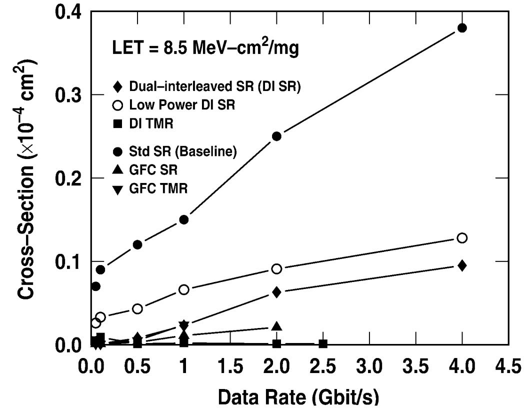


Fig. 12. Device cross-section σ as a function of data rate for $\mathrm{LET} = 8.5$ MeV-cm^2/mg.

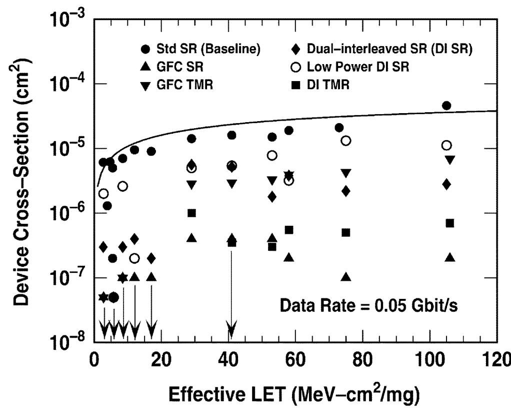


Fig. 11. Device cross-section (σ) as a function of effective LET for data rate = 0.05 Gbit/s.

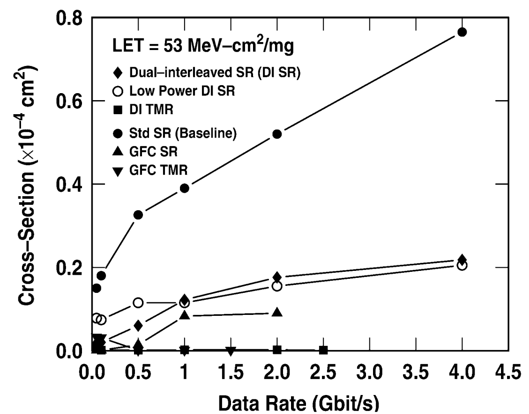


Fig. 13. Device cross-section σ as a function of data rate for $\mathrm{LET} = 53$ MeV-cm^2/mg.

50 Mb/s in DI TMR the SEU response degraded considerably. Despite this anomalous low data rate behavior, the fact that TMR offers significant improvement in the SEU response of the shift registers is in itself an important and encouraging result. Interestingly, the TMR in GFC SR did not provide as much improvement in σ at low speeds as the TMR in the DI SR (Figs. 10 and 11). In addition, the σ of GFC TMR was worse than that of high-power GFC SR at low data rates. Although this observation could possibly be explained based on the reduced bias current in the constituent shift registers, it is still puzzling to note that register-level redundancy and voting had little effect in improving the overall SEU immunity at low data rates, given that the GFC SR in itself had the best performance among non-TMR shift registers. That said, cross-section data for low-power GFC SR would be required for a more meaningful comparison.

Figs. 12 and 13 show that the event cross-section of all the shift registers except the DI TMR and GFC TMR increases with frequency at LETs values of 8.5 and 53 MeV-cm^2/mg, respectively, which is in agreement with a previous study in first-generation SiGe shift registers [2] and consistent with clock edge related SEU sensitivity. This result is evidently in disagreement with results from a previous study using second-generation SiGe technology [5], in which even though σ increased with data rate at low frequencies, a saturation of σ was noted at higher frequencies.

Figs. 14–16 capture the average error per error event as it varies with the data rate, at LETs of 8.5, 29, and 53 MeV-cm^2/mg, respectively. It is clear at LETs of 29 and 53 MeV-cm^2/mg that average errors in all of the circuits except the TMRs increases with data rate, linearly from a value of 1 at low data rates to as high as 8 at 4 Gbit/s in the unhardened standard SR. All other circuits show relatively lower average errors per event compared to the standard SR, which could possibly be due to lower upset durations in these circuits, hence resulting in lower temporal multiple bit errors. At low LETs (Fig. 14), however, average errors did not show a linear increase with data rate, except in the case of the standard SR. In fact, the average errors remained close to 1 to data rates as high as 2 Gbit/s, indicating short upset durations. Interestingly, there were no errors observed at data rates above 100 Mb/s for LETs as high as 75 MeV-cm^2/mg in the TMR shift registers and at low data rates for lower LET values in GFC SR and DI SR (Figs. 14, 15, and 16). Under such conditions average errors per event was assumed to be 0.

Table III gives a summary of our SiGe RHBD results, including threshold LETs of the various circuits. These LET thresholds were estimated in two different ways; by fitting of a standard Weibull curve to the data (L_{th}), and by using the LET value at 10% $(L_{0.1})$ of the estimated saturated cross section. For reference, at 1 Gbit/s comparison of the standard MS SR

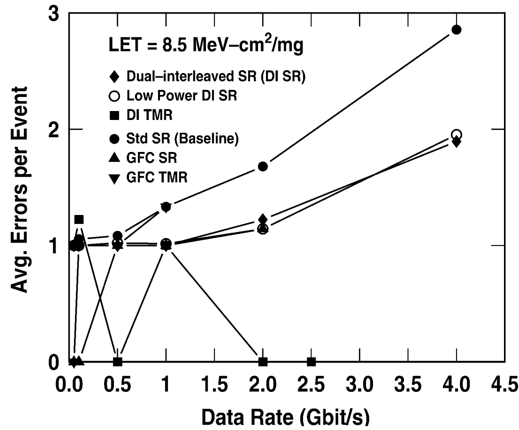


Fig. 14. Average errors per error events as a function of data rate for $\mathrm{LET} = 8.5$ MeV-cm^2/mg.

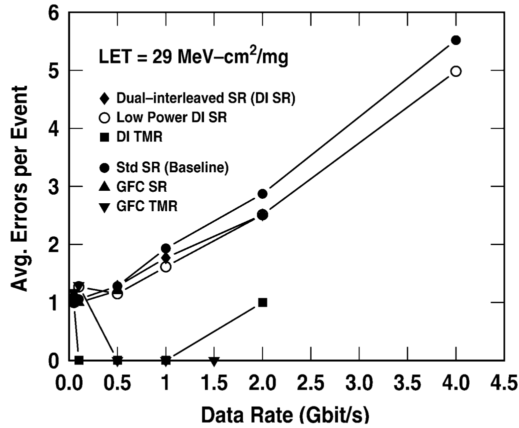


Fig. 15. Average errors per error events as a function of data rate for $\mathrm{LET} = 29$ MeV-cm^2/mg.

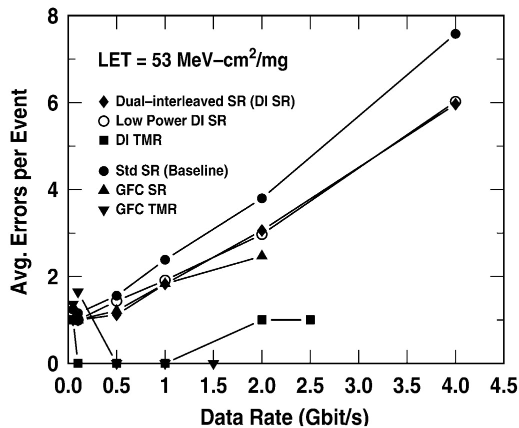


Fig. 16. Average errors per error events as a function of data rate for $\mathrm{LET} = 53$ MeV-cm^2/mg.

to the Dual-interleaved TMR SR (worst to best case), yields an improvement in threshold LET over of $7500\times$ based on Weibull fit parameter, L_{th}. This is clearly a significant improvement, and represents the first successful SEU hardening of SiGe logic circuits. We are encouraged by these results, and believe that they represent a step forward towards a potentially effective mitigation path for SEU hardening of SiGe logic using purely RHBD techniques.

TABLE III
ESTIMATED THRESHOLD LET FOR THE SHIFT REGISTERS

Topology	L_{th}		$L_{0.1}$	
	0.1 Gbit/s	1 Gbit/s	0.1 Gbit/s	1 Gbit/s
Std SR	0.01	0.01	4.0	1.8
DI SR	6.0	2.0	10.0	6.2
DI SR Low-Power	0.05	0.4	1.8	3.4
DI TMR	>75	>75	-	-
GFC SR	6.0	2.2	10.0	10.0
GFC TMR	4.0	>75	10.0	-

VI. SUMMARY

A combination of circuit- and device-level RHBD techniques was successfully applied in the realization of high-speed shift registers for the first time in IBM SiGe 8HP BiCMOS technology. The use of RHBD C-B-E SiGe HBTs with 73% smaller trench-enclosed (DT-enclosed) area than conventional C-B-E-B-C devices, and circuit RHBD techniques such as the dual-interleaving, gated-feedback, and TMR, proved effective in improving the overall SEU immunity of the shift registers, to high LET values. Limiting cross-sections were observed to a LET value of 75 MeV-cm^2/mg at 1 Gbit/s data rate in DI TMR. In addition, a significant improvement in threshold LET was observed in RHBD circuits compared to the unhardened standard CML shift register.

ACKNOWLEDGMENT

The authors are grateful to K. LaBel, L. Cohn, D. Chaney, W. Snapp, D. Radack, A. Campbell, and the SiGe team at IBM for their contributions.

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Task #4: Sensors – related articles.

Distribution of Proton-Induced Transients in Silicon Focal Plane Arrays

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***Abstract*—Proton-induced energy deposition in a silicon P-i-N focal plane array is analyzed with Monte Carlo based simulations. These simulations include all physical processes, including events resulting from multiple particles incident on a single pixel, to describe the experimental data accurately. Post-processing of Monte Carlo simulations is done to account for the effects of pile up (multiple hits on a single pixel during one integration time) and non-radiation-induced noise in experiment. The results are compared with experimental data, and demonstrate how direct ionization dominates the cross section, yet fluctuations in *dE/dx* cause a broad range of energy depositions not addressed by an average LET calculation. An event rate is predicted for a full space proton flux and the dominance of direct ionization is shown and compared to computation using constant LET methods in CREME96. This comparison shows that at lower energies, CREME96 sufficiently predicts the event rate, but at higher energies a high fidelity simulation method is needed to capture the distribution.**

***Index Terms*—Energy deposited, event rate, focal plane array, Geant4, Monte Carlo, pile up.**

I. INTRODUCTION

HYBRID focal plane arrays (FPA) are used in space applications because of their flexibility in infrared applications, reliability, low cost, high resolution, and on-chip signal processing [1]. FPAs have important applications for satellite missions such as space-borne astronomy, Earth surveillance, star tracking, digital imaging, laser communications, etc. They are often used on satellites planned for long duration orbits in harsh proton environments requiring exceptional reliability when exposed to radiation. Because of their high sensitivity to noise, FPAs present a unique challenge in radiation hardness. Optical currents are small and near noise levels, so a single particle can produce enough charge to disrupt a signal [2]. Fig. 1 shows how the image produced by an optical sensor can be degraded by a solar proton event [3]. The image on the left in Fig. 1 captures a coronal mass ejection occurring on August 26, 2001. Coronal mass ejections are very rich in protons, increase the solar wind velocity, and can reach satellites in Earth's orbit quickly. The image on the right shows the image produced by a charge-coupled device (CCD) over an hour later degraded due to transient proton events. Spacecraft shielding helps mitigate incident electrons, but does not protect against protons, which also deposit energy and create secondary electrons. Hybrid visible array technology is especially important due to advantages over CCD-based imagers in high proton exposure applications. CCDs require collected charge to be transferred many times before being readout, and a loss of charge through proton induced traps can occur [4]. Hybrid FPAs require at most one transfer, thereby reducing the trapping vulnerability. On the other hand, a silicon P-i-N device can have quite a thick collection volume, which makes the quantitative evaluation of the sensitivity to proton-induced transients an important issue.

A better understanding of how radiation deposits energy in these devices will help lead to better prediction techniques and a greater understanding of experimental results. Accurate modeling tools will help designers predict the on-orbit response of these devices. In this paper we demonstrate a high-fidelity rate-prediction approach, based on Monte Carlo simulation and a mathematical model that accounts for multiple events that affect a single pixel during the integration time. Previous work has shown the ionization spectrum for a detector is different from the energy loss spectrum of particles causing the ionization [5]. In [6], it is noted that a constant LET approximation is a good assumption for some applications, but not all. In this paper we will quantify through simulation and experiment how using a single-value LET and path length calculation does not capture the full distribution.

II. EXPERIMENTAL DESCRIPTION

Hybrid focal plane arrays consist of a readout integrated circuit (ROIC) and detector array fabricated separately and then joined together with interconnects such as indium columns [2]. Fig. 2 shows the structure of a generic hybrid FPA [7]. The focal plane arrays in this study are well characterized visible-light, back-side illuminated FPAs consisting of a silicon P-i-N

Manuscript received July 17, 2007; revised September 3, 2007. This work was supported in part by NASA Electronic Parts and Packaging (NEPP) program and the Defense Thread Reduction Agency (DTRA) Radiation Hardened Microelectronics Program under IACRO #07-4201i to NASA, as well as the Medical Free-Electron Laser (MFEL) Program. The computational portion of this work was conducted through Vanderbilt University's Advanced Computing Center for Research and Education (ACCRE).

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Digital Object Identifier 10.1109/TNS.2007.909511

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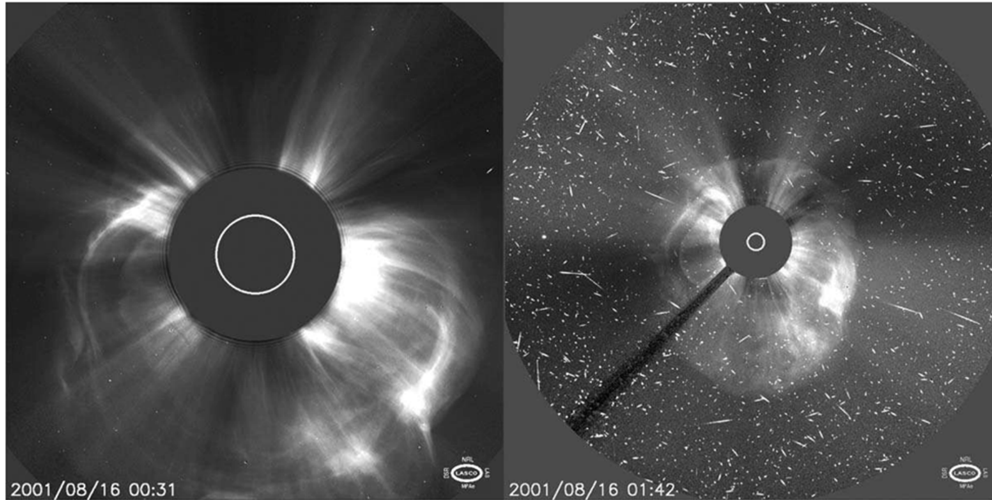

Fig. 1. Coronal mass ejection captured by LASCO on August 26, 2001. Over an hour later, degradation of the image produced by the optical detector can be seen on the right figure [3].

128×128 detector array with a radiation hardened complementary metal–oxide semiconductor (CMOS) ROIC and pixel pitch of 60 μm [8]. Proton radiation studies were performed at the Crocker Nuclear Laboratory (CNL) of the University of California, Davis (UC Davis). Full radiometric characterizations were performed at each radiation dose level to determine the impact of the radiation on dark current, noise, responsivity, sensitivity, and dynamic range both pre and post radiation [8]. In [8], we describe the total-ionizing-dose response of this array. This paper focuses on the proton-transient data, acquired at low fluxes, generating sparse hits to the array with 63 MeV protons at an angle of 45 degrees. The detectors were biased at 15 V, resulting in full depletion. Exposures were carried out at 233 K with temperature monitored by two radiation-hardened sensors not in the proton beam. Protons were incident on the silicon detector and then passed through the ROIC.

III. Modeling Focal Plane Detectors

A. Monte Carlo Simulations

The radiation-transport Monte Carlo code used in this study is MRED (Monte Carlo Radiative Energy Deposition), a Geant4 based tool [9], [10], [11]. The structure used to simulate the focal plane detectors is shown in Fig. 3. The sensitive region corresponds to the region in which energy deposition must occur to produce a transient event. The top and bottom of the sensitive volume are flush with the top and bottom of the surrounding material, which is also silicon.

Simulations using MRED included physics processes that are relevant for radiation effects applications, including electromagnetic and hadronic processes, and elementary particles that live long enough to be tracked [11]. The effects of the finite integration time were simulated in a manner analogous to the computation of pile up in an ordinary nuclear spectrum. Each event in the Monte Carlo simulation represents one, and only one, primary particle. For finite integration times, there is a small but non-negligible probability of multiple hits on a single pixel

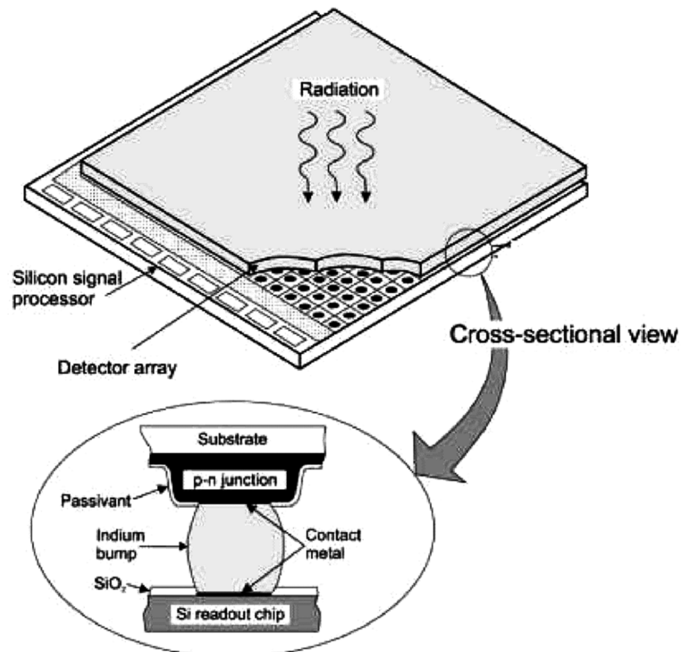

Fig. 2. Generic hybrid FPA with indium bump bonds [7].

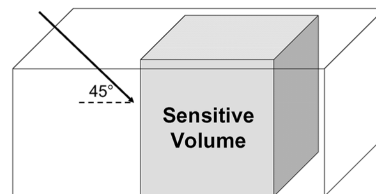

Fig. 3. Structure used to represent one pixel of a silicon p-i-n detector array. The entire structure is made of silicon and the shaded region is sensitive to the proton irradiation.

(pile up). Two non-adjustable parameters are used in post processing the MRED simulations. The first is μ, the mean number

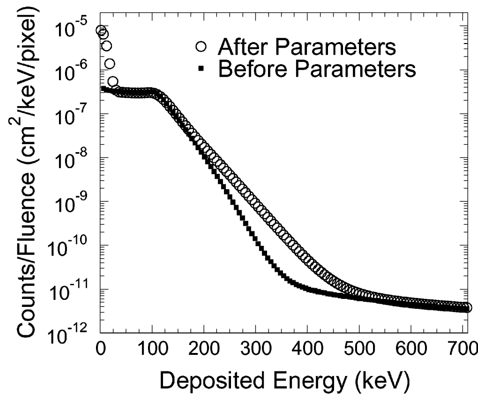

Fig. 4. MRED simulations before and after the effects of pile up and non-radiation-induced noise are applied.

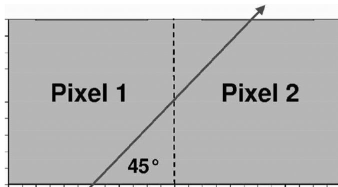

Fig. 5. TCAD structure representing two pixels. Simulations include detailed device parameters.

of proton hits per pixel during a single integration time, and is computed by

$$\mu = \sigma_{\mathrm{sim}} \phi \tau_{\mathrm{int}} \tag{1}$$

where σ_{sim} is the integral cross section of the simulation, ϕ is the experimental flux, and τ_{int} is the experimental integration time. The second parameter is the addition of the non-radiation-induced noise observed in the experimental data. There is an approximately Gaussian broadening of pixels in the zero energy deposition range that represents the amount of system noise present. We applied a Gaussian convolution to the simulation and noise curves to fold the system noise into the simulation.

Fig. 4 compares the differential spectrum of MRED simulations before and after the effects of pile up and the non-radiation-induced noise were included in post-processing of the data. The shape of the sloped region between 125 and 500 keV is affected by the finite number of pixels that receive multiple hits during one integration period. The correction applied is a very general transformation of an arbitrary single-particle spectrum for the case in which the average number of hits per pixel is μ and similar to that described in [12]. The transformation inherently includes multiple hits of all orders, and can be used without numerical difficulty from very low fluxes well into the photon-counting region, where tens or hundreds of particles can hit a pixel in a single integration period. The region of very low energy is affected by the addition of the observed system noise.

B. TCAD Simulations

Technology computer aided design (TCAD) simulations were conducted based on an assumption of pixel structure.

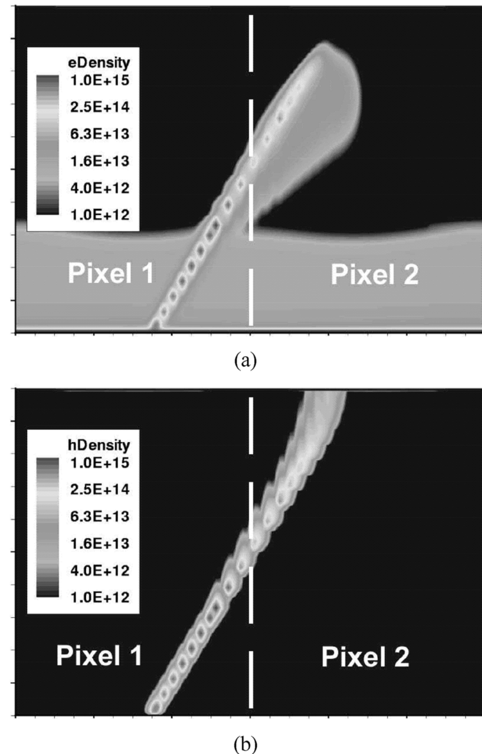

Fig. 6. (a) Electron density and (b) hole density 90 ps after a strike that spans two pixels equally. The motion of charged particles is not only vertical, but along the strike as well.

Fig. 5 shows the TCAD structure used to represent two adjacent pixels. Charge transport and collection within the device was simulated for various strike locations from a 63 MeV proton incident at 45 degrees. For each strike location, approximately 10% less charge was collected on the pixel taking the initial strike, and 10% more charge than expected was collected on the other pixel. The expected collected charge was calculated using a rectangular parallelepiped (RPP) approximation of pathlength and LET.

The motion of electrons and holes can be seen in Fig. 6. Note how the electrons and holes move not only vertically, but along the charge strike as well. This shows that the strike can become a temporary conducting path, causing more charge to collect on the second pixel, as noted above. If the pixels were completely isolated from one another, charge would move only vertically.

Fig. 7 shows the electric field and electrostatic potential 90 ps after a strike that spans two pixels equally. There is a slight disturbance in the electric field where the two pixels meet, but for the most part they stay relatively isolated. There is likewise a slight disturbance in the electrostatic potential, but it is minimal and will restore quickly to equilibrium. Since the effects of charge sharing between pixels is at maximum 10%, it suggests that the RPP assumption is sufficient to estimate the device response for this technology.

IV. Comparison With Experimental Data

In this section, we discuss simulations that mimic the experimental conditions: protons incident at an angle of 45 degrees

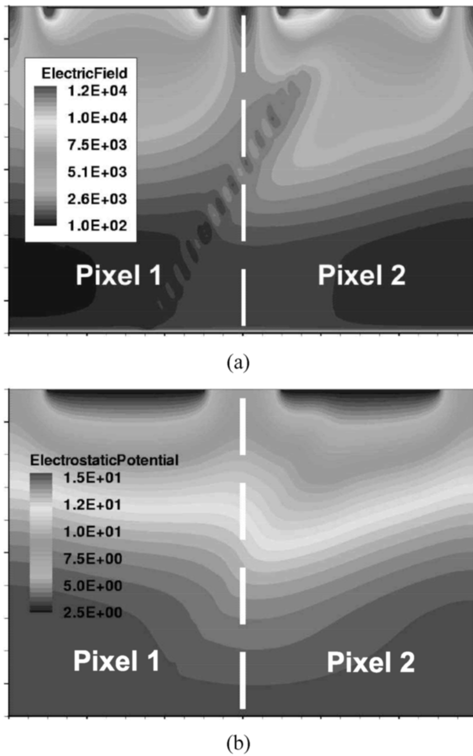

Fig. 7. (a) Electric field and (b) electrostatic potential 90 ps after a strike that spans two pixels equally. The electric field and electrostatic potential are only slightly perturbed suggesting that an RPP approximation for MRED simulations is sufficient for this technology.

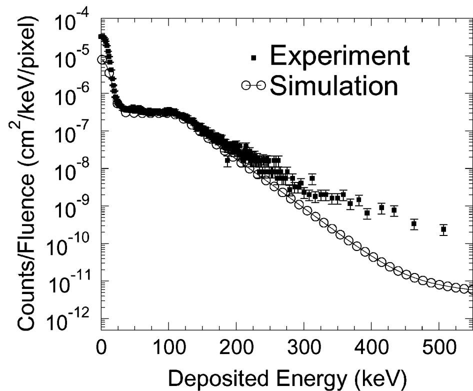

Fig. 8. Differential spectrum of counts per unit fluence per pixel for 63 MeV protons incident on the silicon detector structure from Fig. 3 compared with experimental results. The computed and measured total cross sections agree closely with each other and approximate the geometric cross section.

with energy of 63 MeV. The inclusion of all physical radiation transport processes in the simulation, accounting for pile up, and the inclusion of the measured random noise spectrum provide an accurate description of the experimental data for this device with no adjustable parameters. Fig. 8 shows a differential spectrum of the counts per fluence per pixel as a function of the energy deposited in the sensitive volume, comparing the simulation results with the experimental data. The conversion gain of the experimental data was extracted from the device parameters

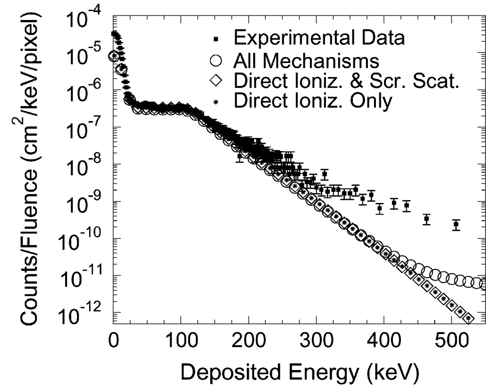

Fig. 9. MRED simulations comparing reaction mechanisms with experimental results. The large open circles represent the simulation of all physics processes available, the open diamonds include direct ionization and screened Rutherford (Coulomb) scattering, and the small stars include only direct ionization. Direct ionization is the dominant mechanism at lower energies, while nuclear reactions dominate at higher energies and screened scattering contributes little as expected.

characterized during device testing. The agreement between the two curves is excellent between 0 and 300 keV.

At higher energies, a few factors are possibly contributing to the difference between the two curves. First, there is an identified issue with the nuclear reaction models used by Geant4 [13]. This systematic error makes it difficult to simulate the sensitive region where nuclear reactions begin to dominate. Another contributing factor is oversimplification of the structure. Secondary particles produced by interactions with materials underneath the pixels may be recoiling back towards the array. These recoils can be lower in energy and highly ionizing. Simulations including the entire pixel array and underlying materials will reveal if these recoils are responsible for the uncertainity in the tail region. All possibilities are actively being researched further.

In Fig. 9, we compare MRED simulations for three situations: inclusion of all physics processes available in the simulation [11], direct ionization and screened Rutherford (Coulomb) scattering only, and direct ionization only with experimental results. At energies below 450 keV, direct ionization dominates the device response. Screened scattering contributes little to the cross section for this structure, as expected for 63 MeV protons since the nuclear stopping power is 2500 times smaller than the electronic stopping power at this energy.

The dashed lines in Fig. 10 represent the expected average and maximum energy deposited in the structure from a constant-LET and path length distribution calculation. The dashed line labeled “Avg” is the energy deposited along an average path length through one pixel, and the dashed line labeled “Max” is the energy deposited along a maximum path length. The maximum amount of energy deposited in the structure via this calculation is approximately 130 keV. Based on a constant LET analysis, no events are considered that deposit energy greater than this value. Therefore, a constant LET model does not describe the shape of the curve above 130 keV. The constant LET approximation considers only direct ionization, which is the dominant mechanism, but a path length analysis can only address averages while even primary ionization has fluctuations.

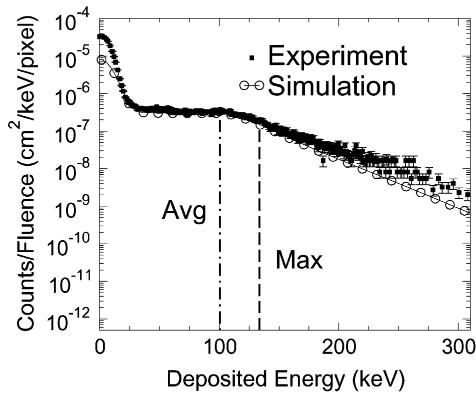

Fig. 10. Differential spectrum comparing the simulation results with experimental data and a constant LET path length calculation. The path length calculation does not predict the occurrence of large energy depositions.

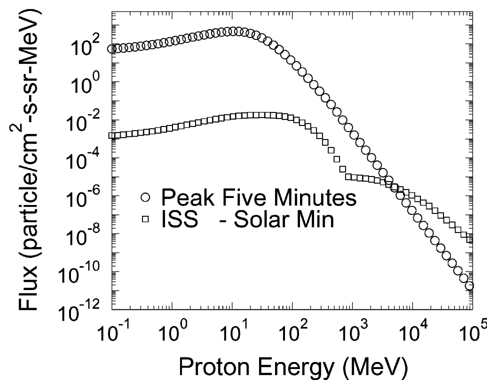

Fig. 11. Proton environments calculated using CREME96 [14]. The "GEO" curve is for the peak five minutes in geosynchronous orbit and "ISS" is for space station orbit using ap8min for solarmin.

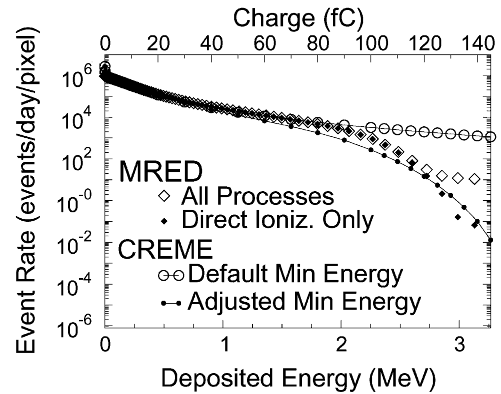

Fig. 12. Simulation results of the expected event rate from geosynchronous peak five minute proton environment in Fig. 11 through the pixel structure. Direct ionization dominates below 2.75 MeV (125f C). To accurately predict the event rate at higher energies using CREME96, the minimum energy in the LET spectrum must be properly adjusted.

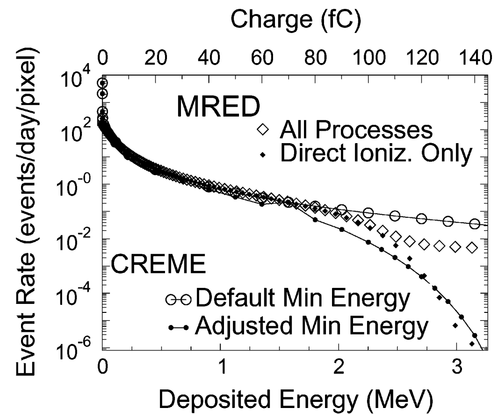

Fig. 13. Simulation results of the expected event rate from ISS orbit solar min proton environment in Fig. 11 through the pixel structure. As expected, the event rate is several orders of magnitude lower than the expected geosynchronous rates, but once again, incorrect adjustment of the CREME96 parameters could result in an over prediction of event rate.

V. Event Rate Predictions From Space Proton Fluxes

In this section, we consider the event rate for proton environments computed using MRED and compare these results to CREME96. For this calculation, simulations were done with an omnidirectional ion fluence. Fig. 11 shows the environment models used in the calculations in this section. The curves were computed using CREME96 [14]. The curve labeled "GEO" is for the peak five minutes in geosynchronous orbit while the "ISS" curve represents the international space station orbit using ap8min [15] for solarmin.

Fig. 12 presents the integrated event rate in events per pixel per day as a function of deposited energy for the peak five minutes in the geosynchronous orbit proton environment. MRED simulations show that when the full proton spectrum is considered, direct ionization dominates at energies below 2.75 MeV (125 fC). Fig. 12 also presents event rate calculations done with CREME96, which only consider direct ionization. At energies below 1.75 MeV (80 fC), there is good agreement between the MRED simulations and the CREME96 results. However, if the default value for the minimum energy in the LET spectrum of 0.1 MeV/nuc is used in the CREME96 calculation, the event rate is overestimated by as much as four orders of magnitude at higher energies. This overestimation is due to the limited range of protons in large silicon volumes, which is not considered by the CREME calculation. This is noted on CREME96's website and its authors suggest this parameter be adjusted for certain SEU applications [14]. When a minimum energy value of 1.25 MeV/nuc is used in the CREME96 calculation, the event rate is comparable to the event rate obtained through MRED simulations. This value was obtained by fitting to the MRED simulations. So for applications in the low energy regime, such as those used for ground testing, CREME96 is a good predictor of device response. However, at higher energies expected in space, a high fidelity simulation is needed to avoid overestimating the event rate by not properly adjusting the minimum energy at which ions should be tracked.

When the same calculation is done for the international space station orbit, again we find that below 2.5 MeV, the rate is dominated by direct ionization, as in Fig. 13. As expected, due to lower proton fluxes, the event rate is several orders of magnitude lower than the geosynchronous rate. The default CREME96 parameters again overestimate the event cross section by several orders of magnitude unless the minimum energy parameter is adjusted to 1.25 MeV/nuc. A high fidelity simulation done with MRED predicts the event rate intrinsically.

VI. Conclusion

We have shown the effects of individual mechanisms on spectral shape that can be separated and studied individually. Through Monte Carlo based simulation, we show that direct ionization is the dominant mechanism for energy deposition below 300 keV in the focal plane detector considered here, while nuclear reactions dominate at higher energies and screened Rutherford scattering contributes very little. Even though direct ionization is the dominant mechanism, a constant LET and path length calculation does not address the fluctuations in *dE/dx*, only the variation in path length, and therefore does not capture the shape of the differential distribution. The methodology used in this paper can be extended to predict the implications of a full space proton flux. A high fidelity simulation is needed to accurately predict the device response at higher energies.

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Comparison of Measured Dark Current Distributions With Calculated Damage Energy Distributions in HgCdTe

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***Abstract*—This paper presents a combined Monte Carlo and analytic approach to the calculation of the pixel-to-pixel distribution of proton-induced damage in a HgCdTe sensor array and compares the results to measured dark current distributions after damage by 63 MeV protons. The moments of the Coulombic, nuclear elastic and nuclear inelastic damage distributions were extracted from Monte Carlo simulations and combined to form a damage distribution using the analytic techniques first described by Marshall *et al.* The calculations show that the high energy recoils from the nuclear inelastic reactions (calculated using the Monte Carlo code MCNPX) produce a pronounced skewing of the damage energy distribution. While the nuclear elastic component (also calculated using the MCNPX) contributes only a small fraction of the total nonionizing damage energy, its inclusion in the shape of the damage across the array is significant. The Coulombic contribution was calculated using the Monte Carlo radiative energy desposition (MRED), a Geant4 application. The comparison with the dark current distribution strongly suggests that mechanisms which are not linearly correlated with nonionizing damage produced according to collision kinematics are responsible for the observed dark current increases. This has important implications for the process of predicting the on-orbit dark current response of the HgCdTe sensor array.**

***Index Terms*—CCD, dark current distribution, GEANT4, HgCdTe, proton effects.**

I. Introduction

MANY emerging space astronomy programs will perform their science using infrared detectors in order to study the early Universe as well as Earth and planetary sciences, and the infrared bands are also important in other civil and military applications. Although we have observed hot pixel formation in proton-irradiated Rockwell IR hybrid detectors to be used in the James Webb Space Telescope (JWST) [8], we do not as yet understand the mechanism producing the hot pixels in HgCdTe. As a result we are unable to predict hot pixel formation on orbit. The purpose of this paper is to predict the proton-induced displacement damage distributions in $Hg_{0.7}Cd_{0.3}Te$ detector arrays based on collision kinematics in order to see if they predict the observed dark current distribution.

In the case of Si sensors (including charge couple devices, active pixel sensors, and charge injection devices), measurements show that the dark current distributions are often well explained by the damage distributions calculated based on collision kinematics [1], [9]–[12]. Damage distributions were first calculated analytically by Marshall *et al.* [1] in 1990 with good agreement obtained for dark current distributions produced by 12 MeV protons in Si charge injection devices. At 63 MeV the data indicated less variance in the measured distribution than in the damage energy calculation, a result also found by Hopkinson *et al.* [9] at 100 MeV in Si charge coupled devices (CCDs). Using the Monte Carlo code CUPID [13], Dale *et al.* showed that this result followed because the recoil ranges were comparable to the size of the dark current sensitive volume. In the limit of bulk material, both the analytic and the CUPID Monte Carlo approaches are in good agreement. As sensitive volumes shrink and incident proton energies increase, the ranges of the spallation recoil fragments approach the smallest dimension of the microvolume, and the pixel-to-pixel damage variance are best calculated using methods which track the damage deposition along the recoil atom pathlengths. In this regime, a Monte Carlo approach is well suited to describe the damage energy distribution.

Nevertheless, in some cases, the Si dark current distributions cannot be described using collision kinematics alone. This has been attributed to hot pixel formation from electric field enhanced emission (e.g., [11], [14]–[17]). It is important to distinguish the two scenarios because in order to predict the hot pixel populations and assess dark signal nonuniformity, one needs to understand whether the underlying mechanisms are due to extraordinarily large damage regions from inelastic reactions in the pixel or by more ordinary damage in the presence of electric field enhanced emission which appears to follow from small damage regions in very small microvolumes filling only a tiny fraction of the pixel's volume. In the later case, the hot pixel population may be expected to follow the Coulomb cross section [14], [17].

II. The Experiment

We use a previously measured dark current distribution of a Rockwell H2RG which is a hybrid device with a 2k $\times$ 2k format and 18 μm pixel pitch. It incorporates a software configurable silicon readout circuit bump bonded to an HgCdTe detector array optimized for the JWST NIR (0.6–5.5 μm) spectral

Manuscript received October 3, 2006; revised January 26, 2007. The authors appreciate funding from the NASA Electronics and Packaging Program (NEPP), the DTRA Radiation Hardened Microelectronics Program, and the James Web Space Telescope project.

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Digital Object Identifier 10.1109/TNS.2007.895804

0018-9499/$25.00 © 2007 IEEE

range. Details of the experiment can be found in [8] but key details are provided here.

An engineering grade device was employed and displayed a number of cosmetic defects and 'hot' pixels that did not meet the stringent JWST flight focal plane array (FPA) operability requirements going into our test. A subset of ~266 000 pixels were extracted that were deemed to be "good" pixels as will be described in the next paragraph. The detector was held at 37 K and irradiated with 63 MeV protons to a 5 krad(Si) level which corresponds to a fluence of 3.7×10^{10} cm^{-2}. The dewar was maintained at temperature while being transported from the UC Davis Crocker Nuclear Laboratory back to the NASA Ames Laboratory, and measurements were taken after residual radioactivity from the proton exposure had mostly decayed. Residual activity and cosmic ray effects were filtered out as described in [8].

As noted in [8], because of the very low dark current levels in these devices, the number of "good" pixels was difficult to precisely quantify in the presence of read noise, cosmic-ray events and induced radioactivity in the cryostat. In order to isolate and remove engineering defects from the test data, a long series of darks was obtained in a clear environment with each device prior to the proton exposure. The distribution of dark currents estimated from the longest integration for each sensor chip assembly (SCA) was examined to determine the width of the peak in the histogram and thus the accuracy to which we Could estimate dark current in these devices. This distribution width arises from a combination of system read noise and the true non-uniformity in dark current among the best pixels in the device. From the observed distributions it appeared that read noise was the greatest contributor to this width for each test SCA. We chose to set a dark current threshold for each long-integration frame in the dark current series at the median-pixel dark current plus the distribution width of the longest integration frame, as given by its full-width at half-maximum. By applying this threshold in each of the long-integration frames and removing from our select population any pixels that exceed the threshold in any of the frames, we derived a subpopulation of pixels that never exceed the dark current threshold over many hours of data collection. Postirradiation data reduction is limited to this very conservative subpopulation of selected pixels. Note that this method is guaranteed to misidentify a number of good pixels as bad, since it makes no attempt to correct for the effects of cosmic ray events that occur during the long integration series, and because read noise will occasionally push marginally good pixels above the threshold. We consider this is not a problem in this work as we still had a sufficient population of pixels remaining to study the dark current distributions.

III. Damage Energy Distribution Calculations

In this section we follow the method described in [1] for Si, but with modifications, to calculate the damage energy distribution for 63 MeV protons on $Hg_{0.7}$ $Cd_{0.3}Te$. The first step in the calculation of damage energy distributions is to calculate the interaction cross sections (σ), as well as the mean damage energy, (μ) and the associated variance, (σ^2) of the $Hg_{0.7}Cd_{0.3}Te$ damage energy distributions due to Coulombic, nuclear elastic and nuclear inelastic interactions respectively. These means and variances correspond to the probability density function (pdf) governing the likelihood of a particular recoil energy resulting from a given proton/$Hg_{0.7}Cd_{0.3}Te$ interaction.

TABLE I

Proton Energy (MeV)	Cross Section (barns)	Mean Recoil Energy (MeV)	Mean Damage Energy (MeV)	Variance of Damage Energy (MeV)^2
Nuclear Elastic Reactions				
63	1.566	0.0367	0.0236	5.56 x 10^3
Nuclear Inelastic Reactions				
63	1.599	0.365	0.204	2.87 x 10^2
Coulombic Interactions				
63			0.734*	9.60 x 10^{13}**

*MeV per pixel with incident 63 MeV proton fluence of 3.7 x 10^{10} cm^{-2}.
** MeV^2 per pixel with a 63 MeV proton fluence of 3.7 x 10^{10} cm^{-2}.

Underlying assumptions include the fact that interaction mechanisms are random in nature, and for our purpose of examining the possible correlation of device dark current with displacement damage, we consider all non-ionizing energy; as with the related nonionizing energy loss (NIEL) energy deposition rate. To achieve this, we use the Lindhard partition [18] as applied to the calculated recoil energy for a given ion and energy. We considered that the nonionizing energy associated with a recoil atom was deposited in the pixel in which it originated. In the next section we describe how the damage energy contributions from Coulomb scattering, nuclear elastic scattering, and nuclear inelastic scattering are determined, and show that each mechanism has its own pdf describing the probability of an individual pixel receiving a given amount of damage. As the three mechanisms are independent, we then show how relatively straight forward statistical tools can combine these pdf's in order to describe the damage distribution throughout the array; taking into account the pixel geometry, material composition, proton energy and proton fluence. Our treatment exercises these tools for the case of comparing a measured dark current distribution with a predicted damage energy distribution to test the hypothesis that there may be a linear correlation.

A. Material and Recoil Spectrum Parameters

The $Hg_{0.7}Cd_{0.3}Te$ has a density of 7.41 g/cm^3 and a gram molecular weight of 151 g. The JWST H2RG pixel area is 18 μm by 18 μm and the HgCdTe layer is ~10 μm thick. From measurements on other HgCdTe detectors we expect the diffusion length to be at least 10 μm, so dark current should be collected from the entire pixel volume, even though the diode junction occupies a small fraction (~10%) of the pixel volume. In this geometry, the volume and density are large enough so that we do not expect the ranges of the recoils to be long compared to the volume dimensions so the analytic approach should offer a valid approximation.

The results for the recoil spectrum parameters are shown in Table I, along with the Monte Carlo radiative energy deposition

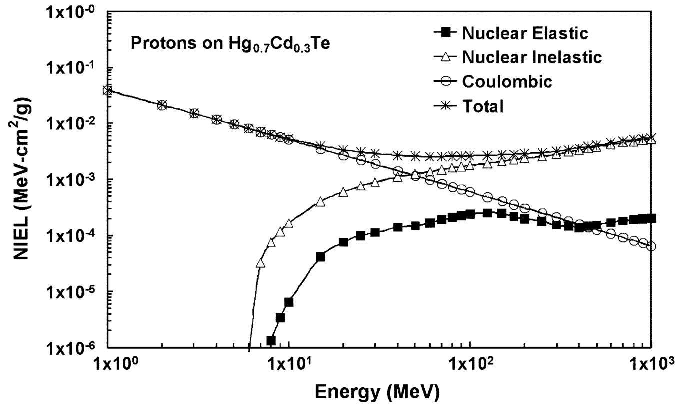

Fig. 1. Proton NIEL in $Hg_{0.7}Cd_{0.3}Te$ as calculated in [21]. Note that the NIEL is very insensitive to the exact stoichiometry.

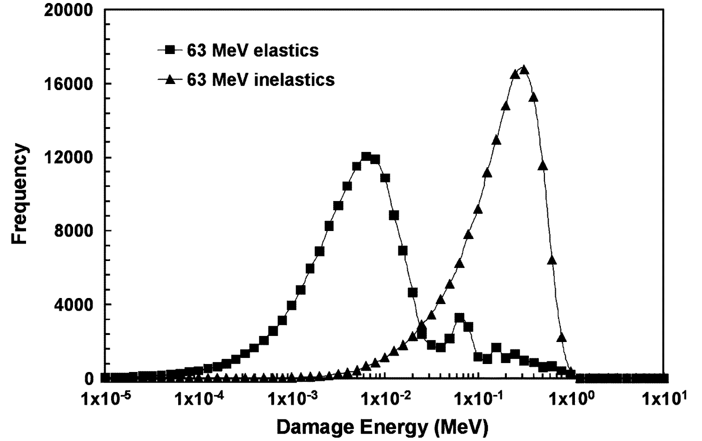

Fig. 2. Comparison of the damage energy distributions for the nuclear elastic and nuclear inelastic interactions at 63 MeV. Note the abscissa is on a log scale to represent the two distributions on the same figure.

(MRED) [3]–[5] results for the Coulomb parameters in the units indicated. MRED is a Geant4-based tool that employs a shielded Coulomb potential. In the future, we plan to develop MRED for a more comprehensive and general solution but for now we are using it for a "point" solution for the case of 3.7×10^{10} cm^{-2} 63 MeV protons on the pixel geometry cited (i.e., 1.2×10^5 protons/pixel). This proton exposure results in 5 krad(Si).

We arrived at the distribution describing Coulomb damage based on the mean damage energy deposited in a large number of Monte Carlo runs (using MRED [3]–[5]) for the pixel geometry and proton fluence of 3.7×10^{10} cm^{-2} 63 MeV protons. Using 100 separate simulations of the mean damage, we calculated the sample mean presented in the Table. It is interesting to note that the mean damage energy per pixel calculated using the NIEL value in Fig. 1 (based on the analytic Ziegler–Biersack–Littmark (ZBL) method [20]) agrees to within 17% with the value obtained using the MRED Monte Carlo runs.

Calculation of the sample variance for the 100 simulations yields the surprisingly small value listed in Table I. Note that each simulation incorporated a new random number seed, and each case was run for exactly 1.20×10^5 protons/pixel. Consideration of our test condition and inclusion of the variance associated with the Poisson probability describing the incident particle fluence associated with an average of 1.2×10^5 protons/pixel yields a much larger variance of 4.49×10^{-6} MeV^2. The variance used in the following calculations is therefore very heavily dominated by this Poisson contribution, and for such a large incident fluence we have confidence in assuming a Gaussian form for the distribution of Coulomb damage throughout the array. Inspection of the variance indicates very little difference in the Coulomb damage from pixel to pixel. This follows from the fact that the mean energy imparted per Coulomb scattering event is on the order of the displacement threshold ($\sim$20 eV), and this results in the generation of isolated Frenkel pairs (and possibly point defects in HgCdTe). So the Coulomb damage is spread very evenly throughout a pixel and hence the pixel-to-pixel uniformity is expected. This parallels the treatment of proton damage from Coulomb scattering in Si in ([19] and [20] and references therein).

The nuclear elastic component (calculated using the Monte Carlo code MCNPX [2]) has an almost negligible effect on the NIEL (Fig. 1) as it is typically an order of magnitude below the dominant term across the entire energy range. But as we will demonstrate later, consideration of the nuclear elastic contributions has important consequences for the shape of the composite damage distribution. We can see from the table that the mean recoil energy and variance are an order of magnitude below that of the inelastic interactions, but their cross sections are essentially equal. The difference in damage energies per event gives rise to the lower NIEL relative to the nuclear inelastic events, and this is also illustrated in Fig. 2 which shows the comparison of damage energy distributions for nuclear events generated in the MCNPX calculations.

The method used to compute the nuclear contribution to NIEL and the associated variance is based on the thin target approximation using MCNPX and a methodology developed by Jun [22]. A thin cylindrical disc of the material of interest with a normalized density of 0.01 atoms/barn-cm was modeled, and a simulated pencil beam of protons penetrates the material. Using the damage energy tally, the history tape written by MCNPX was analyzed to calculate the mean damage energy per source particle, $T_{\rm dam}$, which is the nonionzing portion of energy deposited (i.e., after application of the Lindhard partition function). Then, NIEL is calculated by

$$S_{\rm NIEL} = \left(\frac{N_A}{A}\right)\frac{T_{\rm dam}}{(N_v \cdot x)} \qquad (1)$$

where N_A is Avogadro's number, A is the gram atomic weight of the target material, N_v is the atom density and x is the target thickness. By using MCNPX, we were able to compute the nuclear contributions to the proton NIEL for each material and then superimpose them to arrive at the NIEL for the $Hg_{0.7}Cd_{0.3}Te$. The production of displaced atoms is dominated by the Coulombic interactions below 10 MeV, while the nuclear collisions (particularly the nuclear inelastic) take over at energies exceeding $\sim$50 MeV. For the Coulombic NIEL shown in Fig. 1, the calculation was done analytically using the ZBL method. This analytic approach provides the mean, but as previously mentioned the MRED calculations were necessary

to determine the variance for Coulomb scattering events. Mean values and their variances for nuclear elastic and inelastic damage distributions were determined using the history tape out of MCNPX for the distributions shown in Fig. 2, and later we refer to these as the moments of the single event probability density functions for describing nuclear collision damage.

B. Calculated Damage Distributions

The cross sections for nuclear scattering events to produce damage listed in Table I, combined with the proton fluence chosen to represent a relevant JWST mission exposure, result in only a few events in the H2RG pixel volume. We define η as the average number of recoils per pixel and it is given by

$$\eta = \sigma \cdot \Phi \cdot \rho \cdot V_{\text{pixel}} \cdot N_A / A \tag{2}$$

where σ is the interaction cross section, Φ is the proton fluence, ρ is the HgCdTe density, V is the pixel volume, N_A is Avogadro's number, and A is the gram molecular weight of $Hg_{0.7}Cd_{0.3}Te$. We find that the average number of nuclear elastic and inelastic recoils per pixel is 5.7 and 5.8 respectively, and the maximum number of events expected for any pixel is ~20 for our pixel population. Also note that only ~800 pixels out of ~266 000 have no nuclear elastic interactions, and similarly ~800 pixels have no inelastic collisions. As these are independent variables, the population of pixels having only Coulomb damage is given by the product of the Poisson probability of no nuclear elastics and the probability of no nuclear inelastics which yields only ~2 pixels! From this we see that even though the total damage from nuclear elastic processes in small, the consideration of this damage is very important in arriving at the appropriate distribution describing pixels with no nuclear inelastic collisions, essentially adding to the tail of the Coulombic contribution thereby increasing the variance. Obviously where nuclear inelastic collisions are present, their importance in the damage of a given pixel plays a dominant role.

Since the damage from Coulombic, nuclear elastic and nuclear inelastic events are each independent and random variables, the statistical description of the cumulative damage can be approached by evaluating them independently and then combining by convolution. The functional form of the Coulomb portion is Gaussian arising from the fact that each pixel has a very large number of relatively small collisions. Inspection of the functional form of the damage distributions of Fig. 2 reveals an asymmetric distribution which is skewed towards higher energies (note the abscissa is on a log scale to represent the two distributions on the same figure). After considering several candidate distributions, we determined that the two parameter gamma function is well suited for describing both the nuclear elastic and nuclear inelastic damage functions (as in [1]). The gamma function is expressed as $\Gamma(\mu^* \lambda)$, where μ is the mean recoil energy and $\lambda = \mu/\sigma^2$, where σ^2 is the associated variance. This result affords a very convenient approach for the techniques we use to combine distributions in that the convolution of two gamma functions yields a new gamma function. This fact, along with the result that distribution means and variances add linearly under convolution, affords a concise approach to this analytic technique. In addition, since the Gaussian function is a special case

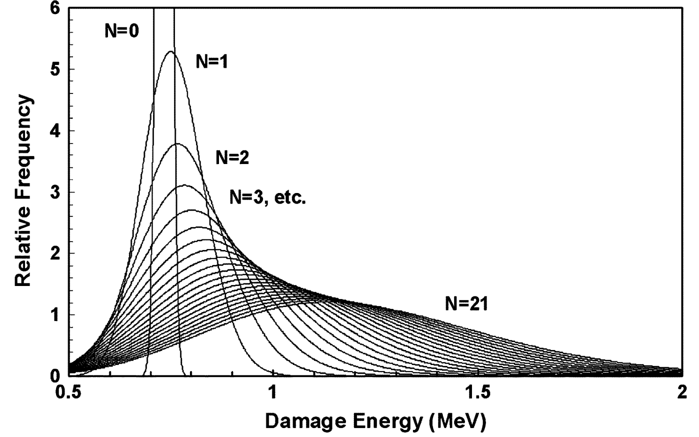

Fig. 3. Total elastic pdf's for a pixel with $N = 0, 1, 2, \ldots 21$ nuclear elastic interactions. [The $N = 0$ (Coulombic interactions only) is a Gaussian curve with a maximum value of 29.5.]

of the gamma function, their combination under convolution results in a gamma function and this result means we have a simplified path to combining all three independent variables without requiring FFT-based convolution methods.

Using the technique just described, we proceed to combine Coulombic damage with the single event probability function (SEpdf) for elastic nuclear reactions. This step reduces to defining a new probability density function based on the gamma function (with added means and variances) as shown in equation below. The probability (P) of having the damage energy (DE) is

$$P(\text{DE}) = \frac{\lambda}{(\lambda \cdot \text{DE})^{1-r}} \cdot \frac{e^{(\lambda \cdot \text{DE})}}{\Gamma(r)} \tag{3}$$

where and $\lambda = \mu/\sigma^2$ and $\mathrm{r} = \mu^2/\sigma^2$. (This function is also normalized to unit area.) For convenience, we note that a gamma function is defined as

$$\Gamma(\alpha) = \int_0^\infty x^{(\alpha-1)} \cdot e^{-x} dx \tag{4}$$

where $\alpha > 0$ and x is the independent variable. For example, the damage probability function (3) applies to pixels that have Coulombic damage and only 1 nuclear elastic recoil for which μ is the sum of the Coulombic mean damage energy and the mean damage energy for one elastic recoil, and likewise, σ^2 is the sum of the Coulomb variance and the variance for one nuclear elastic recoil. By extension we generate a family of gamma distributions accounting for pixels with multiple nuclear elastic recoils by examining the N-fold convolution of the SEpdf with itself to get the pdf for a pixel with N elastic recoils. This is done for $N = 2, 3, 4$, etc., up to the maximum $N = 19$ events expected to occur for the given population of pixels. The resulting total elastic (combined Coulomb plus nuclear elastic) pdf's for a pixel with N nuclear elastic recoils is shown in Fig. 3. Note that as N increases the mean of the distribution increases, it broadens and also tends towards a Gaussian—all expected based on the Central Limit Theorem.

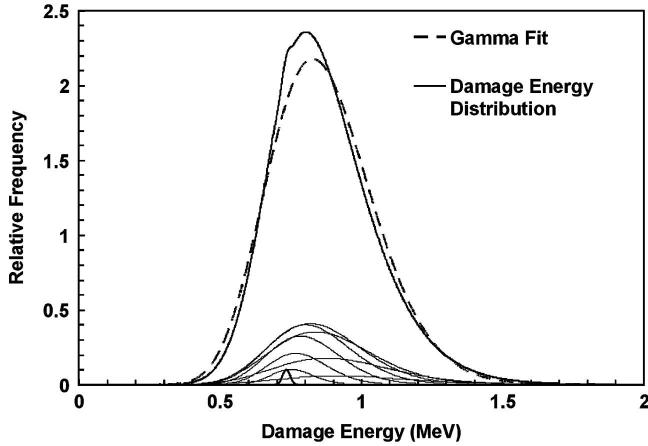

Fig. 4. Comparison of the combined elastic damage energy distribution and a gamma function with the same mean and variance. The distributions underneath the two curves are the Poisson weighted gamma distributions from Fig. 3 for pixels with N nuclear elastic recoils which are summed to arrive at the total elastic damage energy distribution. For clarity only $N = 0-6, 8, 10$ are shown. Note the reduced variance for the $N = 0$ (Coulomb only) case. Recall that the average number of nuclear elastics is 5.7.

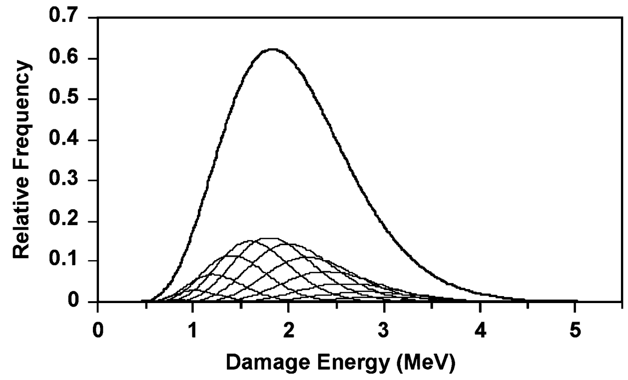

Fig. 5. Calculated damage energy distribution for 266 000 $Hg_{0.7}Cd_{0.3}Te$ pixels irradiated with 3.7×10^{10} cm^{-2} 63 MeV protons. Below the summed damage distribution we show the Poisson weighted damage distributions for the pixels with only elastic events (left most peak barely visible in figure), and the pixels with elastic events plus 1 (left peak with maximum at $\sim$1 MeV),2, 3 . . . 18 inelastic interactions per pixel. (Note that a pixel may contain up to 18 inelastic interactions though only distributions with up to 10 are resolved in the plot.)

For the sensitive volumes (V_{pixel}) and fluence (Φ) of interest, the variation in the number of nuclear elastic (or inelastic) recoils per pixel is described by a discrete Poisson distribution in which the probability P is

$$P(x, \eta) = \frac{(e^{-\eta} \bullet \eta^x)}{x!} \quad (5)$$

where x $= 0, 1, 2, \ldots$ recoils per pixel and η is the average number determined according to (2). Using this relation, we weight each of the 19 gamma distributions with the Poisson probability for x (nuclear elastic) recoils in a pixel and then sum them to arrive at the combined Coulomb and nuclear elastic (which we will refer to as the combined elastic) damage energy distribution across the array. Note that $\sum P(x, \eta) = 1$.

In Fig. 4, we present the Poisson weighted pdf's as well as the sum in graphical form, and using standard statistical techniques we calculate the mean and variance of this resulting combined elastic function to be 0.87 MeV and 0.19 MeV^2. Note that the Poisson weighting and superposition results in a functional form which is not described exactly by a gamma function, but due to the ease of working with gamma distributions for the next step of the analysis to incorporate nuclear inelastic damage, we approximate the resulting combined elastic distribution with a gamma function having the same mean and variance. This function is also shown in Fig. 4. The comparison shows a reasonably good fit, and we consider the tradeoffs associated with this assumption to favor this approximation.

Note that the variance in the combined elastic damage is four orders of magnitude greater than the Poisson dominated Coulomb only case. Even though nuclear elastic collisions impart only a small fraction of the total NIEL, their inclusion in the population of pixels in the array ($\sim$800 total) which have no inelastic damage is necessary.

Fig. 1 and Table I reveal the important implications of the nuclear inelastic damage in that it accounts for >60% of the total damage at 63 MeV, and with an average of 5.8 events per pixel the variation from pixel-to-pixel is obviously the most significant aspect of the distribution of damage throughout the array. Using the techniques already described, we combine the N-fold convolution of up to 20 inelastic events per pixel with the gamma function describing the combined elastic damage and apply Poisson weighting per (4) and finally perform the summation of all the Poisson weighted distributions.

The calculated damage distribution is shown in Fig. 5, which shows the distribution of pixels with elastic damage plus 0, 1, 2, etc. inelastic interactions underneath the sum of each contribution. The average number of inelastic collisions per pixel was $\sim$5, and the maximum number of inelastic recoils expected per pixels is 20 for our fluence and pixel population. As one can see, skewness in the distribution is primarily attributed to the Poisson weighting of the inelastic interactions. This function describes the distribution of damage corresponding to our proton-induced dark current distribution. Note that the shape assumed for the SEpdf's (gamma functions in our case) is not very critical.

It is interesting to compare the damage distribution calculated for a high atomic number compound such as HgCdTe with the previous Si result [1]. In HgCdTe the effect of the inelastics is much more prominent—a higher mean energy and a broader peak with a more pronounced tail is observed because the inelastic cross section is 3 times larger, the mean recoil damage energy is 30% higher and the variance is an order of magnitude larger in HgCdTe as compared to Si.

IV. Comparison of Damage Distribution With Dark Current Histogram

The measured dark current histogram for 266 000 selected pixels is shown in Fig. 6 along with the pre-irradiation histogram. In [8], the slight median shift was not investigated, and hence was not presented as necessarily real. However, we have reanalyzed this data and do find a small shift in the median dark current after irradiation to 3.7×10^{10} cm^{-2} 63 MeV protons as indicated in the figure. It is apparent in Fig. 7 that the calculated damage distribution does not predict the measured dark current distribution which indicates that some other mechanism than collision kinematics is also responsible for the high dark

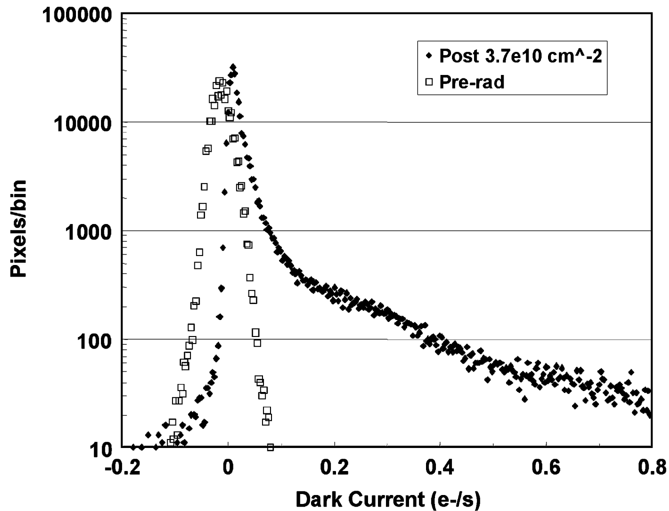

Fig. 6. Measured dark current distribution for 266 000 $Hg_{0.7}Cd_{0.3}Te$ pixels before irradiation and after irradiation with 3.7×10^{10} cm^{-2} 63 MeV protons. The data represent measured absolute values and the negative numbers reflect measurement noise in the system. The mean dark current is extremely small.

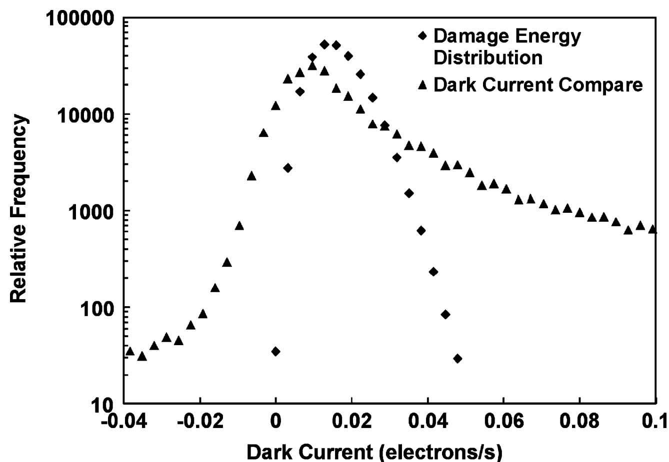

Fig. 7. Comparison of measured dark current histogram with damage energy calculation. The high dark current pixels are not the result of collision kinematics.

current pixels seen in the data. This makes an on-orbit prediction of the dark current based on proton results at a single energy (63 MeV in our case) problematic since the nonionizing energy loss rate (NIEL) correlation does not appear to hold. Measurements at 8 MeV are planned to see if the high dark current pixels correlate with the Coulombic portion of the NIEL which would be the case if electric field enhanced emission via trap-assisted tunneling is responsible as has been seen in Si. (Trap-assisted tunneling is known to be important in HgCdTe sensors at low temperatures.) If this is also the case with the present HgCdTe array then first order estimates of hot pixel rates expected on-orbit which are based on dark current histograms for the 63 MeV equivalent fluence for a given mission will underestimate the number of hot pixels.

V. Discussion and Summary

In comparison to earlier analytic damage energy distribution predictions (e.g., [1]), we find that the role of the inelastics in producing the highly damaged pixels is even more dominant for the HgCdTe case as compared to Si. The cross section for inelastic interactions is larger in the (higher atomic number system) HgCdTe by a factor of three and the variance is an order of magnitude larger in HgCdTe.

We have developed a new combined Monte Carlo and analytic approach to the calculation of the pixel-to-pixel distribution of proton-induced damage in a HgCdTe sensor array and compared the results to measured dark current distributions after damage by 63 MeV protons. The moments of the Coulombic, nuclear elastic and nuclear inelastic damage distributions were extracted from Monte Carlo simulations and used to generate single event probability distributions describing each class of proton/HgCdTe interaction. These were combined as discussed in the text to form a damage energy distribution. The calculations show that the high energy recoils from the nuclear inelastic reactions (calculated using the Monte Carlo code MCNPX [2]) produce a pronounced skewing of the damage energy distribution. While the nuclear elastic component (also calculated using the MCNPX) contributes only a small fraction of the total nonionizing damage energy, its inclusion in the shape of the damage across the array is significant because its variance dominates in those pixels with no inelastic reactions. The Coulombic contribution was calculated using MRED [3]–[5], a Geant4 [4], [6] application. We noted that only two pixels in the entire array have only Coulombic interactions. The comparison with the 63 MeV proton-induced dark current distribution strongly suggests that mechanisms which are not linearly correlated with nonionizing damage produced according to collision kinematics are responsible for the high dark current pixels. Measurements at 8 MeV are planned to see if the high dark current pixels correspond to the Coulombic portion of the NIEL which would be the case if electric field enhanced emission is responsible as has been seen in Si. The technique for describing the damage energy distributions is extendable to other proton energies, material systems, and pixel geometries.

Acknowledgment

The authors would like to thank J. Hubbs from Ball Aerospace for useful discussions.

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