Cadence Tutorial

EECE 285 VLSI

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Purpose of Cadence

1) Cadence is an Electronic Design Automation (EDA) environment in which different applications and tools can are integrated together. This allows all the stages of IC design and verification to be done in a single environment. The different tools are supported by different fabrication technologies allowing for customization of the Cadence environment to fit the particular technology.

Linux

1) Linux is an operating system that is a multi-user, multi-tasking system that can be used on servers, desktops and laptops. Linux was originally developed at Bell Labs in 1969. Linux is used to access cadence and manage the files in its libraries.
2) Basic Linux commands used for running cadence
   A) Command: ls
      Function: lists the files in the current directory
      Example: ls
   B) Command: pwd
      Function: tells you what directory you are currently in
      Example: pwd
   C) Command: mkdir
      Function: makes a new directory
      Example: mkdir project (makes a new directory called project)
   D) Command: cd
      Function: takes into the specified directory
      Example: cd NCSU_AMI06 (takes you into the directory called NCSU_AMI06)
   E) Command: cd ..
      Function: takes you back one directory
      Example: cd ..
   F) Command: mv
      Function: moves a directory to the specified location
      Example: mv adder adder2 (moves the directory adder to the current directory and changes the name to adder2)
   G) Command: cp
      Function: copies a file
      Example: cp ../multi . (copies the file named multi from the previous directory to the current directory)
   H) Command: gzip
      Function: compresses files, so they take up less space
      Example: gzip inv (compresses the file called inv)
   I) Command: gunzip
      Function: uncompresses files that have been compressed by the command gzip

Example: gunzip inv.gz (uncompresses the file named inv.gz)

J) Command: chmod
Function: changes the read, write and execute permissions on the files
Example: chmod nand (lets you change the read, write and execute permission for the file named nand)

K) Command: rm
Function: removes a file
Example: rm nor.zip (removes the file named nor.zip)

L) Command: diff
Function: compares two files and shows their differences
Example: diff or and (compares the files called or and and showing their differences)

M) Command: clear
Function: clears the screen
Example: clear

N) Command: tar -cvf
Function: combines many files or directories into one file
Example: tar –cvf homework3.tar layout schematic symbol (combines the directories names layout, schematics and symbol into one and names it homework3.tar)

O) Command: rmdir
Function: removes a directory that is empty
Example: rmdir pad (removes the directory called pad)

P) Command: zip
Function: zips up a file
Example: zip add lock (zips up the file named add and saves it as lock.zip)

Q) Command: --help
Function: Tells you the function of a command
Example: chmod –help (tells you the function of the command chmod)

R) Command: zip –r
Function: zips up a directory
Example: zip –r Bickham_HW4 Bickham_HW4 (zips up the directory named Bickham_HW4 and saves it as Bickham_HW4.zip)

S) Command: unzip
Function: unzips a file that has been zipped up by the zip command (ends in .zip)
Example: unzip Homework4.zip (unzips the file named Homework4.zip)

T) Command: tar –xvf
Function: separates files or directories that have been combined by the tar –cvf command
Example: tar –xvf Homework1.tar (separates the directories and files that have are combined in the Homework1.tar file)

U) Command: rm –r
Function: removes a directory and its contents

Example: rm –r nor (removes the directory called nor and all of its contents

V) Command: cp –r
Function: copies a directory and all of its contents
Example: cp –r HW5 (copies the directory called HW5 and all of its contents)

W) Command: history
Function: shows the list of the last 100 commands
Example: history

X) Command: find
Function: searches the current directory and all subdirectories for the specified file(s)
Example: find project3 (searches the current directory and all subdirectories for files called project3)

Y) Efads

Z) Fewfds

AA)

3) Logging onto cadence

3.1) To log into cadence log onto polarbear and then a campus machine by using the ssh –Y command.

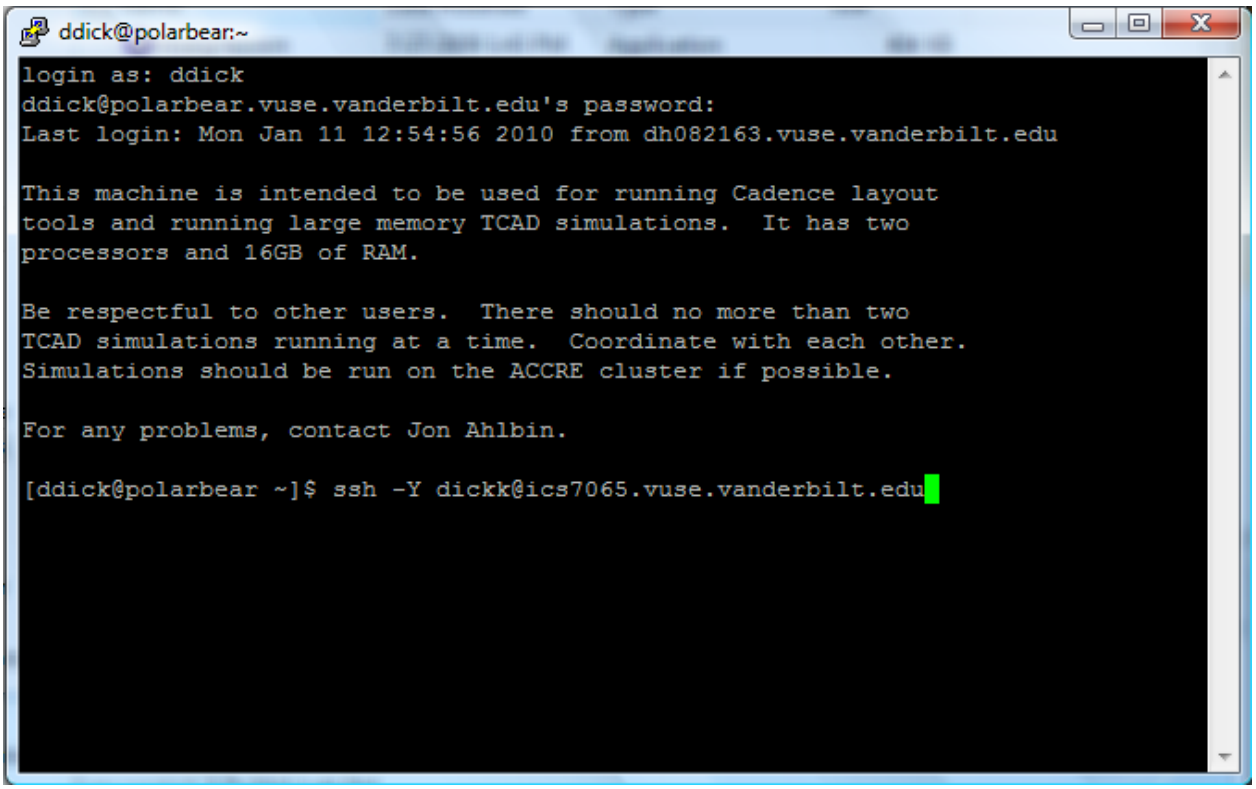

Figure 1: logging onto a campus computer

Here is a list of the campus machines:

ics7055.vuse.vanderbilt.edu
ics7056.vuse.vanderbilt.edu

ics7057.vuse.vanderbilt.edu
ics7058.vuse.vanderbilt.edu
ics7059.vuse.vanderbilt.edu
ics7060.vuse.vanderbilt.edu
ics7061.vuse.vanderbilt.edu
ics7062.vuse.vanderbilt.edu
ics7063.vuse.vanderbilt.edu
ics7064.vuse.vanderbilt.edu
ics7065.vuse.vanderbilt.edu
ics7066.vuse.vanderbilt.edu
ics7067.vuse.vanderbilt.edu
ics7069.vuse.vanderbilt.edu
ics7070.vuse.vanderbilt.edu
ics7071.vuse.vanderbilt.edu
ics7072.vuse.vanderbilt.edu

Next, you need to go into the NCSU_AMI06/ directory.

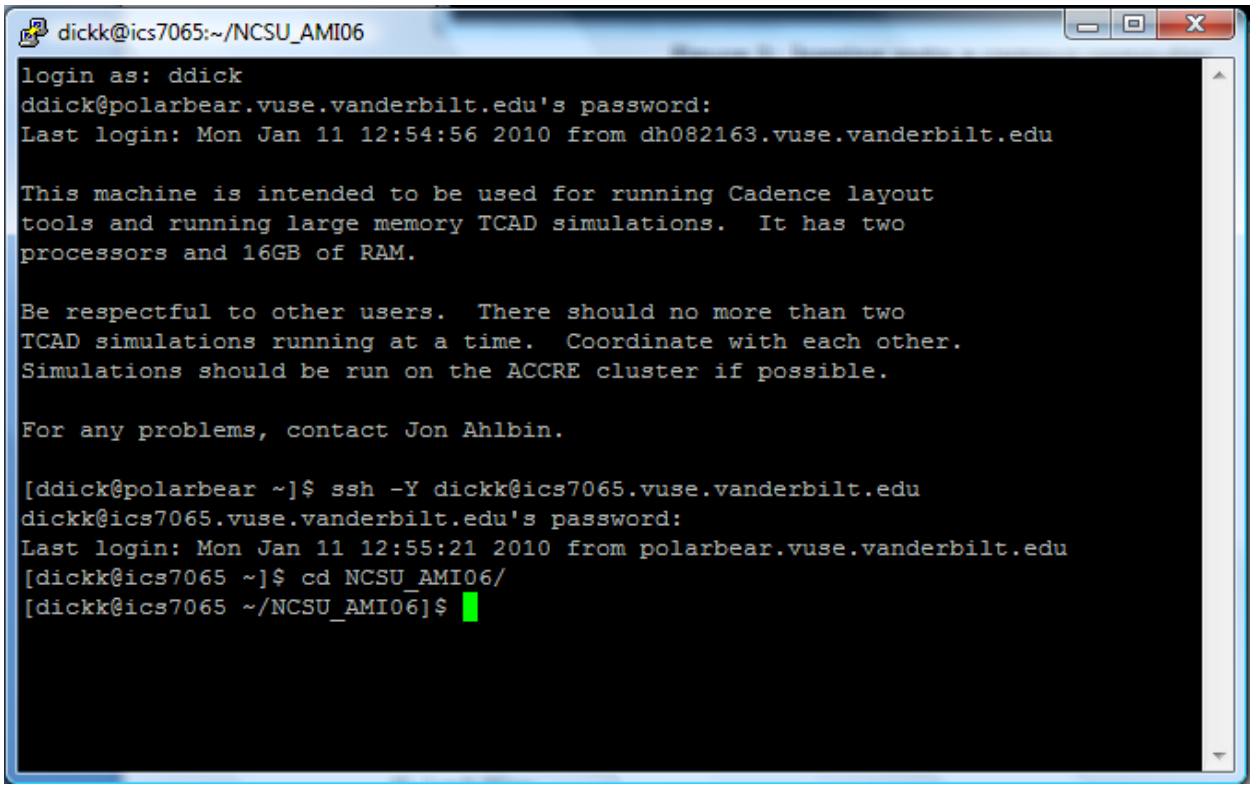

Figure 2: The NCSU_AMI06/ directory

Then, use the command **exec /bin/bash**. In bash, use the command **source soureme.sh** and then **icfb&**. This will log you into cadence.

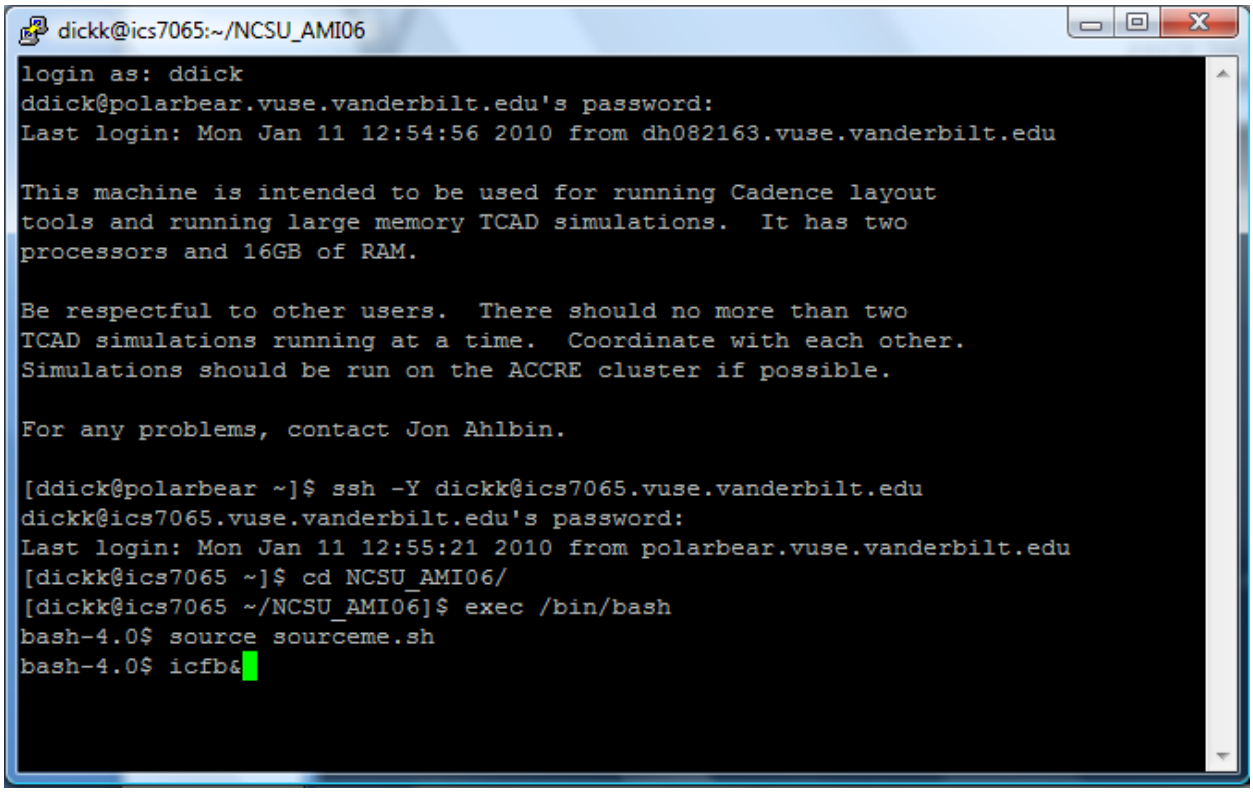

Figure 3: Logging into cadence

4) Lock files

4.1) If your file says "edit mode only" or otherwise does not respond, there is a good chance you have a .cdslck lock on your schematic or layout file. So, before you start and before you source the sourceme.sh file, type:
find $HOME -name *.cdslck
The find command should show you where the cdsclk files are in your directory. Delete (rm) these files, then you shouldn't have any trouble till the next time it locks the files.

Navigating in Cadence

1) The icfg log is the window that gives you gives you a list of the actions that have taken place in cadence, Figure 1. This most recent action is at the bottom of the list. This is where you go to see the result of DRC and LVS checks. The file tab allows you to create a new library or cell, import files, export files and open files in the library manger. The tools tab gives you a list of the different tools that are available in cadence. The options tab allows you to save the session and change the preferences.

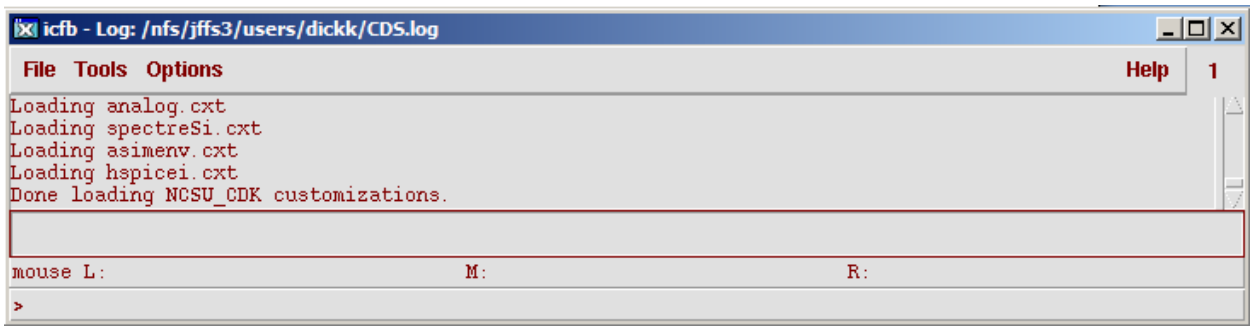

Figure 1: Icfb log

2) The library manager is where the libraries, cells and views are stored, Figure 2. If you select a cell of one of the libraries you can view the different layouts (schematic, extracted, layout, symbol, etc.) of that cell, by double clicking on the type of view. The file tab allows you to create a new library, cell view and category, open a cell view, load or save defaults or exit. The edit tab allows you to copy, rename, delete, change properties, access permission and library path.

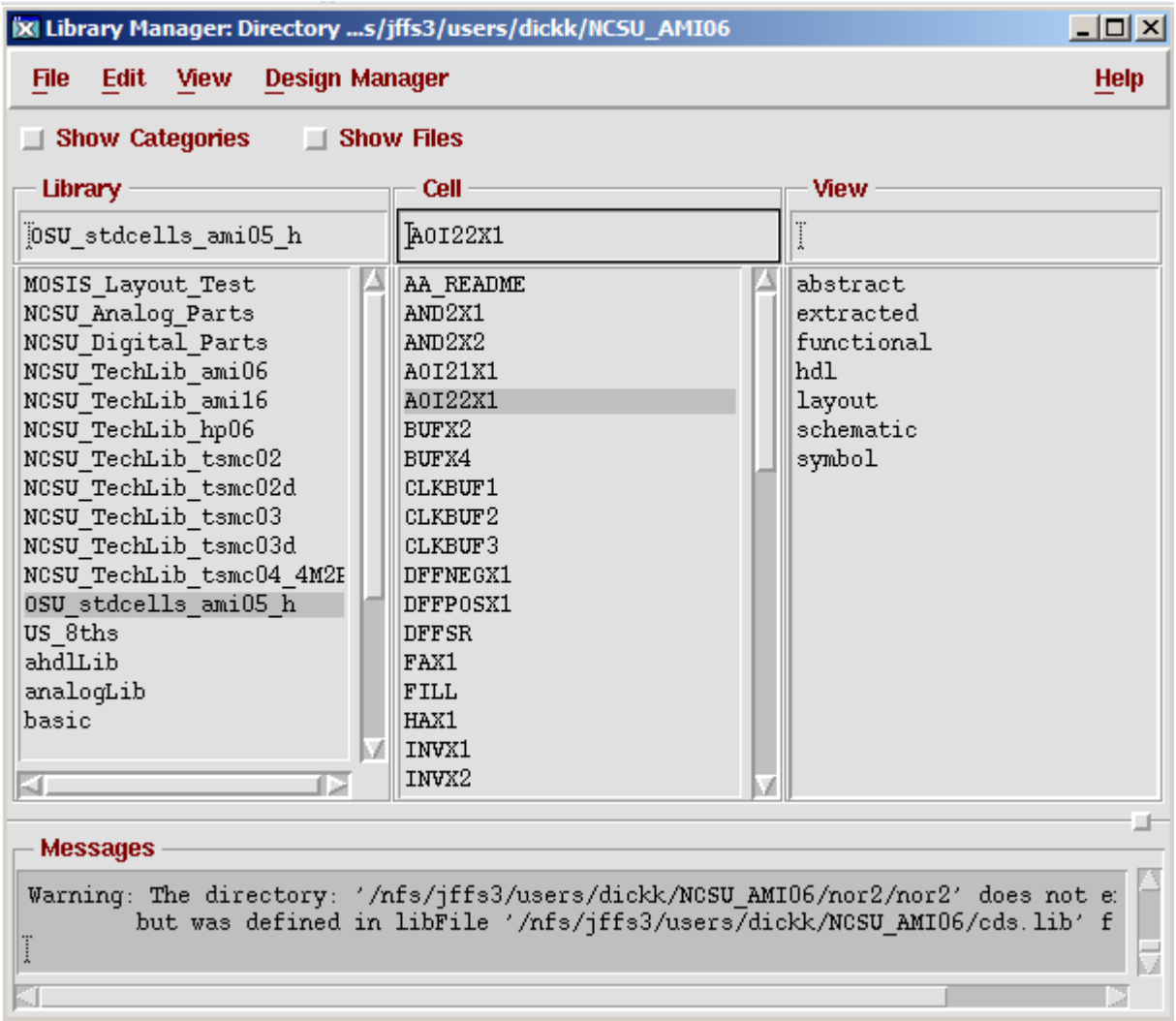

Figure 2: Library Manager

3) The virtuoso schematic editing window is where the schematic is built. The buttons on the left side are common used commands. To select an object, make sure that you do not have other commands running by hitting the Esc button on the keyboard, and run the cursor over the object and click on it, Figure 1.

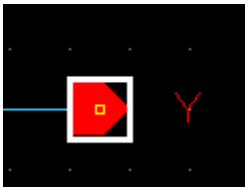

Figure 1: Selecting an object

There is a list of short hand keyboard commands that allows you to quickly call the command. For example "m" is short for move, which will allow you to move an object. These short keyboard commands can be found by going to the tabs at the top of the window and looking at the right of the command, Figure 2.

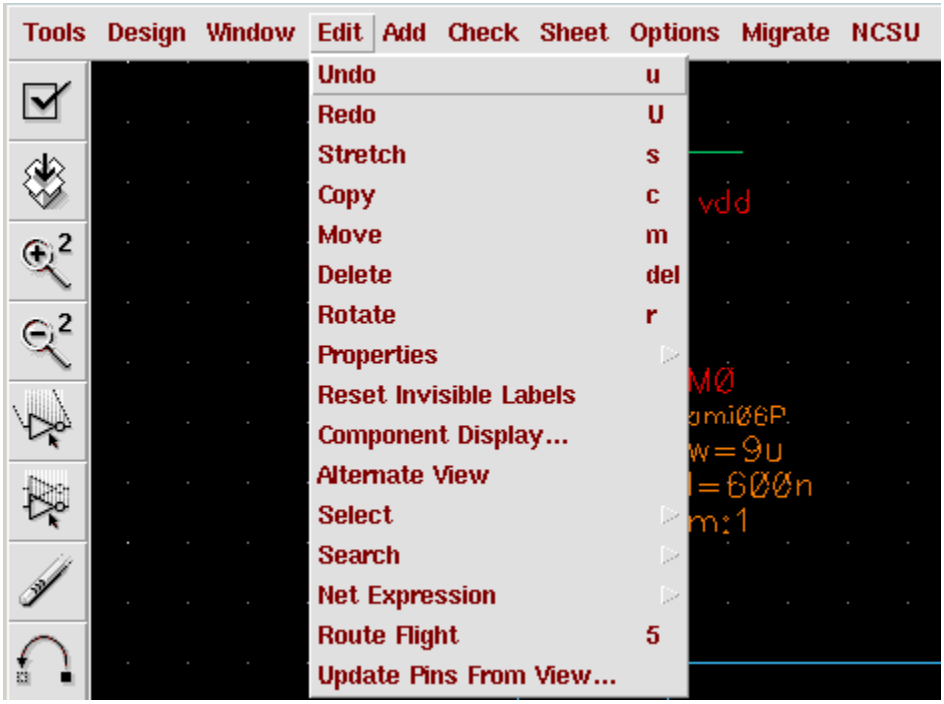

Figure 2: Finding the short cut keyboard commands

To move an object around go to the edit tab and select move, or use the short command of "m", and select the object you wish to move. To delete an object you can click on the  button to the left of the window and click on the object, select the object and hit the delete button and the keyboard, or go to the edit tab and select the delete command and click on the object you wish to delete. If you drag the pointer across the buttons on the left side of the screen they will give a description for what they do 

. The virtuoso symbol editing window is very similar to the virtuoso schematics editing window. The symbol editing window is laid out the same way but has less functions. The virtuoso layout editing window has is similar to the virtuoso schematic editing window but it also has a LSW window that appears with it. This window is to select the different layers to the parts of the transistor and connections between them. To select a layer, click on it in the LSW window and then go to the virtuoso layout editing window and draw the rectangle for that layer.

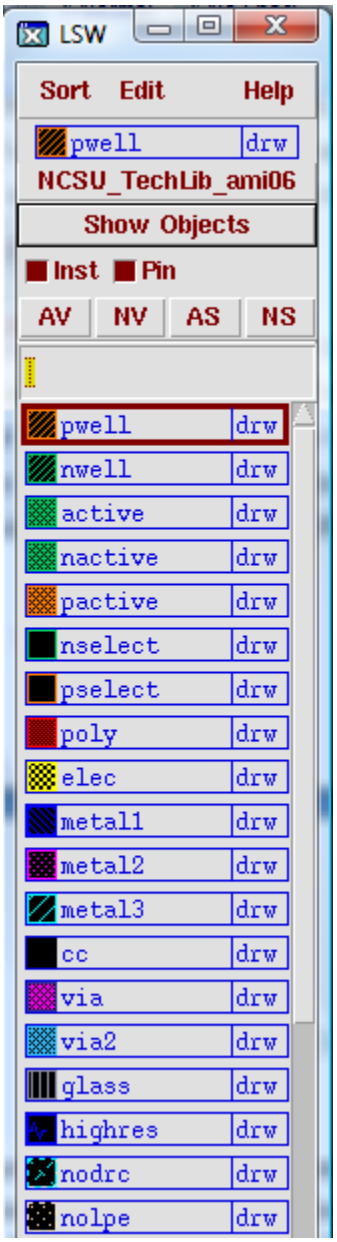

Figure 5: LSW window

If you want to view only one layer, select a layer from the LSW window and click on NV, which will select only that layer.

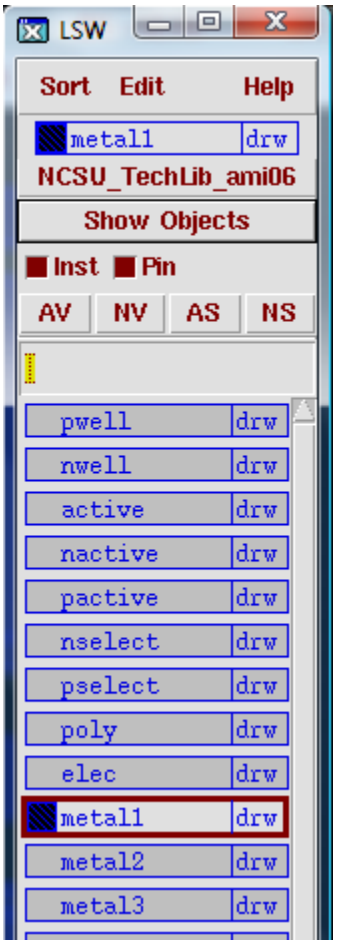

Figure 6: Selecting only one layer

Then go to the virtuoso layout editing window and click  . This will let you view only that layer that was selected in the LSW window.

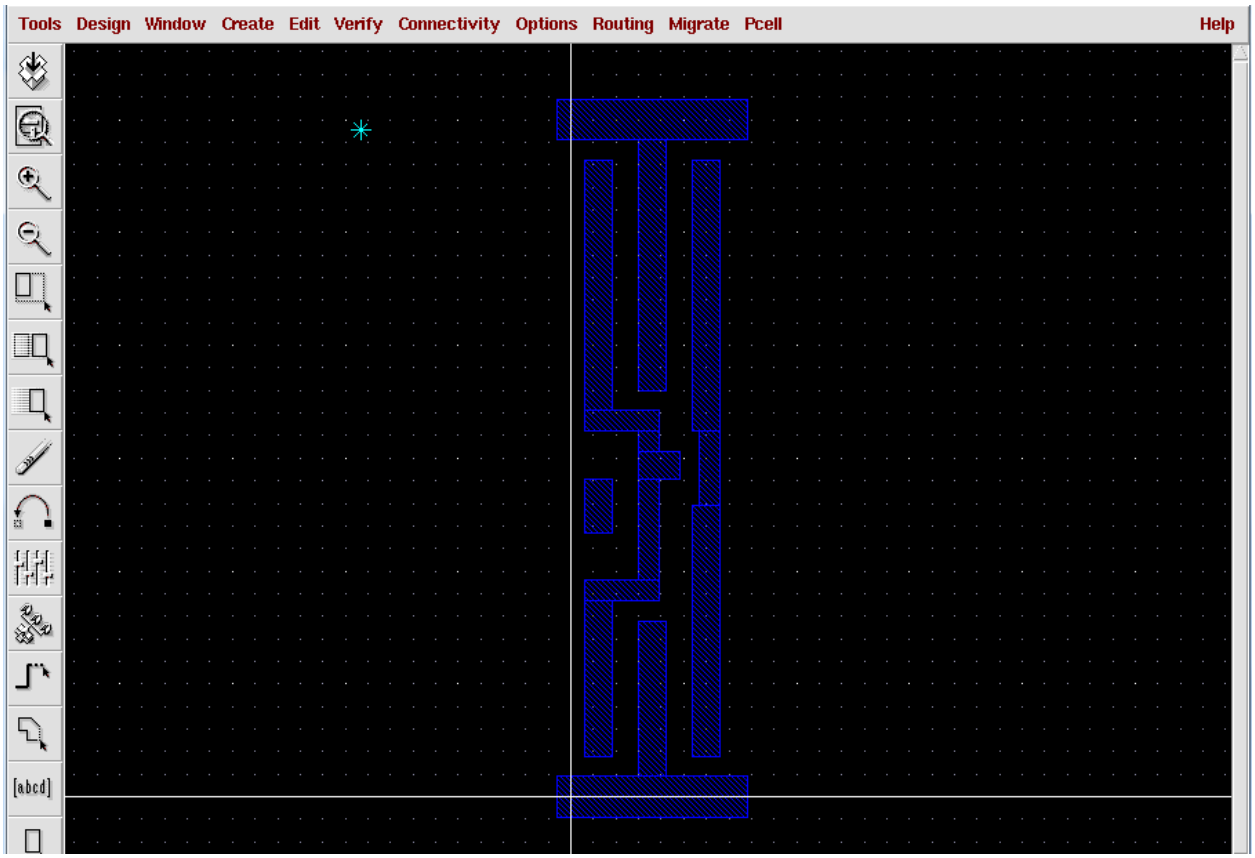

Figure 7: Viewing a single layer

Building a schematic

1) Creating a new library is the first part in building a new schematic. You can do this in one of two ways, first you can create a new library from the Library Manager, or the CIW. In either case select **File->New->Library**. This will bring up the create library window, Figure 1. Enter the name of the new library, for example **digital_lib**, and select **Attach Existing Library**. When there is no path entered, it will place the library in the directory from which you started Cadence. If you started Cadence correctly, this will be your **Working Directory**.

Figure 1: Create New Library Window

Next, select **Attach to existing tech library** and select one of the available libraries. Remember which one was selected because it will be required for simulation later, Figure 2.

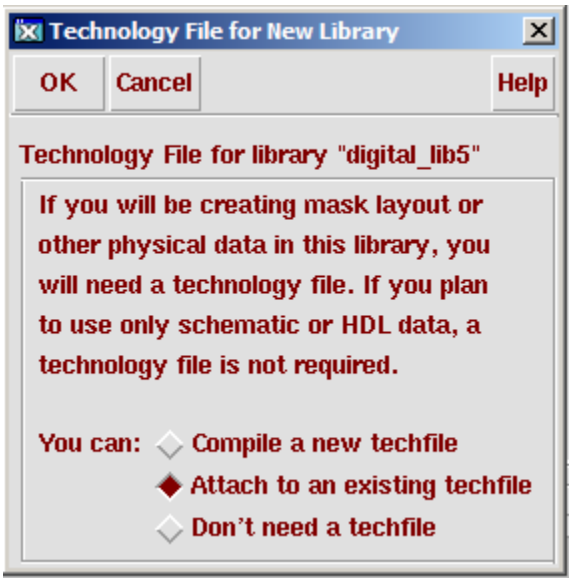

Figure 2: Attaching a techfile

2) The next step to creating a schematic is creating a new **Cell View**. This is done in the Library Manger, but it can be done it two ways. First, select the Library in which you will be adding this Cell. Second, either select **File->New->Cell View** from the Library Manger or you can type the name of the new cell in the blank under **Cell** in the Library Manger and hit the enter key. This will bring up a window in which you can specify the type of view you are creating, Figure 3. Since we are creating an inverter, we will name the Cell **inv**. It is good to give the cell a name that will help you remember what is in it.

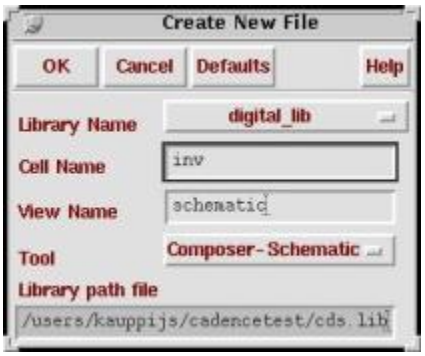

Figure 3: Create New Cell Window

In the **Create New File window**, select as the tool **Composer-Schematic**. This will cause the View Name to be automatically filled with the name **schematic**. When you are finish click the **OK** tab. This will close the current window and bring up the window in which we will design the schematic of the Inverter.

3) Now we are ready to layout the schematic design of the Inverter. After creating the new cell, a window opens in which we will create our schematic, Figure 4. This window is the Virtuoso Schematic Editing window.

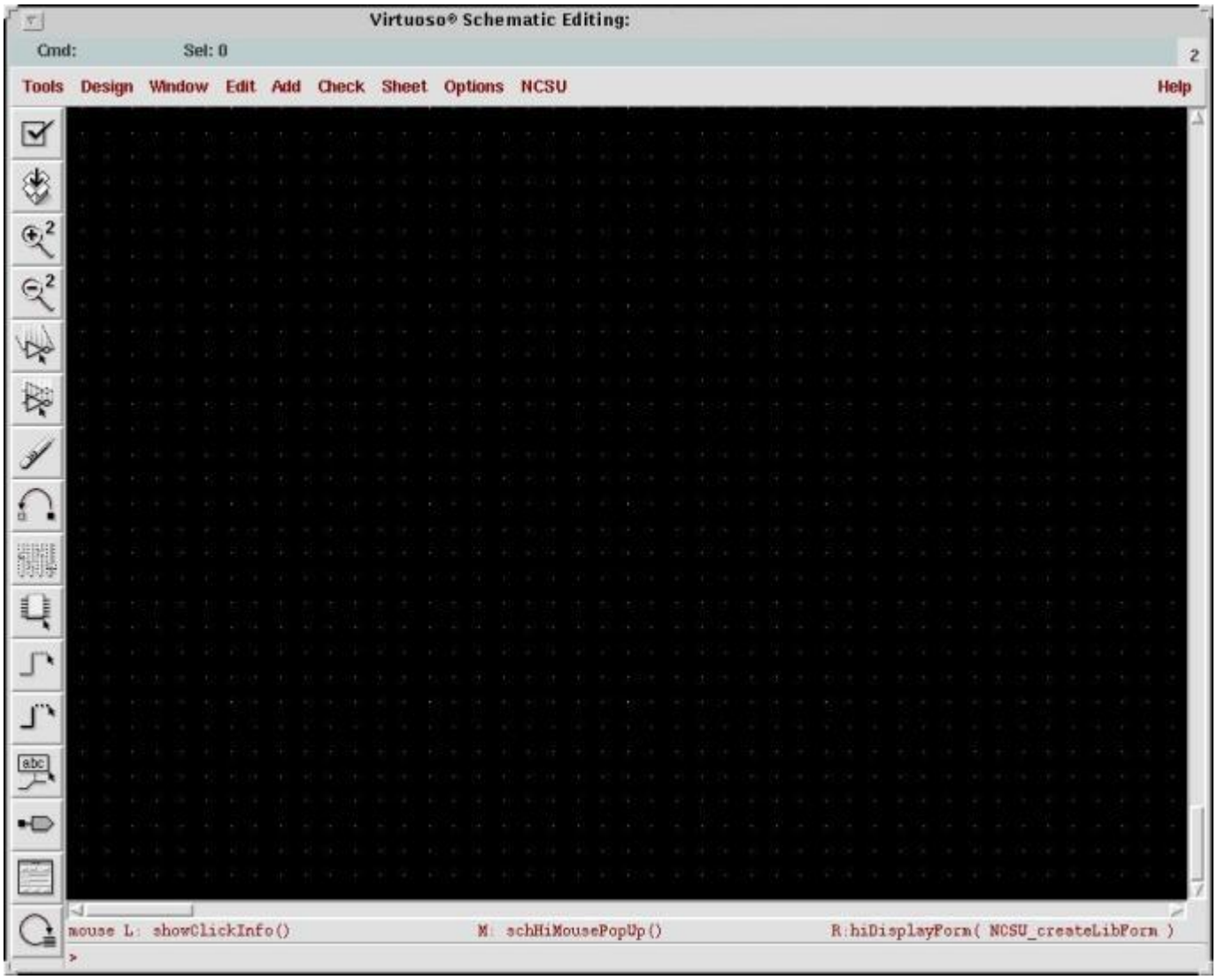

Figure 4: Virtuoso Schematic Editing Window

The schematic level design is building the inverter from the transistor level. To add a component click **Add->Instance**. This brings up the Component Browser and a window in which you can specify the component to be added, Figure 5.

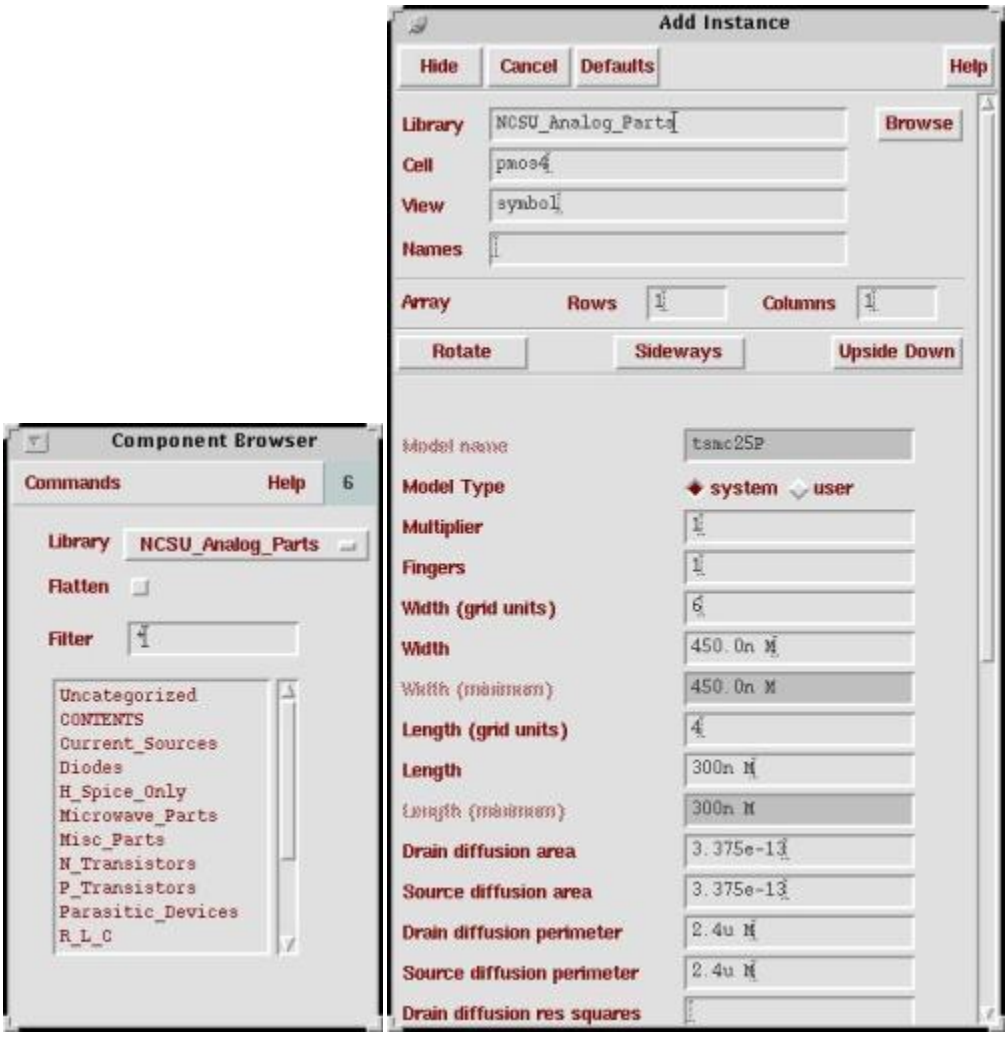

Figure 5: Component Browser and Add Instance Windows

The first to add is the nmost transistor. To select this transistor, select **NCSU_Analog_Parts** then select the category **N_Transistors** and select the **nmos4** transistor from the list. In the Add Instance window enter the width as 4u and the length as 2u. Cadence will automatically change this to 4u M and 2u M respectively. Move the cursor into the editing window. Notice that there is an nmos transistor there instead of the normal cursor. To place the component, you need to left click. To rotate the component you need to right click. To exit from adding the current component or any other action press the Esc key. Notice that there are letters next to many of the choices in the menus, these are hot keys and can make you work progress a lot faster if they are learned. Place the nmos transistor in the bottom half of the screen on the right side of the center line.

Next, we will add a pmos transistor. This is located under the library **NCSU_Analog_Parts->P_Transistors** and select the **pmos4**. Give it the same width and length and place it on the top half of the screen above the nmos transistor.

The next step is to add the pins. Click **Add->Pin** and a window appears for adding pins to the schematic. We will add pins *vdd, vss, in,* and *out*. Ensure that the direction is set to inputOutput, Figure 6.

Figure 6: Add Pin Window

The order in which the pins are added does not matter. You can also add only one pin at a time. In the current method, the pins will be placed in the order they appear in the list. First, place the vdd pin above the pmos transistor. Note the small diamond that is the actual pin so rotate the object until the diamond faces down toward the pmos transistor. Add the vss below the nmos, the in to the left of the screen, and the out to the right of the screen. In all cases make sure the small diamond faces the transistors.

Now we will add wires to connect the entire Inverter so it will work. Click **Add->Wire** to add wire or you can use the hot key 'w'. Refer to Figure 7 below to see how the connections are made. Notice that as you get closer to a device or node when placing wire, a small diamond appears. This is where you need to click to place a wire. If you make a mistake click on the error and select **Edit->Delete**.

Once you have completed adding all components and wire, Figure 7, click the "check mark" icon on the left of the window. This will check your work for errors and save your work to the library. The same can be done with **Design->Check and Save**. Any errors will be reported in the CIW.

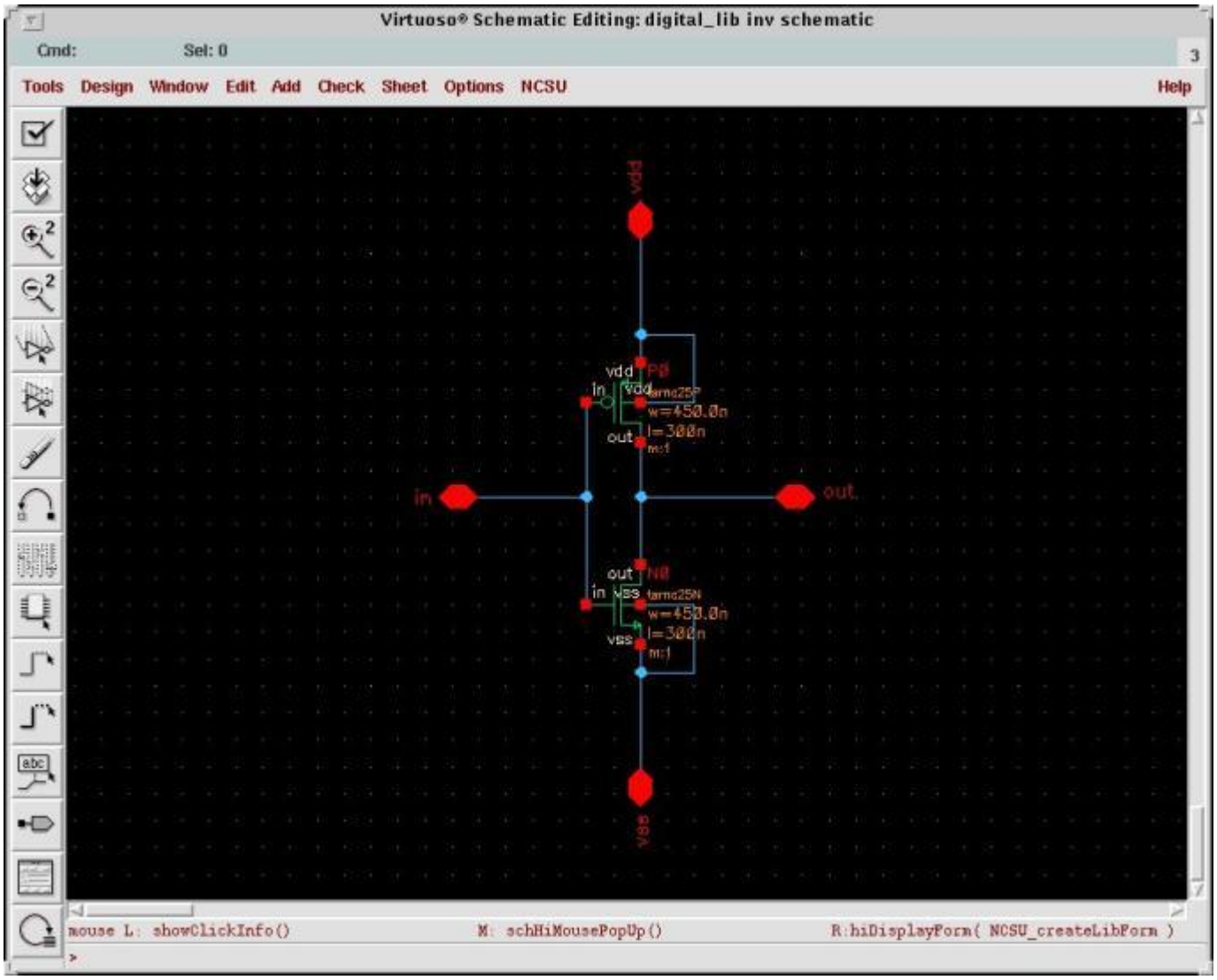

Figure 7: Finished Schematic of the Inverter

4) When the schematic is finished you can print it out. To do this click **Design->Plot->Submit**. The window that appears allows you to select the options for printing, Figure 8. You can print directly from here, or if desired, the schematic can be saved as a file, such as a PostScript. To save to a file click **Plot Options** on the bottom of the window. In the new window, select **Send Plot Only to File** and enter the desired file name, such as plot.ps.

Figure 8: Submit Plot and Plot Options Windows

Building a symbol

1) This part of the tutorial deals with the layout of the symbolic representation of a circuit, in this case an inverter. As with the schematic, we will create a new cell view for the symbol. You can make the new cell view though any of the methods we have previously discussed. We will also name this view **inv**, but it will be a symbol rather than a schematic, Figure 9.

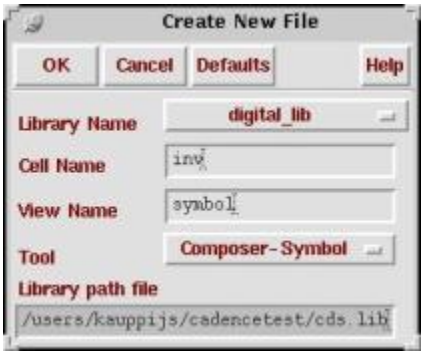

Figure 9: Create New Symbol Window

Make sure symbol is the View Name and Composer-Symbol is the Tool. Press OK to continue and a familiar window will appear in which you will draw the symbol, Figure 10.

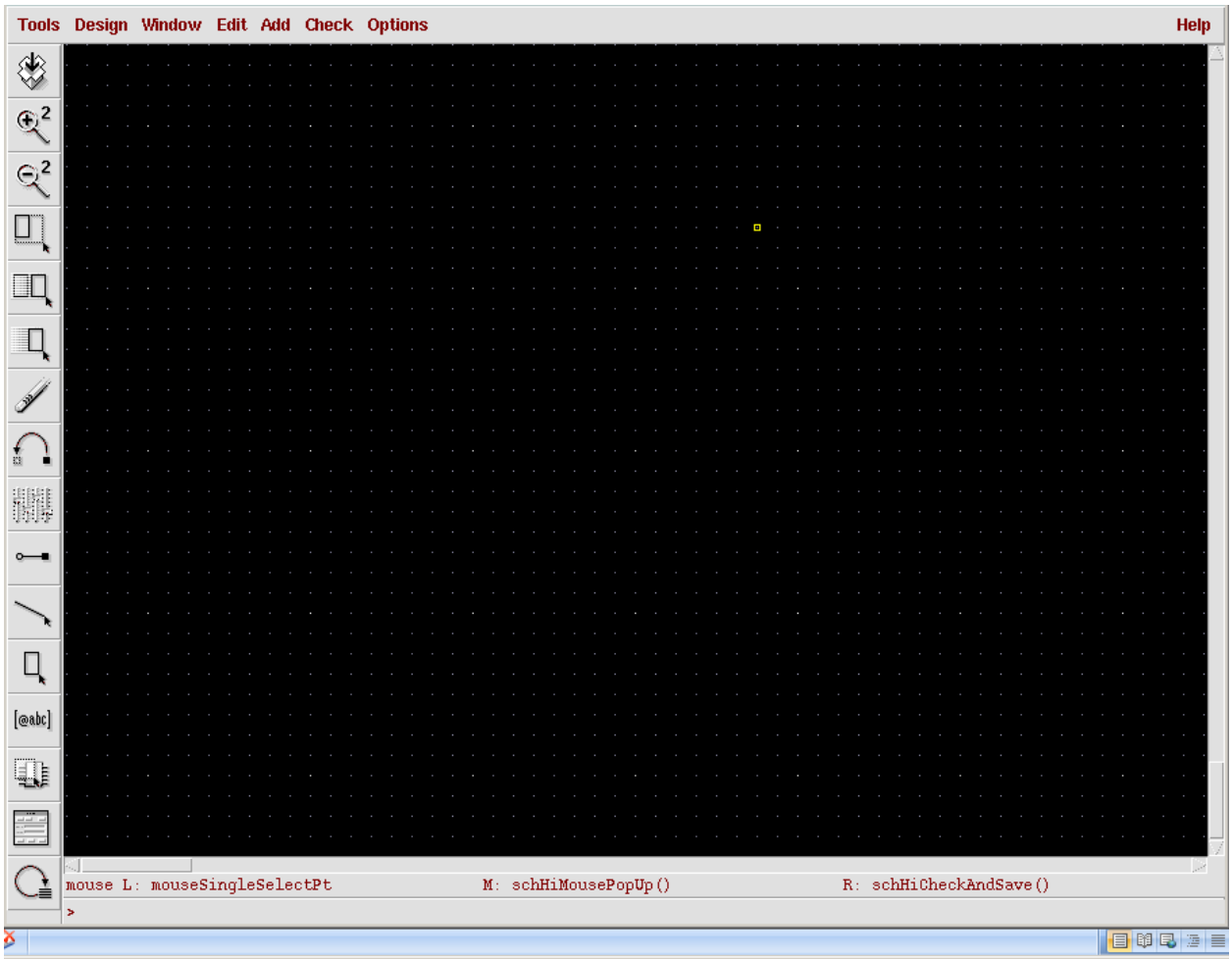

Figure 10: Virtuoso Symbol Editing Window

First, we need to draw a triangle on its side to represent the body of the inverter. Draw a vertical line on the left of the center line and connect the ends at a point on the right of center. To access the tools needed to draw the shapes click **Add->Shape->Polygon**. Figure 11 shows this window and other required settings.

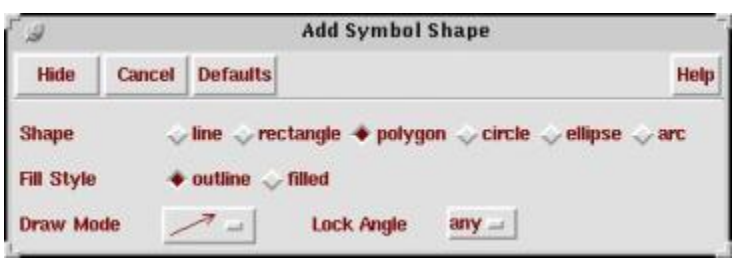

Figure 11: Add Shape Window

After adding the triangle, we need to add a circle at the right point to indicate negation. Click **Add->Shape->Circle** and then on the diagram click where you want the center of the circle, move the mouse until the circle is the size you want, and click again to stop sizing the circle.

Next we need to add the pins to our inverter. As before, click **Add->Pin** to bring up the Add Pin Window. We will again create pins **vdd, vss, in,** and **out**. As in the schematic make sure the pins are specified as **inputOutput**. The Add Pin Window can be seen in figure 12 below.

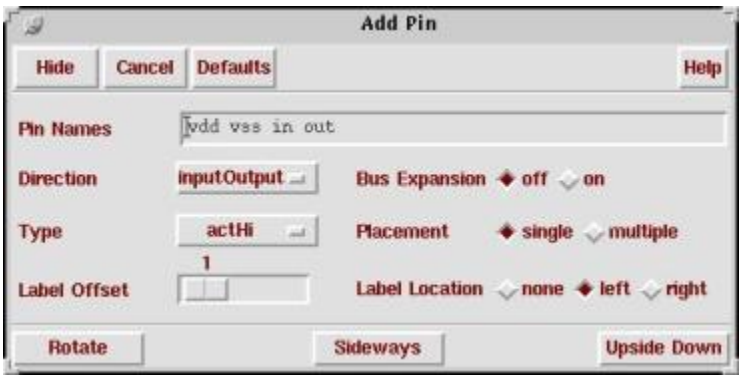

Figure 12: Add Pin Window

Now we need to place the pins. This is done in the same manner as in the schematic, but these pins are represented differently. On these pins, one end of the line has a small box. This box is the actual pin. Place this box away from the symbol. The shortcut of right click to rotate will save a great bit of time here. Because the pin names may be hard to read now, you can move them by clicking **Edit->Move** or using the shortcut **'m'**.

Now we want to label the symbol. We will add two labels here. Begin by clicking **Add->Label**, which will invoke the Add Label box, Figure 13.

Figure 13: Add Label Window

The first label is going to be the *instance label*. This is the default label as seen above. Place this label near the symbol of the inverter. The second label will be the name label. If the Add Label box disappeared after adding the instance label, bring it back up. Change label type to **normalLabel** and type the name of the device in the Label field, Figure 14. Place this label on or near the symbol. When we place the symbol in schematics, all of the symbols will have the same name, but different instances, e.g. U1, U2, etc.

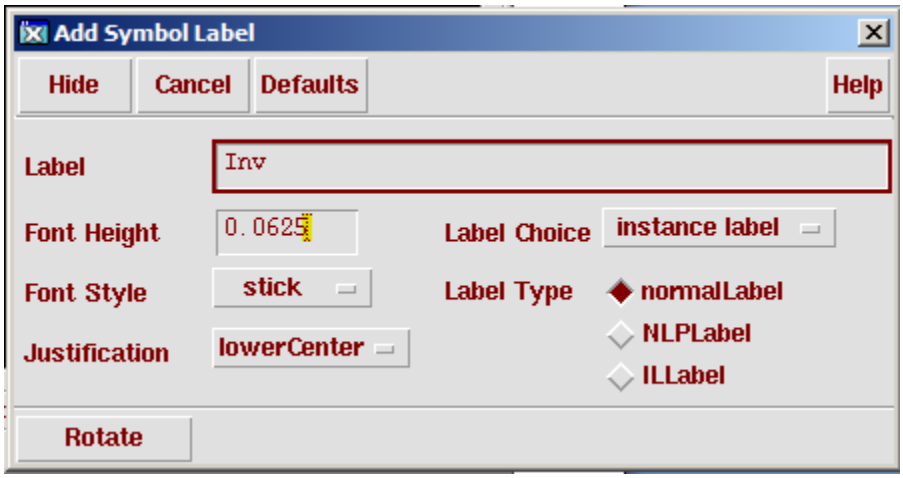

Figure 14: Add Symbol Label Window

The last task is to add the selection box to the symbol. Click **Add->Selection Box** and click on the choice of **Automatic** on the window that appears.

The symbol is now finished and should look similar to the symbol below in **Figure 15**. If you are satisfied with the symbol, save it by clicking **Design->Save**.

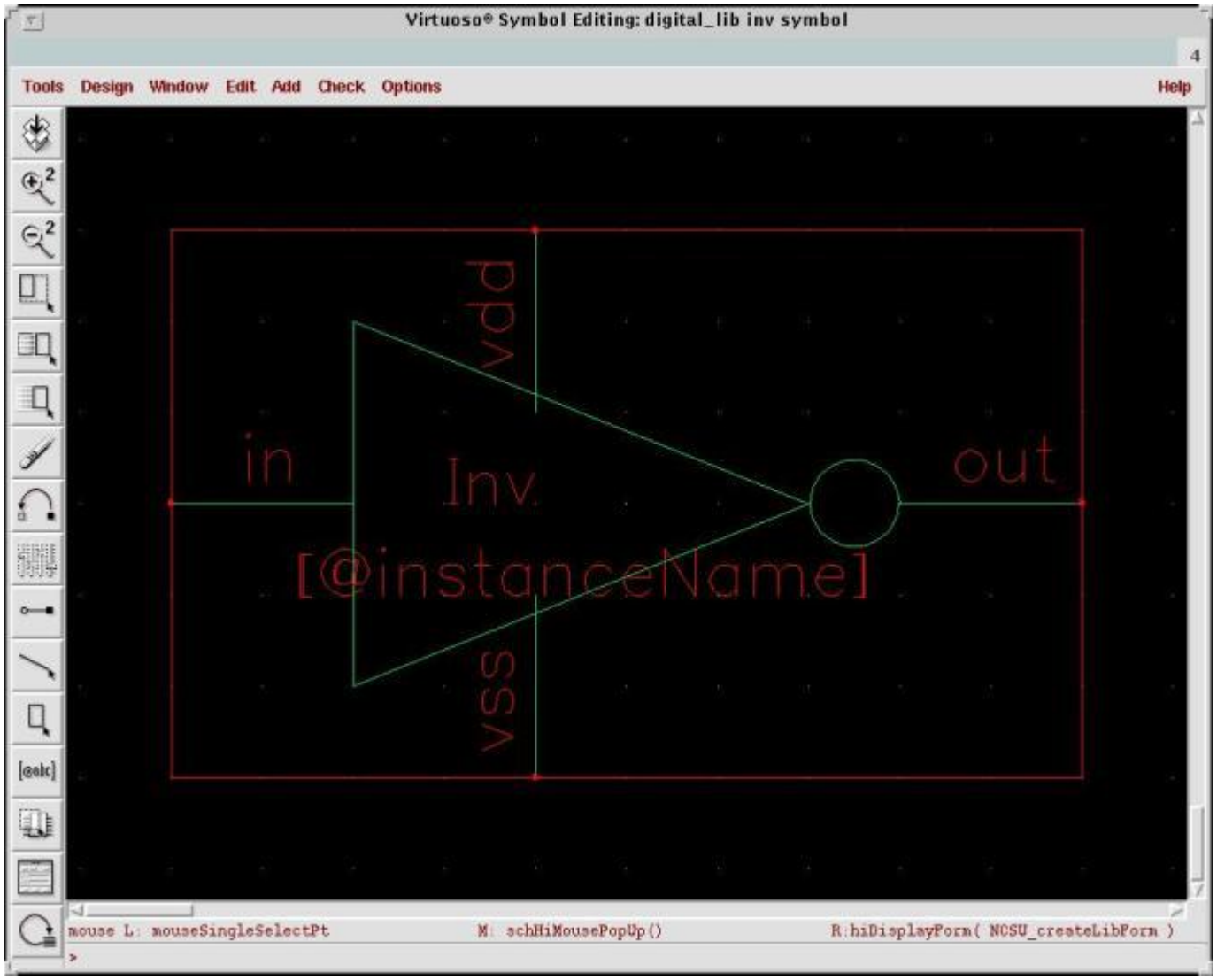

Figure 15: The Finished Inverter Symbol

Simulating the Circuit

1) This final part of the tutorial deals with simulating a circuit that has been designed, in this case the inverter. To test out the inverter, we will make a new schematic of a network with the inverter in it. To create a new schematic, we need a new cell view. We can create a new library entirely, but for simplicity, we will create a cell view within our current library. This is done in the same manner in which it was done in all of the previous steps. We will call the new cell view **inv_test**. Make sure that the selected tool is **Composer-Schematic**.

In the new schematic, we need to add the inverter, two DC voltage supplies, a ground connection, and a capacitor. First we will add the inverter. Click **Add->Instance**, change the library to your library, and select inv. Place it in the center of the schematic. Next we will add the two voltage supplies. The first we will add is the input supply. Click **Add->Instance**, change to NCSU_Analog_Parts, click Voltage Supplies, and select vdc, Figure 14. Place the first supply to the left of the **in** pin on the inverter. You may want to rotate the supply so that it is horizontal with the positive terminal closest to the **in** pin. Before placing the next supply (the vdd supply) we need to change a parameter for the supply. In the Add Instance window, set the DC Voltage to 5 V. Place the supply at the top of the schematic.

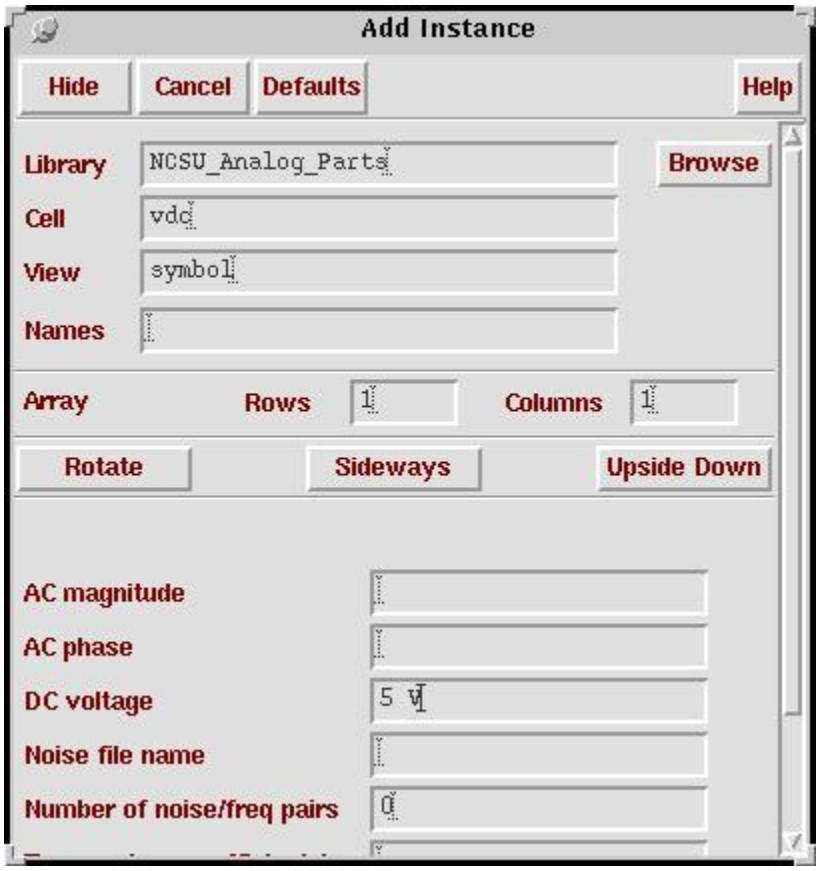

Figure 14: Add instance of 5V DC voltage supply

Next we need to add the ground connection below the **vss** pin of the inverter. This is found under Supply_Nets in NCSU_Analog_Parts. We also need to add a capacitor at the output of the inverter to act as a load. This is found under Parasitic_Devices in NCSU_Analog_Lib. When all of the components are placed, we need to add a pin at the output of the circuit. Add a pin called out. This pin should be an INPUToutput pin as have all of the previous pins. The finished circuit should look similar to the one below:

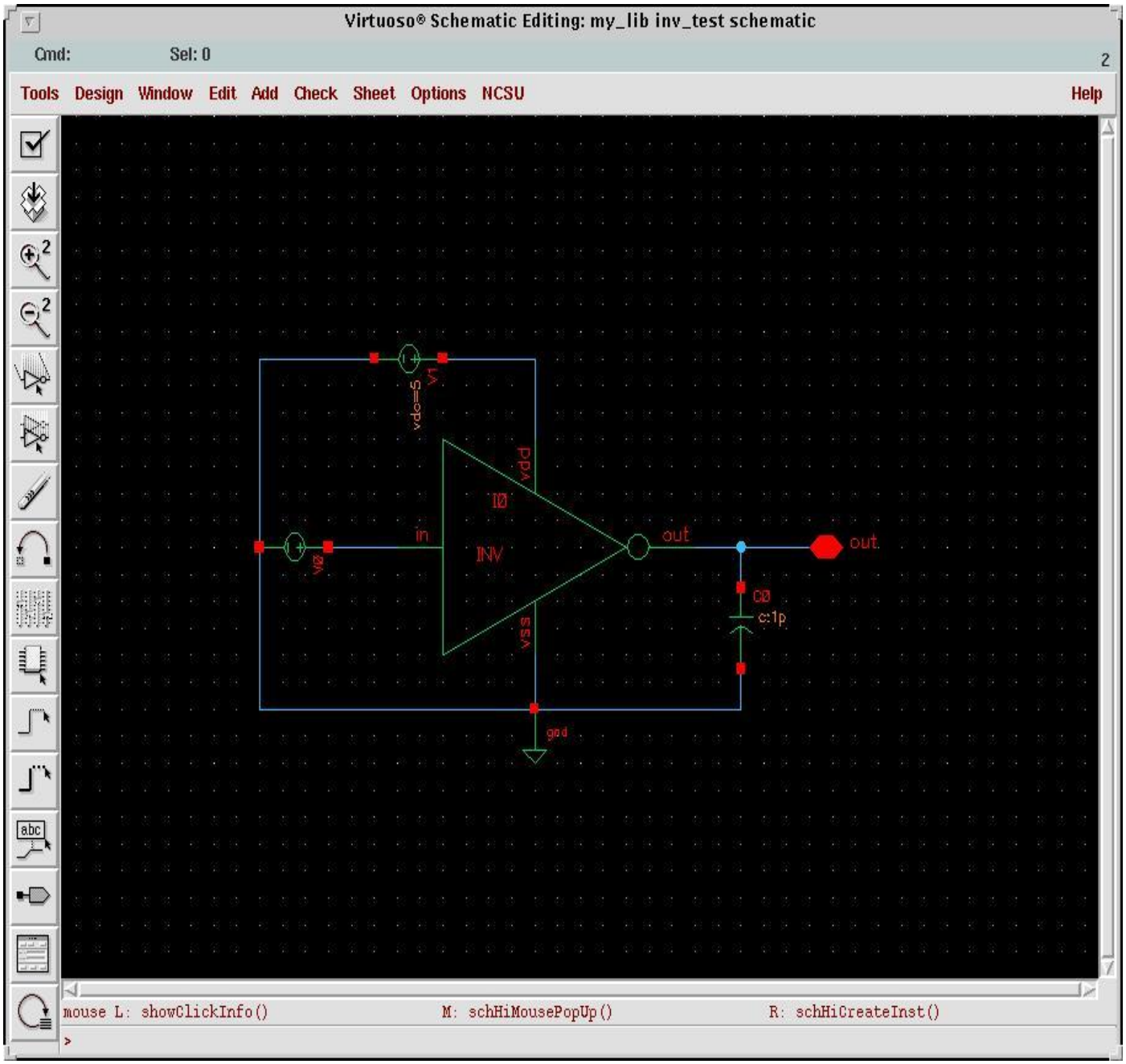

Figure 15: The test schematic

2) We are now ready to simulate this schematic. Click **Tools->Analog Environment** to open the window that gives access to the simulation tools, Figure 16.

Figure 16: The Analog Environment Window

Make sure the simulator is set to **spectreS**. Go to the tab, Setup, and select Simulator/Directory/Host… In this window make sure that simulator is set to specterS.

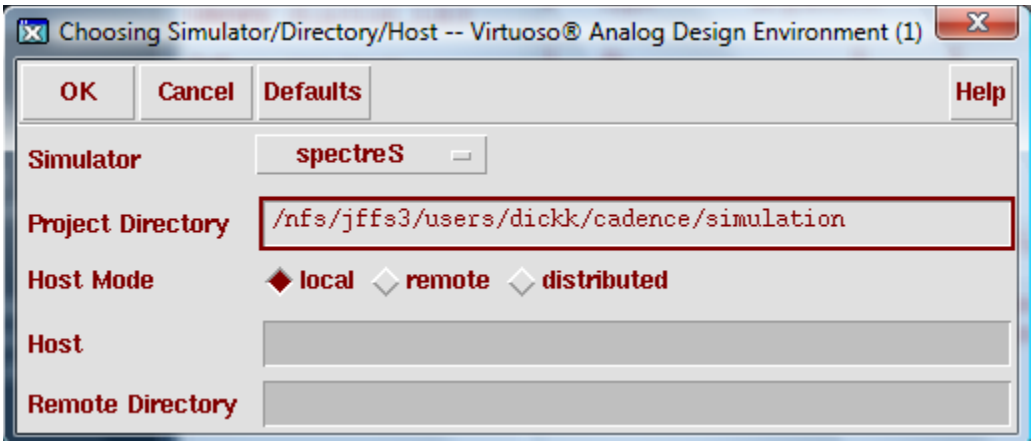

Figure 17: Setting up the simulator

Now we need to specify what we want to do with our simulation. We first need to specify our analysis, click **Analyses->Choose**. In the window that appears, select **dc** and click **Component Parameter**. Next double click **Select Component**, so that you can select the input DC voltage source on the schematic, Figure 18. This will bring up another window in which you need to select the parameter of the source that will be used in the analysis. Select **dc**.

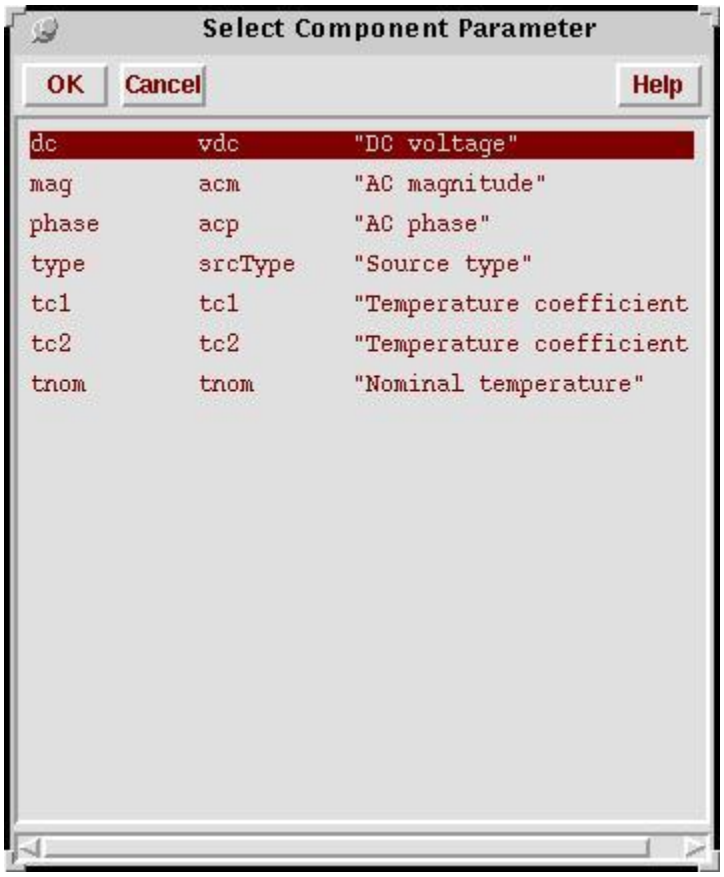

Figure 18: Select Component Parameter

Next enter the starting and stopping voltages for the supply (Start: 0V, Stop: 5V). Select linear for **Sweep Type** and make the **Step Size** 0.1. The Analysis window should appear similar to the one below:

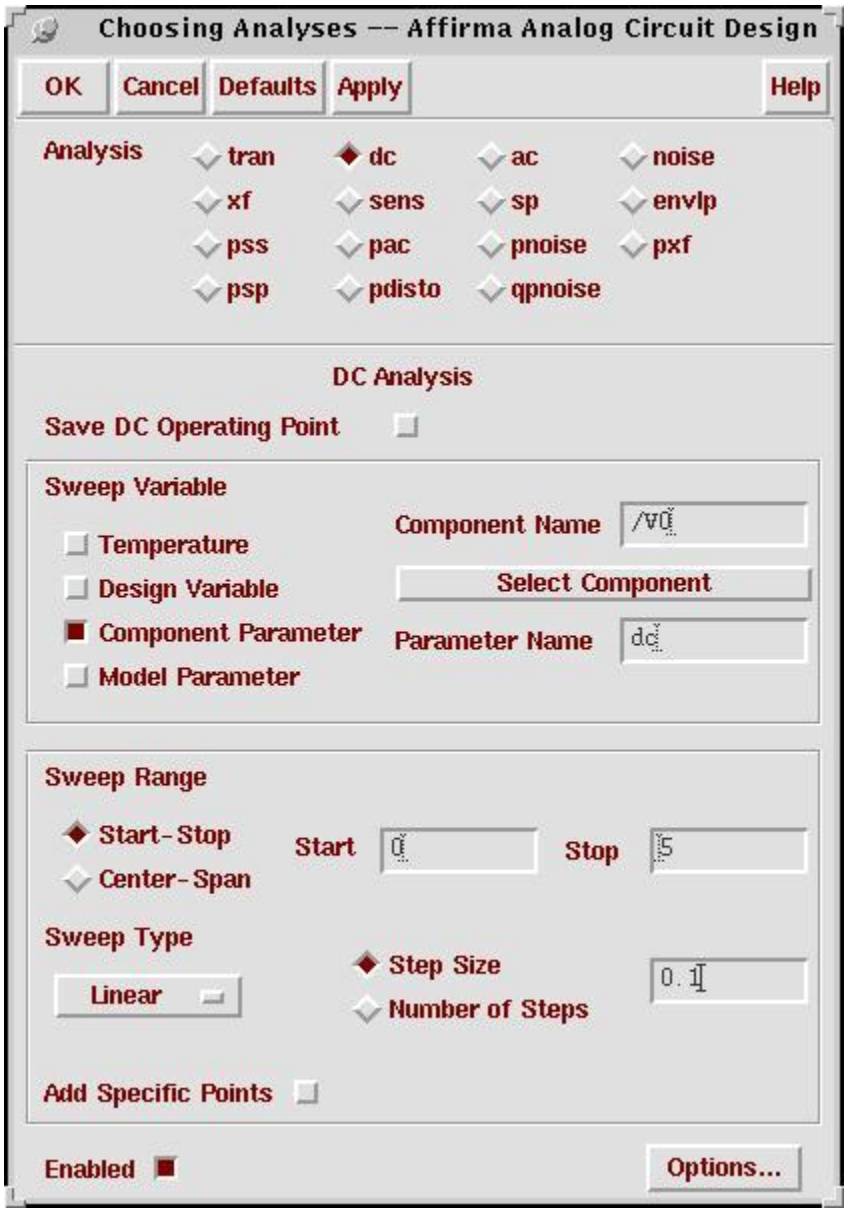

Figure 19: Analysis Setup Window

Click Ok to close the window. The next step is to select the outputs. Click **Outputs->To Be Plotted->Select On Schematic**. This will bring the schematic window to the front. Select the nodes at the input and output of the inverter, Figure 20.

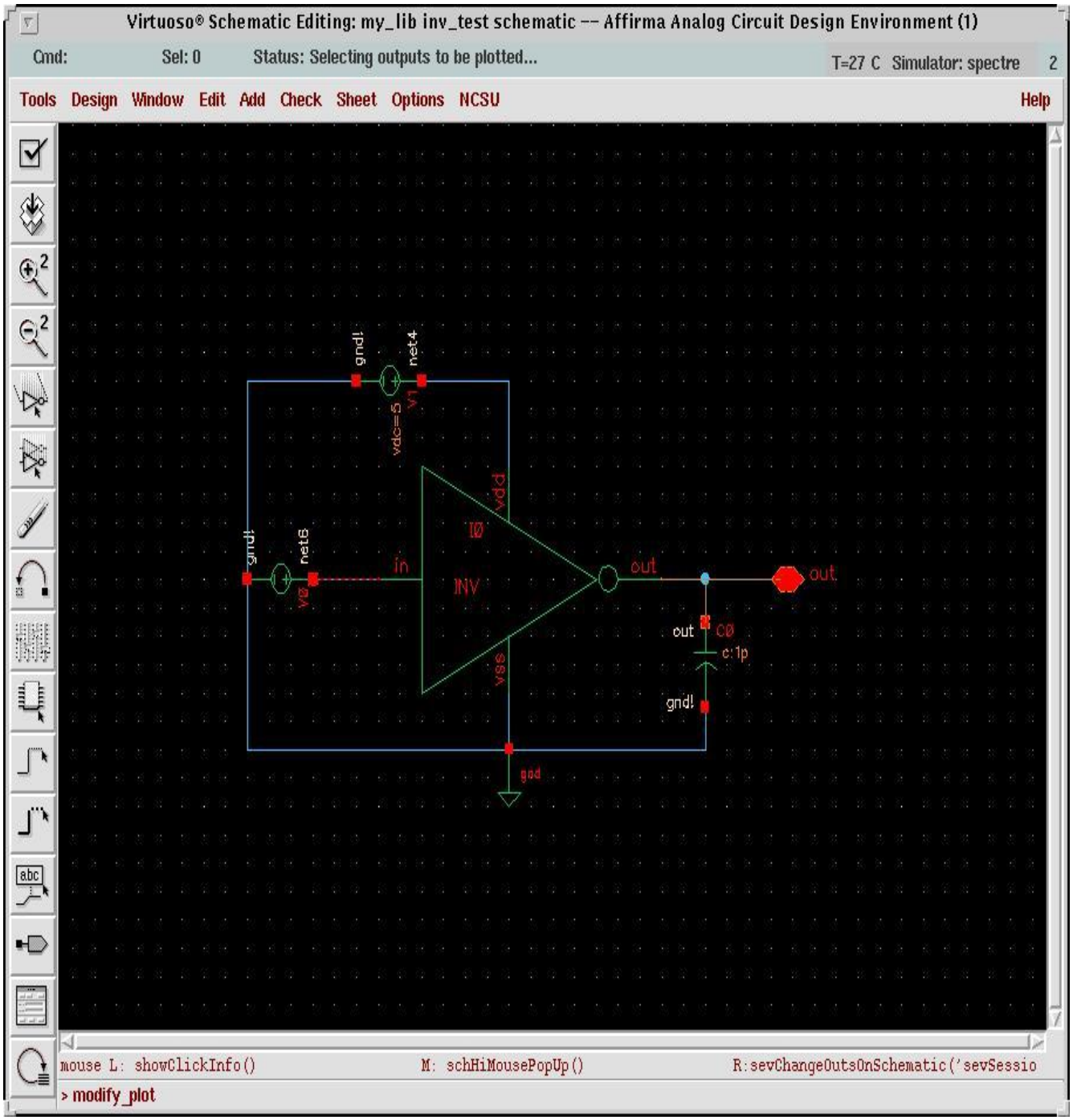

Figure 20: Test Schematic with input and output nodes selected

This is done by clicking them once. Minimize the schematic and return to the Analog Environment window. This window should now look like the one below, Figure 21.

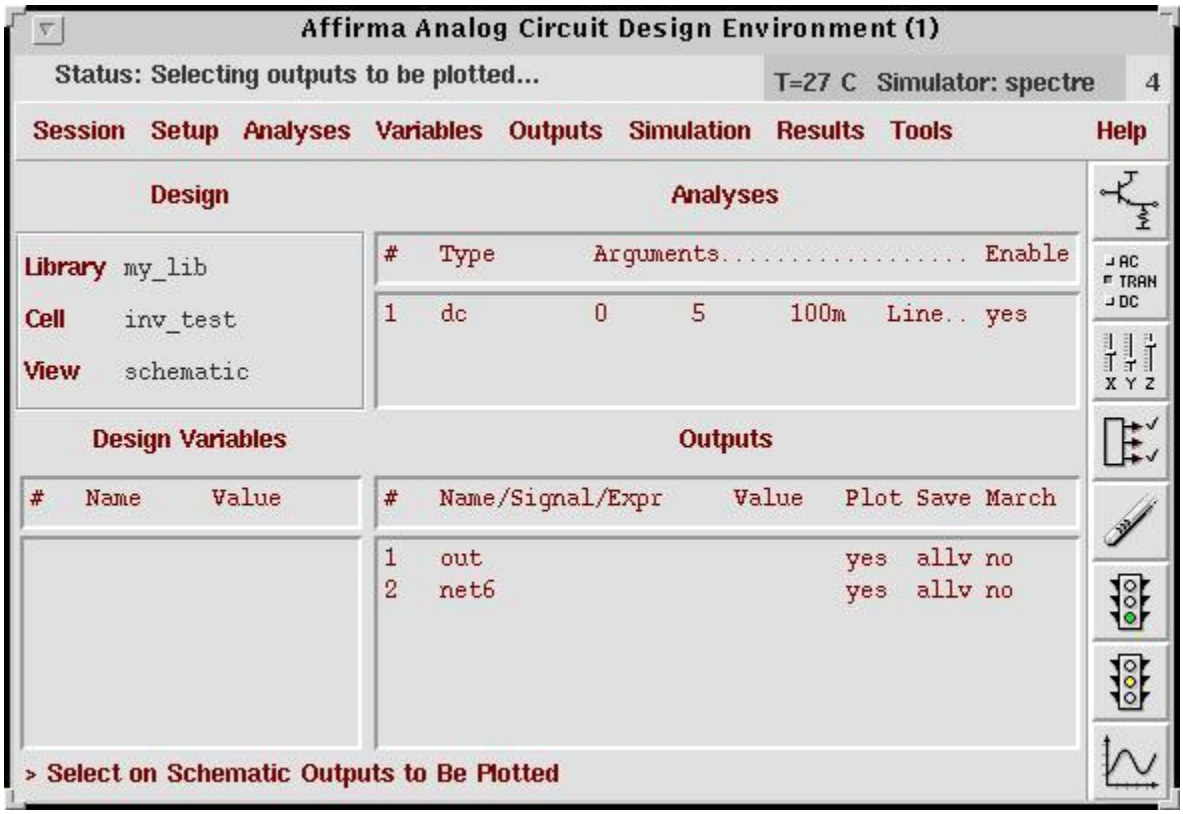

Figure 21: Analog Environment Window after simulation setup

Finally, we are ready to run our simulation. Click **Simulation->Netlist and Run**. This will run the simulation and should produce an output file and a plot of the inverter's input and output, Figure 22.

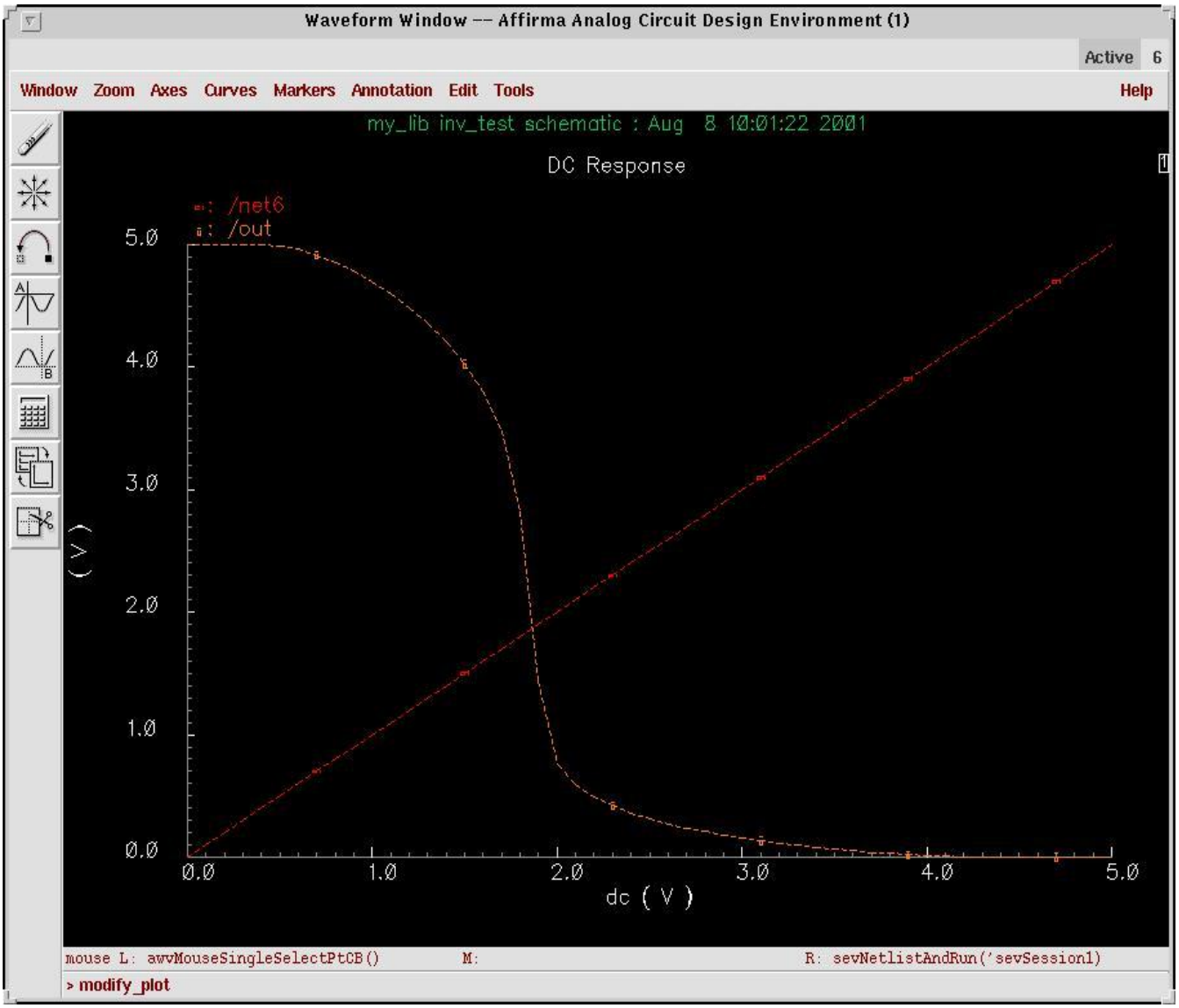

Figure 22: Input/Output plot for the inverter

```
/nfs/nietzsche/users/kauppijs/cadence/simulation/inv_test/spectre
File                                                    Help    5

          equations 5
            bsim3v3 2
          capacitor 1
            vsource 2

Entering remote command mode using MPSC service (spectre, ipi, v0.0,
        spectre0_23730, ).

************************************
DC Analysis `dc': V0:dc = (0 V -> 5 V)
************************************
Important parameter values:
    reltol = 1e-03
    abstol(I) = 1 pA
    abstol(V) = 1 uV
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    gmin = 1 pS
    dc: dc = 200 mV         (4 %), step = 100 mV          (2 %)
    dc: dc = 400 mV         (8 %), step = 100 mV          (2 %)
    dc: dc = 700 mV        (14 %), step = 100 mV          (2 %)
    dc: dc = 900 mV        (18 %), step = 100 mV          (2 %)
    dc: dc = 1.2 V         (24 %), step = 100 mV          (2 %)
    dc: dc = 1.4 V         (28 %), step = 100 mV          (2 %)
    dc: dc = 1.7 V         (34 %), step = 100 mV          (2 %)
    dc: dc = 1.9 V         (38 %), step = 100 mV          (2 %)
    dc: dc = 2.2 V         (44 %), step = 100 mV          (2 %)
    dc: dc = 2.4 V         (48 %), step = 100 mV          (2 %)
    dc: dc = 2.7 V         (54 %), step = 100 mV          (2 %)
    dc: dc = 2.9 V         (58 %), step = 100 mV          (2 %)
    dc: dc = 3.2 V         (64 %), step = 100 mV          (2 %)
    dc: dc = 3.4 V         (68 %), step = 100 mV          (2 %)
    dc: dc = 3.7 V         (74 %), step = 100 mV          (2 %)
    dc: dc = 3.9 V         (78 %), step = 100 mV          (2 %)
    dc: dc = 4.2 V         (84 %), step = 100 mV          (2 %)
    dc: dc = 4.4 V         (88 %), step = 100 mV          (2 %)
    dc: dc = 4.7 V         (94 %), step = 100 mV          (2 %)
    dc: dc = 4.9 V         (98 %), step = 100 mV          (2 %)
Total time required for dc analysis `dc' was 20 ms.

modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
```

Figure 23: Spectre output file

Designing the Layout

1) Opening Layout File
    1.1) Log onto cadence.

1.2) Select the inverter file from your library.
1.3) Open the schematic of the inverter.

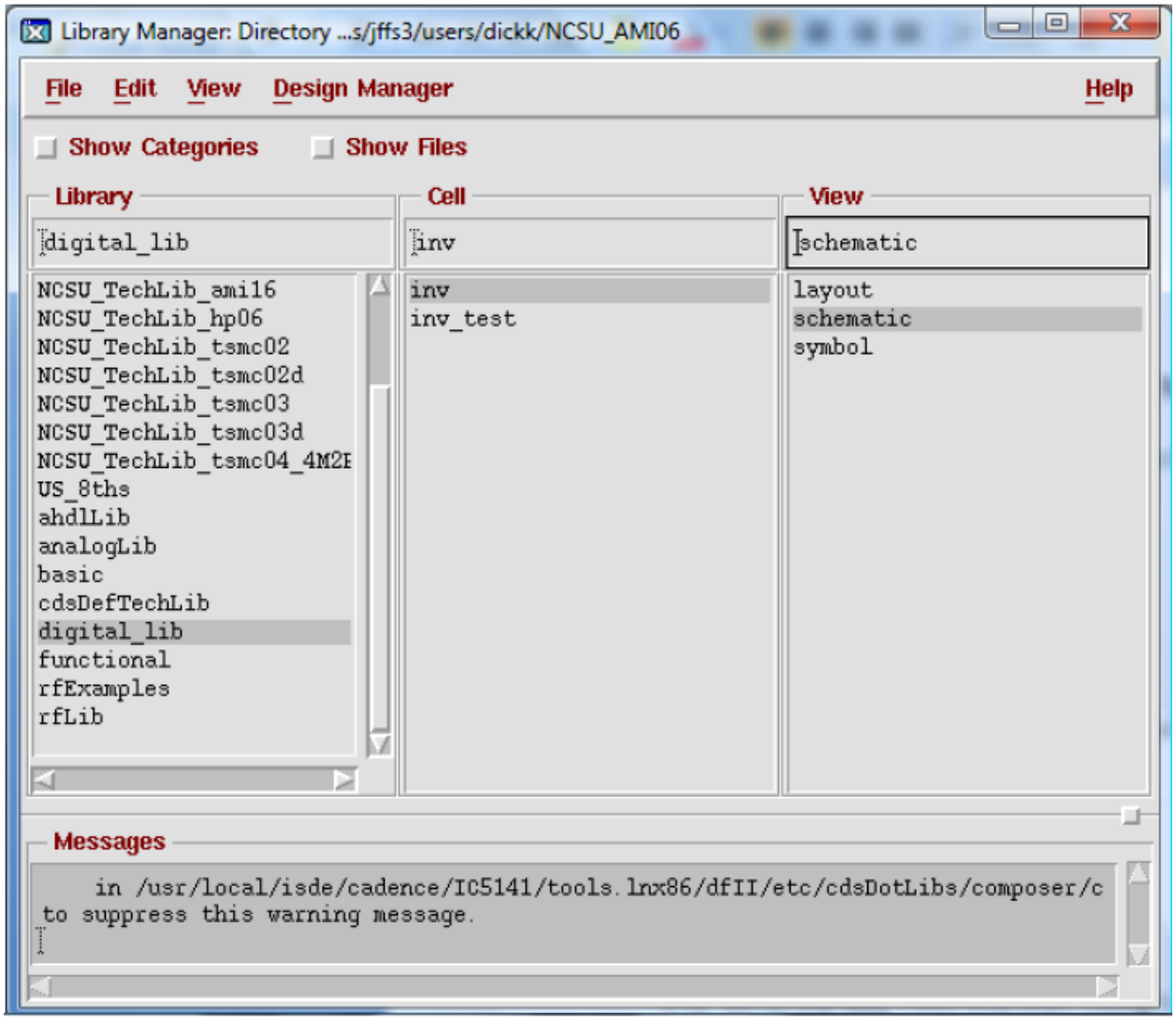

Figure 1: Opening schematic view

1.4) Go to the tab labeled Tool, and then Design Synthesis and select Layout XL.
1.5) This will open the Setup Options window. Select create new and click OK.

1.6) In the create new file window, fill in the cell name, make sure Virtuoso is selected for the Tool and then click OK. This will bring up the XL layout editor window and the LSW window.

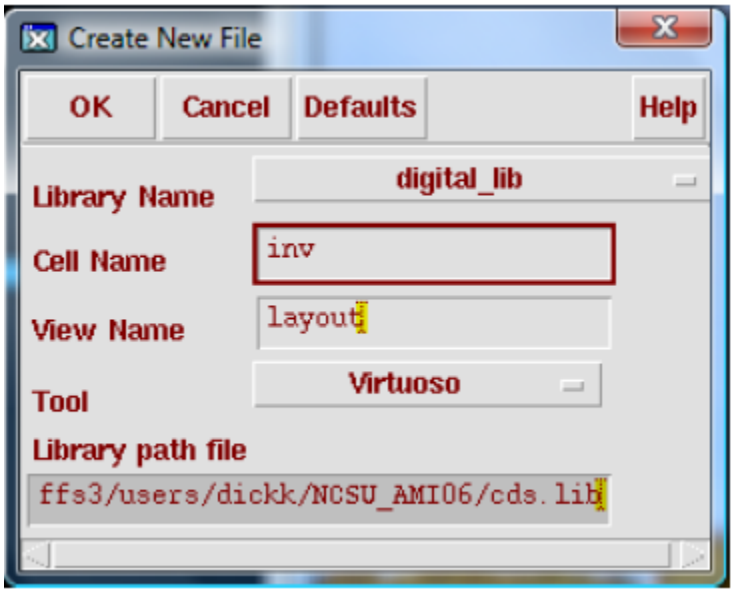

Figure 2: Creating a new file

Figure 3: XL Layout Editor

2) Setting up the parameters

2.1) In the XL layout editor, go to the Design tab, and click on Gen From Source. This will bring up the Layout Generation Option window, in which you can select the options for generating the layout. Make sure that they match the selection below.

Figure 4: Setting up layout options

2.2) Go to the tab, Options, and select Display. This will allow you to select what is being displayed on the layout screen. To see the different levels inside the transistor change the display level stop to 32.

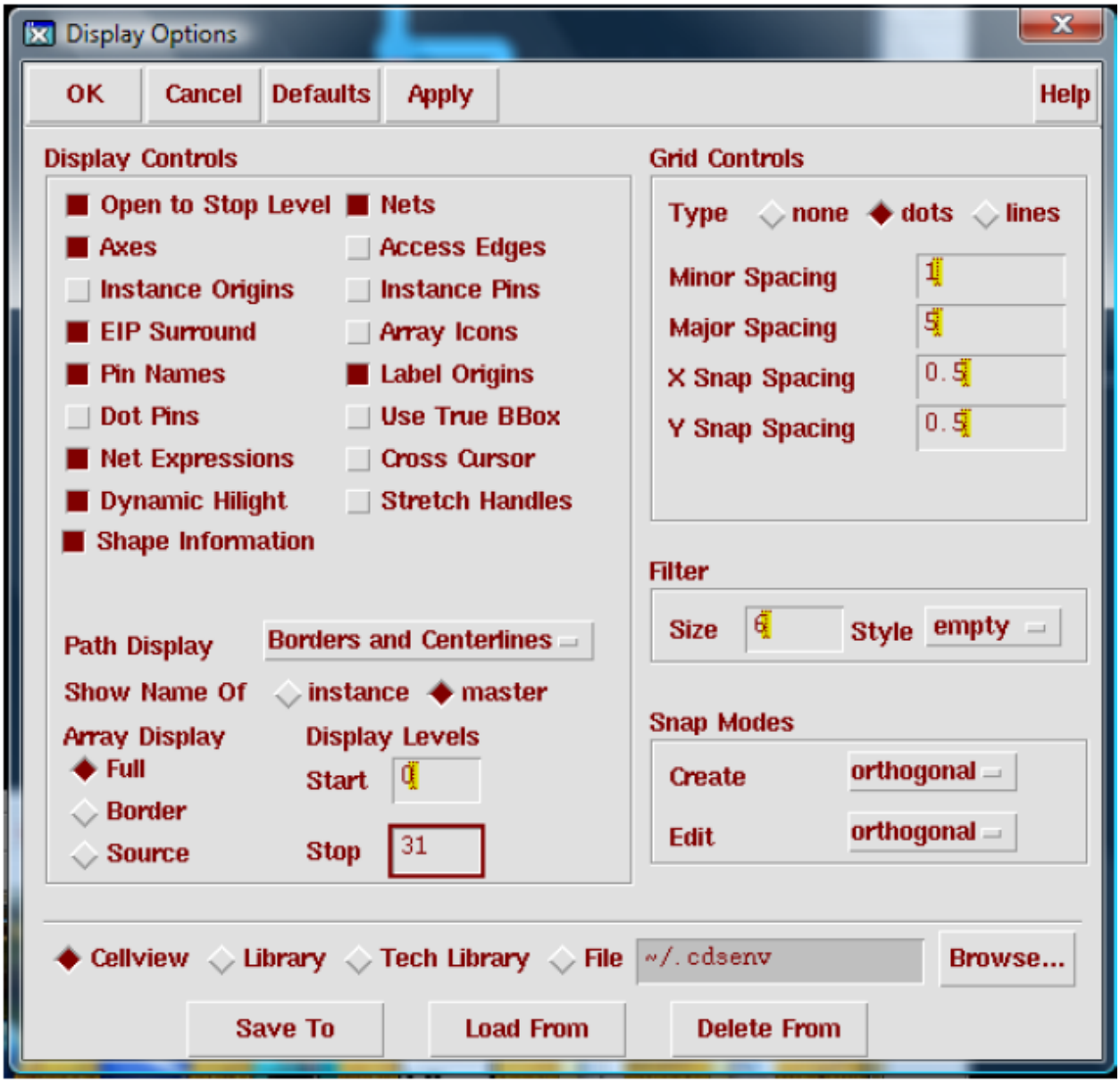

Figure 5: Display options

3) Setting up the connections

3.1) To move your components around select the move tool, on the left side bar. Move the components into the first quadrant and position them so that they can be connected.

3.2) When you select a component to move in the XL layout editor window, the component will be highlighted in the schematic window. It will also show you what else it is connected to by showing a line to the connection. This will help you, if you forget what something is connected to.

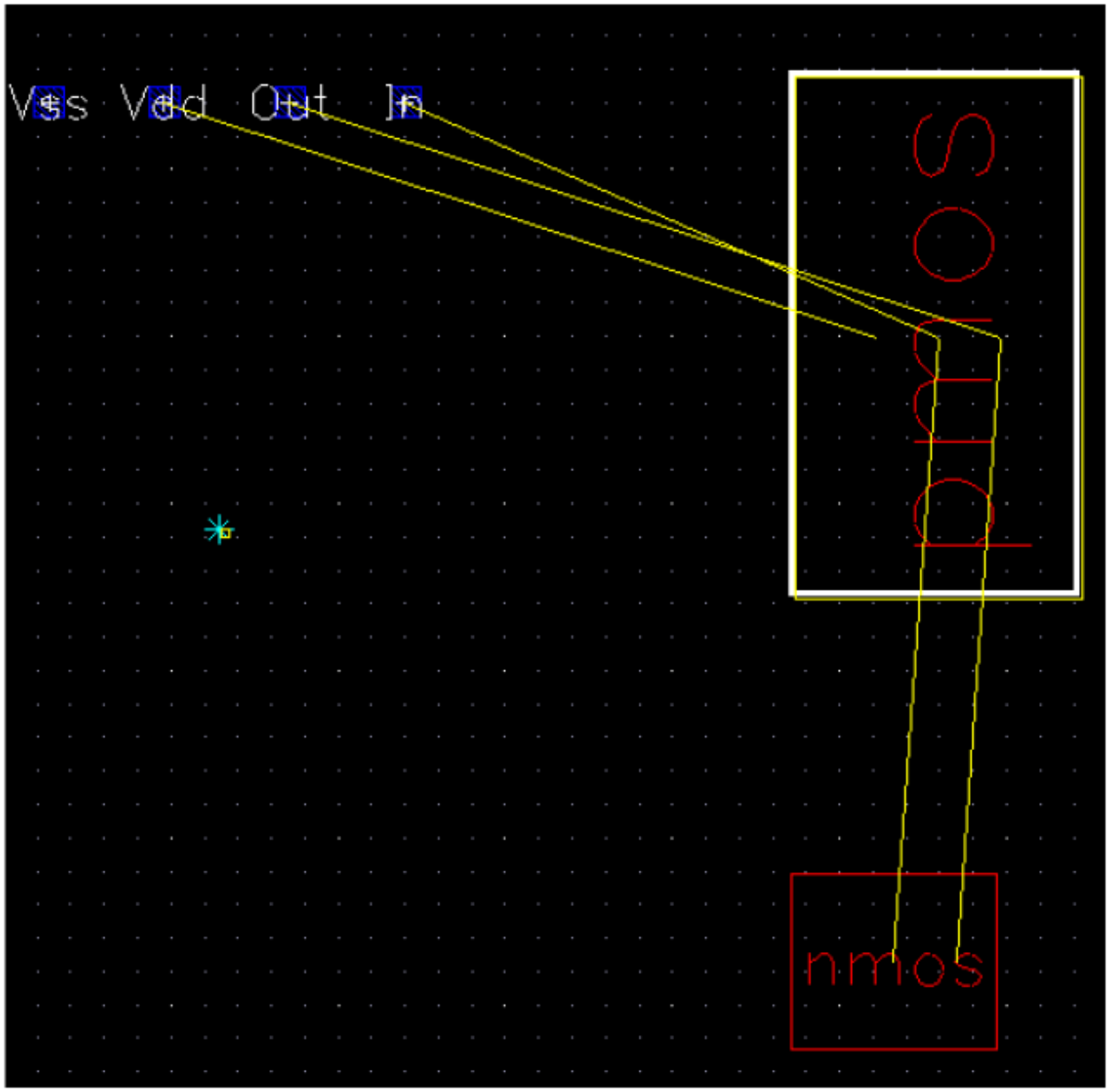

Figure 6: Moving pins and transistors

3.3) To connect the components together go to the LSW window and select the intended layer and select the rectangle tool from the left side bar in the LX layout editor window. Connect the nmos and pmos gates with poly and the pins with metal1. To connect the input pin to the poly you will need the poly to metal 1 via.

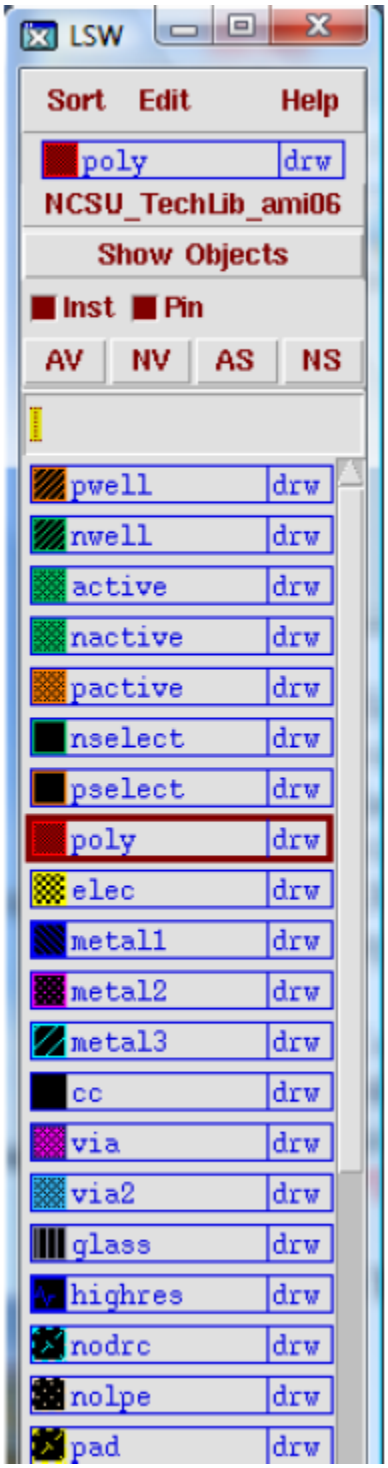

Figure 7: LSW window

3.4) Make sure to keep your cells the same height so that they will be easy to connect to each other.

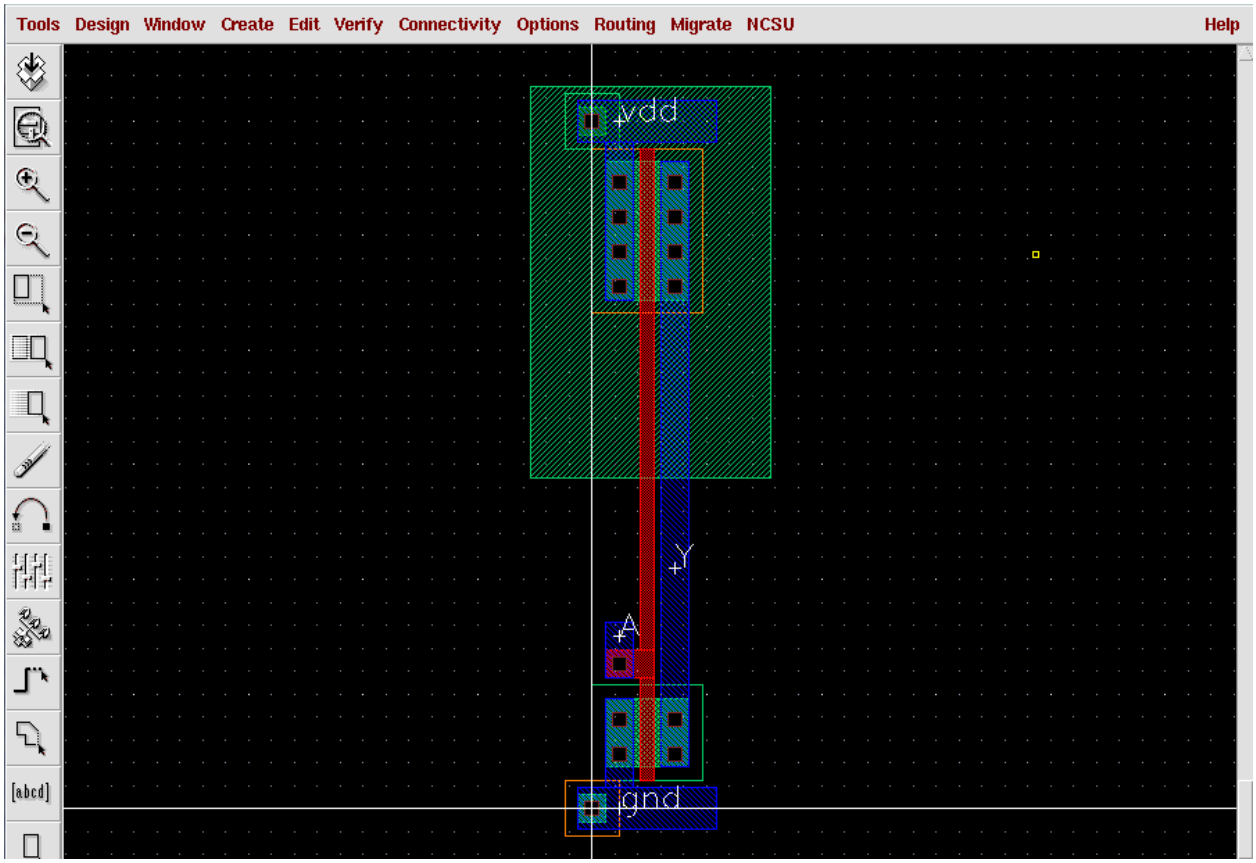

Figure 8: Final layout design of an inverter

4) Running DRC (Design Rule Checker)

4.1) Throughout the design process, make sure to run DRC, which is located under the tab, Verify. When the DRC window appears click the OK button for it to run. The DRC check will give you the number of the rule, if there is a violation.

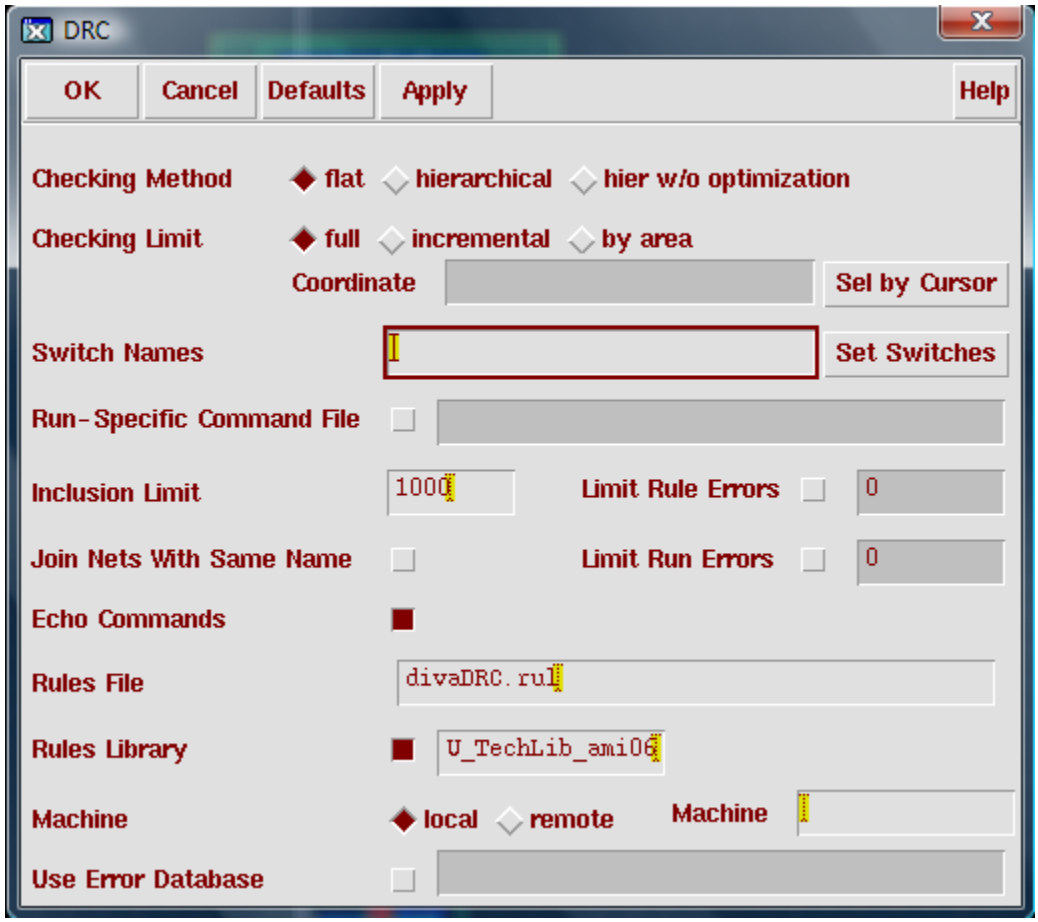

Figure 9: DRC window

4.2) The results of the DRC can be viewed in the icfb log window. It will list the number of errors as well as the rule that was violated.

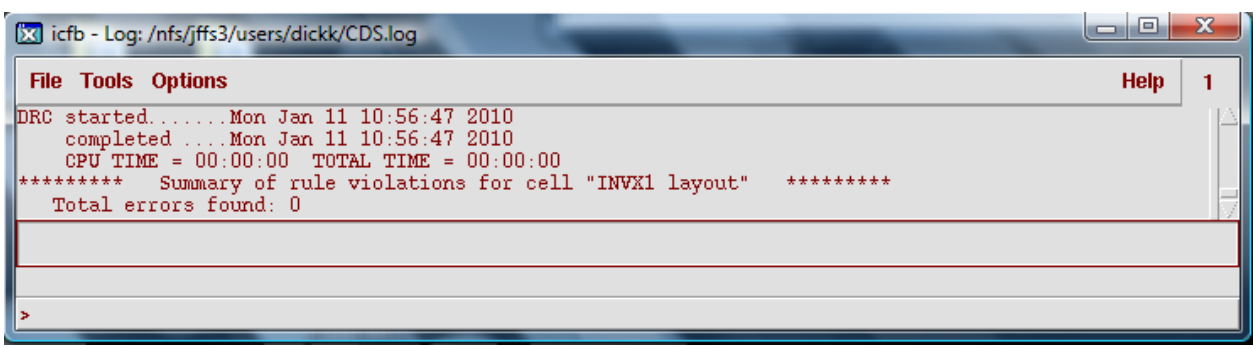

Figure 10: Checking the results of the DRC

4.3) One of the DRC errors that you might encounter is an off the grid error. This happens when wire nets or symbols are not on the same grid. There is a default grid setting, but it can be changed. It is under the display options. It is a good idea to keep them on the default settings. This can also occur if you use symbol created on a different grid setting. For example if you create an inverter symbol instance on a grid with minimum of 0.3 you can draw the inverter symbol such that it is 2.4 X 3.6 in size. However, if your grid is set at 0.5, then errors will occur during the DRC check. A 0.5 setting could handle 2.5 X 3.5. In other words, if you

use a W and L that is not a multiple of the minimum grid setting you will get an "off the grid error".

5) Extracting the circuit

5.1) After you have finished the circuit you will need to extract it. This can be done by going to Extract under that tab Verify. This will allow you to check the circuit against the schematic to see if they are equivalent. When Extract is selected a window will appear that gives the extract information. Click on the OK button.

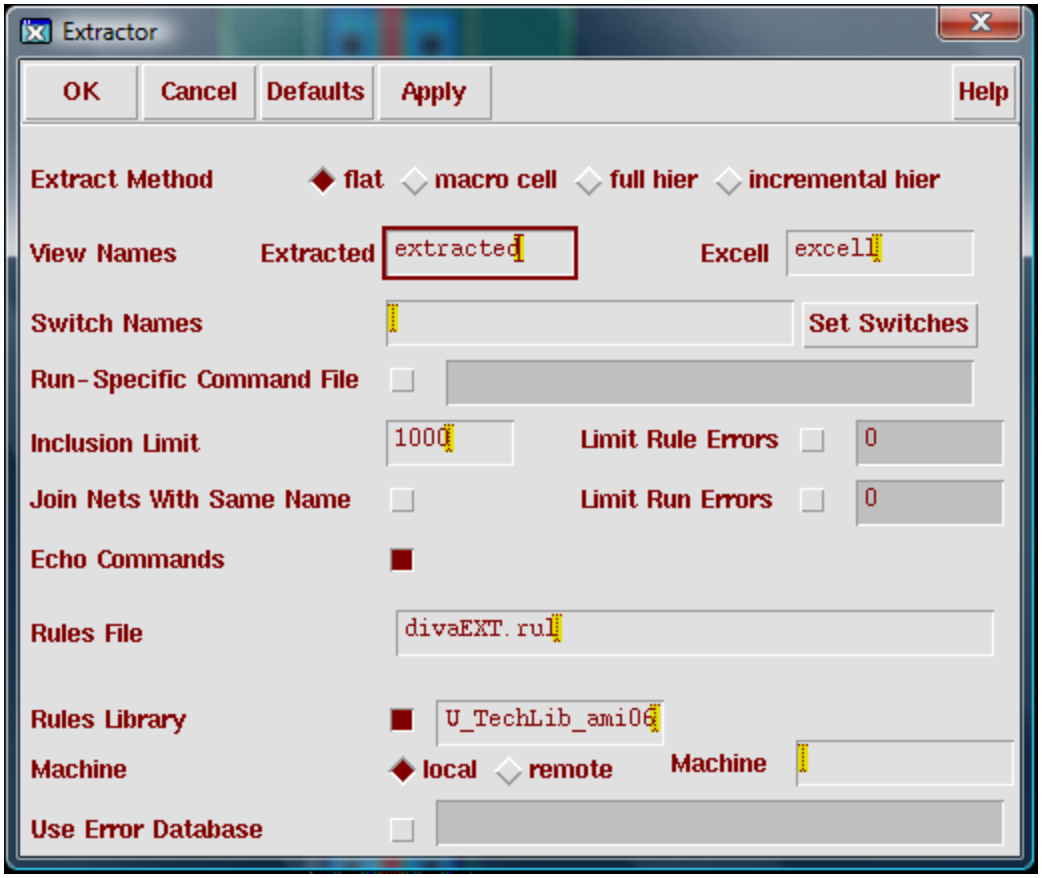

Figure 12: Extract window

6) Running LVS (Layout versus Schematic)

6.1) When you are done laying out the inverter in the layout window you can compare it to the schematic to see if they match. This can be done by using LVS. LVS is located under the tab Verify.

6.2) When LVS is opened an LVS contents window will appear. This is the window that lists the contents of what is going to be compared. If it does not match what you desire to compare then go to the Artist LVS window and fill in the correct information for the schematic and layout. You will need to fill in the Library that the schematic and layout are in, the cell name for the schematic and layout and the view name. Then click on the Run button, located in the bottom left.

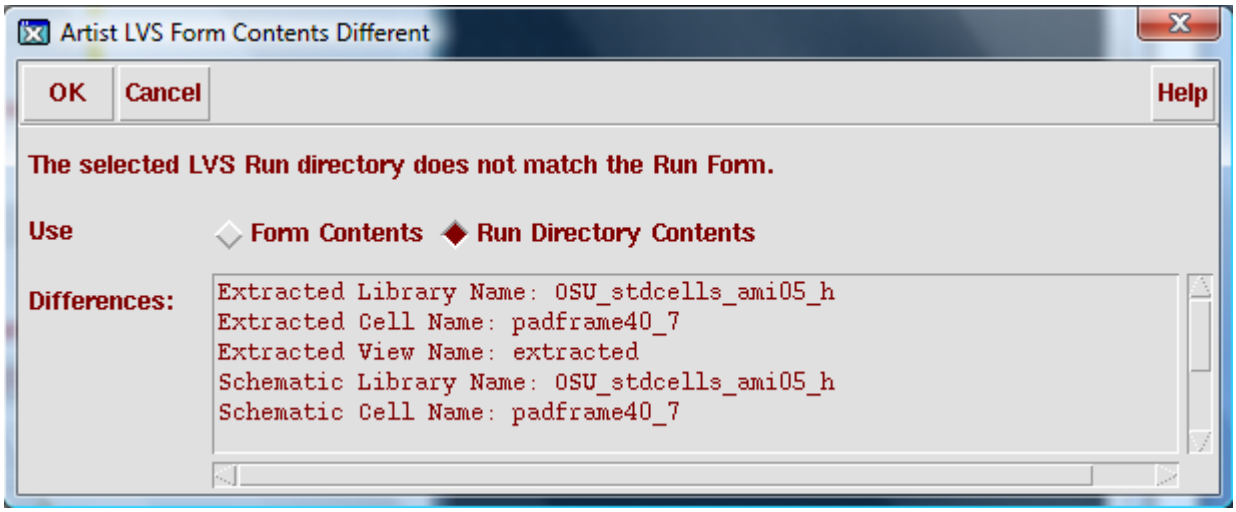

Figure 11: LVS contents window

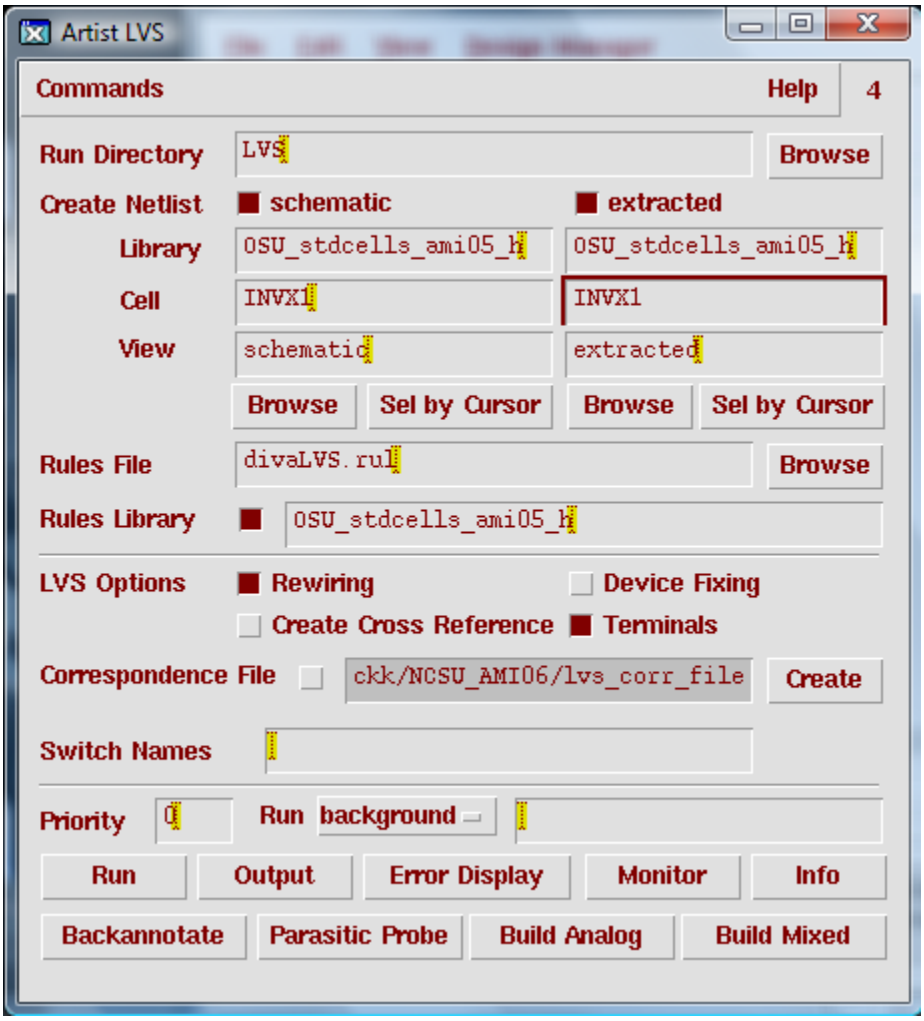

Figure 12: Artist LVS window

6.3) When the LVS is complete a window will appear that will let you know if the layout and schematic matched. The result of LVS can also be seen in the icfb window.

Figure 13: LVS Result window

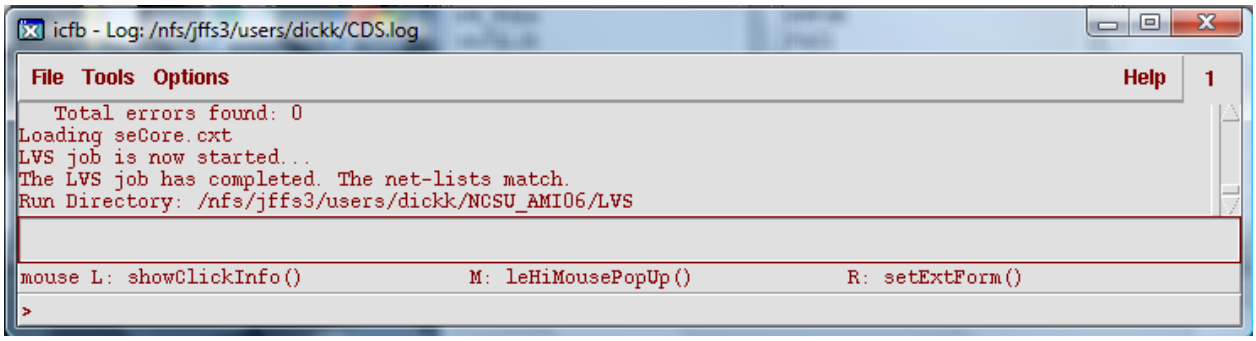

Figure 14: icfb window